ISBN: 978-3-95450-254-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS1991-S02SRU11

A New Architecture for Fermilab's Cryogenic Control System

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Abstract

In order to achieve design energy in the Tevatron, the magnet system will be operated at lower temperatures.[1] The increased requirements of operating the Tevatron at lower temperatures necessitated a major upgrade to the both the hardware and software components of the cryogenic control system. The new architecture is based on a distributed topology which couples Fermilab designed I/O subsystems to high performance, 80386 execution processors via a variety of networks including: Arcnet, iPSB, and token ring.

Introduction

The addition of "cold compressors" to the Tevatron's satellite refrigeration system, as well as the desire to dynamically balance the site's distributed compressor load, introduced additional performance requirements on the cryogenic control system. The required signal processing capabilities basically doubled, raising the number of I/O terminations to approximately 2,000 per satellite.

To effect global optimization the system's software also required significant enhancements. These included: support for global communications between refrigeration processors, an improved user interface to the finite state machines, both code and parameter down-loading capabilities, and substantially improved diagnostic support for the system's hardware.

Together, the performance criteria exceeded the capabilities of the original, Z80 based control system[2]. Therefore, a complete upgrade was warranted.

The new architecture

To achieve the desired performance with a minimum of hardware, we adopted a distributed architecture centered around Intel's 32 bit, 80386 microprocessor. Multibus II was selected as the hosting platform. We prefer it not only for the architectural advantages it offers, but also because of the existing support services which have already been developed for our front end computers[3]. The substantial amount of hardware and software that we were able to inherit allowed us to concentrate the majority of our efforts on developing smaller, more efficient I/O subsystems.

We partitioned the control system into six sectors following the physical distribution of satellite compressors around the Tevatron. Each sector consists of four satellite refrigerators and their associated compressor. The sectors are connected by a token ring network to effect global communications.

Each satellite unit is controlled by an Intel, iSBC 386/120 single board computer. The five CPU modules reside in a common Multibus II chassis which is located at the compressor installation. The loosely coupled architecture of Multibus II is ideally suited to this application. It supports protected, independent execution for each processor module, while simultaneously providing fair access to centralized system services. These services include: a Tevatron clock distribution processor, a "machine data" (MDAT) I/O module, global shared memory, a DOS based 386PC/AT for system initialization and diagnostics, and a token ring processor for global communications.

Inter-processor communications within the sector are accomplished over the parallel system bus (iPSB) which, in conjunction with the message passing protocol of Mutibus II, functions as a 40 megabyte per second local area network. The crate configuration is illustrated in Figure 1.

* Operated by the Universities Research Association Inc., under contract with the U.S. Dept. of Energy.

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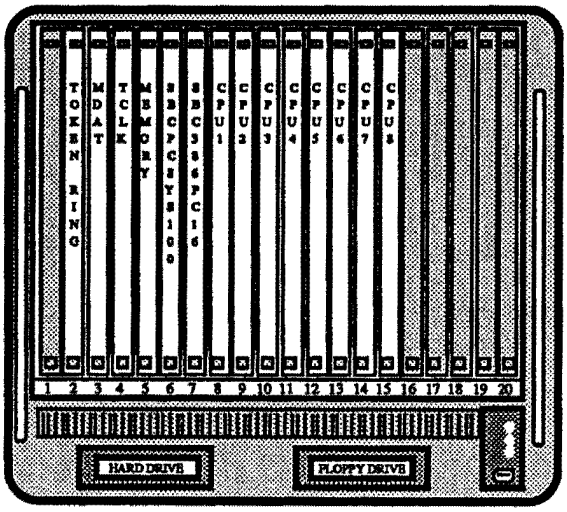


MULTIBUS II CRATE

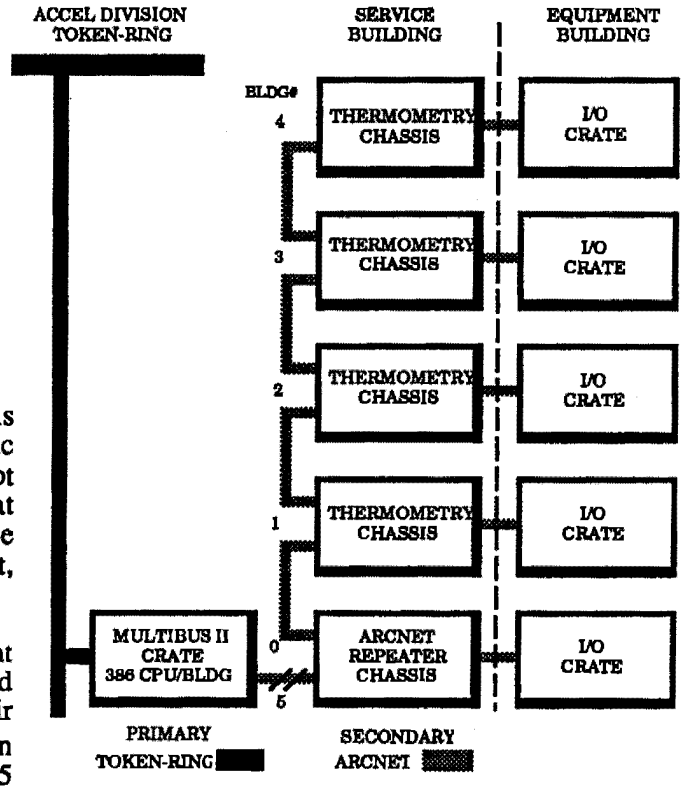
FIGURE 1

Subsystem communications

Control for each of the satellite refrigerators is further divided into two I/O subsystems: Cryogenic Thermometry and Device I/O. (Compressors do not require thermometry .) The subsystems are located at the source of their respective signals and are connected to the execution processors by Arcnet, which functions as a small area network.

Arcnet is a low cost, highly reliable network that supports up to 255 nodes and can be implemented over a variety of media including coax, twisted pair and fiber[4] . It utilizes a deterministic "modified token passing" access scheme with a data rate of 2.5 megabits/second and a packet size of 512 bytes. It has a very simple protocol and all of the network services are provided at the silicon level by a variety of commercially available controller chips. The controller interfaces to a system through a page of dual ported RAM, and a single command/status register. To initiate a network transmission the host processor simply loads a message packet into the RAM buffer and issues a "transmit request". Message packets consist of a source ID, a destination ID, the message byte count, and up to 508 bytes of user defined data. All messages are accompanied by a 16 bit CRC character which the receiving node uses to verify the integrity of the transmission. Additionally, all error free transmissions are positively acknowledged.

There are no hardware imposed restrictions on communications within a sector. Each node is permitted equal access to all the other nodes on the network, thereby allowing a variety of logical topologies. Currently, a Fermilab designed protocol layer called "Virtual I/O Bus" (VIOB)[5] , manages communications between the execution processors and the I/O subsystems. VIOB enables the subsystems to appear as extensions of the execution processor's local buses. The current topology for a single sector is illustrated in Figure 2.



COMMUNICATIONS TOPOLOGY

FIGURE 2

The I/O subsystems

The basis for each of our subsystems is a 16 Mhz Intel 80C186EB functioning as an I/O processor. The "EB" is a low power, CMOS version of Intel's 80186 embedded microprocessor. It is based on a modular CPU core that integrates most essential system services onto a single 80 pin package. The object code of the 186 is directly compatible with the "real mode" of the 80386 microprocessor. Hence, a subset of the tasks developed for the execution processors could, in the future, be ported to the I/O processors as a way to further improve software performance.

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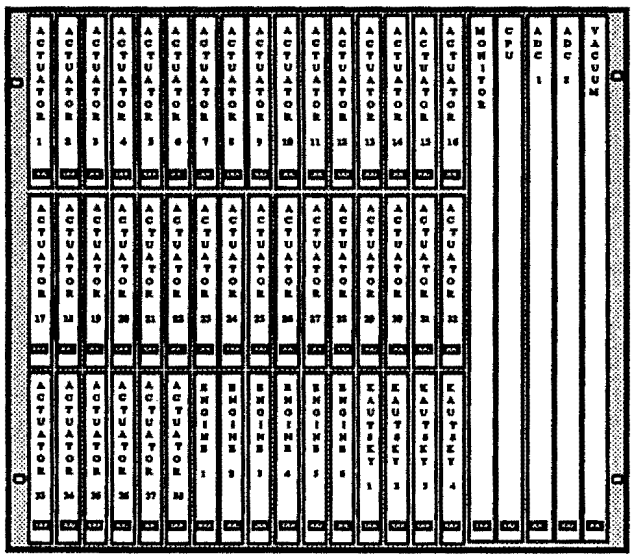
The Device I/O subsystem

The Device I/O subsystem includes support for 128 transducer inputs, 38 actuator valves, 32 helium relief valves, 12 vacuum gauges and 6 "wet" or "dry" expansion engines. The subsystem is housed in a Euro-chassis located within the cryogenic equipment building. The current configuration is illustrated in Figure 3.



EQUIPMENT BULDING I/O CRATE

FIGURE 3

Activity within the subsystem is orchestrated by a 9U size processor module which hosts the 80186EB. In addition to those system services provided by the 80186, the processor module also provides fast data logging facilities, Tevatron clock decoding, the Arcnet interface, and distribution of various clock signals.

The I/O processor interfaces to the rest of the system via three identical backplane buses referred to as the "F2" bus. The F2 bus was developed in house to overcome the difficulties associated with cabling an average number of process I/O signals to a 3U size Eurocard while simultaneously supporting a high performance 16 bit bus interface on a single 96 pin DIN connector. It provides 32 pins of user defined I/O at each slot along with addressing space for up to 512 sixteen bit memory mapped registers. The individual slots are mapped to the I/O processor's memory and are individually selected in a fashion similar to the CAMAC standard.

Transducer interfacing is accommodated by two, 9U size A/D converter modules. Each module supports 64 differential input channels with a 10 volt range. The analog front end consists of two stages of input multiplexing, an instrumentation amplifier, and a 12 bit, self calibrating ADC. To facilitate fast data logging all 64 channels are digitized within a one millisecond period. The results are stored in a double banked, dual ported RAM. The arrangement allows the I/O processor fast access to the digitized data with a minimum of arbitration conflicts.

Actuator Control cards provide a comprehensive interface to the Barber–Coleman electromechanical valve actuators used throughout the cryogenic system. Each 3U size card incorporates all of the functionality necessary to interface a single device including: 24 volt DC drive control, Linear Variable Differential Transformer instrumentation, and A/D conversion circuitry. A local front panel control mode is also provided.

Wet engines, dry engines and cold compressors[5] all interface to the control system via Engine Control cards.[6] Each 3U card provides momentary relay contacts to implement "start", "stop" and "reset" commands. Also included are two independent channels of analog I/O (one for engine speed and one spare), and 16 optically coupled status bits. A front panel display reflects the state of both command and status bits.

The variety of solenoid valves used throughout the cryogenic system are interfaced by Kautzky[7] Control cards. Also implemented in the 3U format, each card provides control and status readback for up to eight solenoids. A front panel display reflects both the actual state and the requested state of each valve.

Pirani (vacuum) gauges are interfaced by a 9U size Vacuum card. The card supports 12 transducer circuits. A free running, multiplexed A/D converter continuously scans the transducer voltages, storing the digitized results in a dual ported RAM buffer.

Miscellaneous status bits are monitored by a Digital Input card. The 3U size card supports 30 bits of optically coupled status with input voltages ranging from 5 to 24 volts D.C.

The thermometry subsystem

The thermometry subsystem supports 96 channels of pulsed current, resistance thermometry. Unlike the Device I/O subsystem, it is implemented as an

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application specific single board computer. It resides in a NEMA–12 enclosure mounted along the back wall of the Tevatron Service building.

The free running measurement scheme uses a precision current source (along with six stages of multiplexing) to deliver a 50 microsecond current pulse to each resistor module. The voltages developed by the resistors are scaled by a programmable gain instrumentation amplifier before being digitized by a 12 bit, self calibrating A/D converter. Here too, a dual ported RAM is arrangement is used to store the digitized results.

The subsystem also maintains a hard-wired 16 bit bi-directional data link with the Tevatron Quench Protection system (QPM). In the event of a magnet quench, the QPM provides the refrigeration control system with specific cell information to assist automatic recovery schemes. The refrigeration system provides the QPM with a permit allowing the magnets to be turned on.

Reliability and system diagnostics

One of the notable benefits of using the Multibus II architecture is the emphasis that the platform places on confidence testing and system diagnostics. Every module in the system supports a standardized set of "built in" self tests (BIST). During the initialization phase following a power–on reset, each module executes a subset of these routines to test its own functionality. The results are posted in "interconnect space" and are globally available to the rest of the system. Upon the coordinated completion of a reset, one module (in our case the PC16) assumes a temporary role as the systems' "boot master". The master can subsequently invoke, or download additional tests for each subsystem on an individual basis. This can be accomplished locally via an RS232 port or from a remote facility with the use of a modem.

Upon completion of confidence testing the operating system and refrigeration specific application software are down-loaded via the iPSB. At that time the execution processors are started and the PC16 relinquishes control of the system. The PC16 is now free to be utilized as a local information data base or console emulator by technical personnel. System schematics, diagnostic flowcharts and related maintenance histories can be displayed, as well as any other useful DOS based application.

Conclusion

The use of a hierarchical, networked architecture is ideal for this application. The higher cost, 32 bit microprocessors have been de-coupled from the cryogenic system, thereby protecting the investment from premature obsolescence. The distributed subsystems can be incrementally upgraded – or even replaced – with a minimum of impact to the rest of the system. Additionally, the maximum limit of 255 nodes per sector permits almost unlimited expansion of the system.

Acknowledgements

We wish to acknowledge the contributions of those individuals whose efforts were responsible for turning ideas into functioning components for this system, especially: Loren Anderson, Ryan Hagler, Joe Gomilar, Timothy Gierhart, Rich Klecka, Rich Koldenhoven, Robert Marquardt and Thomas Zuchnik.

[1]Fuerst,J.D. "Trial Operation of Cold Compressors in Fermilab Satellite Refrigerators", Advances in Cryogenic Engineering, Vol. 35B, Plenum Press, New York (1990) .

[2] Zagel,J. et al., "Tevatron Satellite Refrigeration Control Subsystem",IEEE Transactions on Nuclear Science, Vol NS28 , p 2153-2154.

[3]Glass,M., et al., "The Upgraded Tevatron Front End"' NIM A, 1990, Vol 293, p.87-92.

[4]Glass,Brett; "The Return of Arcnet", BYTE, February 1991, p119.

[5]Chapman,L. et al., "Microcomputer Software Architecture for Cryogenic Controls", (This conference).

[6]Rode,C.H., "Tevatron Cryogenic System", 12th International Conference on High Energy Accelerators, 1983. p 529-535.

[7]"The Kautzky Valve", Fermilab Reports, June, 1982.