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Control System for a Heavy-Ion Accelerator Complex K4 – K10

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Abstract

Control systems for newly created accelerators, perhaps for the first time, may be designed almost only around international standards for communication and control techniques. This is also true for the project of a control system for the accelerator complex K4-K10 at the Joint Institute for Nuclear Research Dubna. Nevertheless, open systems architecture with construction principles being essential for modern systems of such big devices as particle accelerators leaves designers enough possibilities for solving even very sophisticated problems.

I. INTRODUCTION

The control system of the heavy-ion accelerator complex K4-K10 is similar to the systems developed for controlling the accelerators of other physical laboratories the experience of which was used in preparing the given project [1,2,3]. Nevertheless irrespective of the similarity of accelerators and control problems there are no equal control systems. This depends not only on the differences of accelerators as such but first of all on the time the system was designed and on the present state of computing and communication technique and on the special features of the system architecture, which allow new technical acquisitions during the realisation.

II. THE ARCHITECTURE OF THE K4-K10 CONTROL SYSTEM

The architecture of the K4-K10 control system is based on a two level distributed computing system (Fig. 1). The upper level uses a modular system IEEE 1296 (Multibus) from the Siemens AG [4] (SIMICRO) as well as workstations with UNIX and X Window in the Central Control Room, and is integrated into a system via a Local Area Network (IEEE 802.3).

The standard IEEE 1296 and its realisation in the SIMICRO products allows a high computing power inside every crate (the CPU on-board in the SC^{TM}-systems based on RISC processors providing 5 MIPS and more) as well as the use of CPU with embedded PC/AT 386 in the OSM^{TM} and AMS^{TM} systems[1]. These SIMICRO systems are equipped with a complete set of communication modules for LAN in the IEEE 802.XX standards.

The functions of the system at this level are supported by the operating system SORIX^{TM} - a UNIX^{TM} Real Time version (reaction time for interrupt signals $\leq$ 100 µsec.) and permit an exit to LAN via TCP/IP protocols[2].

Therefore, using the possibilities of the 7 level scheme for the OSI model of open systems, the architecture of the upper level of the control system provides an output to the equipment and to the real time programs as well as a complete support for the TCP/IP protocols for an output to a LAN IEEE 802.XX. According to the loading of the network at this level by means of bridges one may distinguish two LAN segments: one for the workstations WS in the Central Control Room running under UNIX and the other for the Front End Computing. The latter are mainly crates in the IEEE 1296 standard with Real Time UNIX, joining the node computers for data acquisition and handling in the control mode as well as that for graphics and monitoring. They are equipped with terminals, Touch Screens and other man-machine communication devices.

The lower level of the distributed computing system directly corresponding to the equipment and executing devices and based on standards for industrial systems (for example in the VEPP4 [5] CAMAC instrumentation is used at this level) is connected to the upper level by means of the communication environment FIELD BUS (MIL-1553-B). This standard mostly agrees with the demands for a multidrop bus and in 1983 was proposed as a standard protocol for the field bus in accelerator control systems [6]. Together with well developed hand shaking features for the message transfer between bus controllers and remote terminals (RT) this standard allows simple and cheap data transfer to single serving devices, fulfilling simplest functions. For connecting digital measuring devices to the upper level the standard IEEE 488.X is used.

For the most part all the bus controllers (BC) MIL-1553-B are placed on the upper level of the control system. They provide the interfacing of the node computing system to the lower level equipment. The BC for the K4-K10 control system is developed on the basis of a processor module in the Multibus II standard, designed in the Laboratory of Computing Technique and Automation of the JINR using the VLSI of a 32-bit microprocessor set K1839 software-compatible with a micro VAX [7]. The interface controller for the MIL-1553 bus is a piggy-back module for the CPU board. One such BC may control 30 standard interfaces (Remote Terminals) on each bus.

The standard interface of the MIL-1553 bus has to provide a prompt/reply regime. In this case a microprocessor is needed. In the case of simple messages of the type "adjust and/or read" it has to handle the transfer directly.

The use of the MIL-1553 for the communication with the equipment together with the time synchronization channel allows one to put the real time mode on the lowest control level. Such a solution proposed and realized in the GSI [1] relieves the upper control level of the real time business and allows on this level the use of the LAN 802.3 alone without a TOKEN RING (IEEE802.5) as it is done for the SPS/LEP in CERN [2].

1TM SIMICRO, SX, SORIX, OSM, ASM - Trade Marks of SIEMENS AG
2TM UNIX - Trade Mark of AT & T

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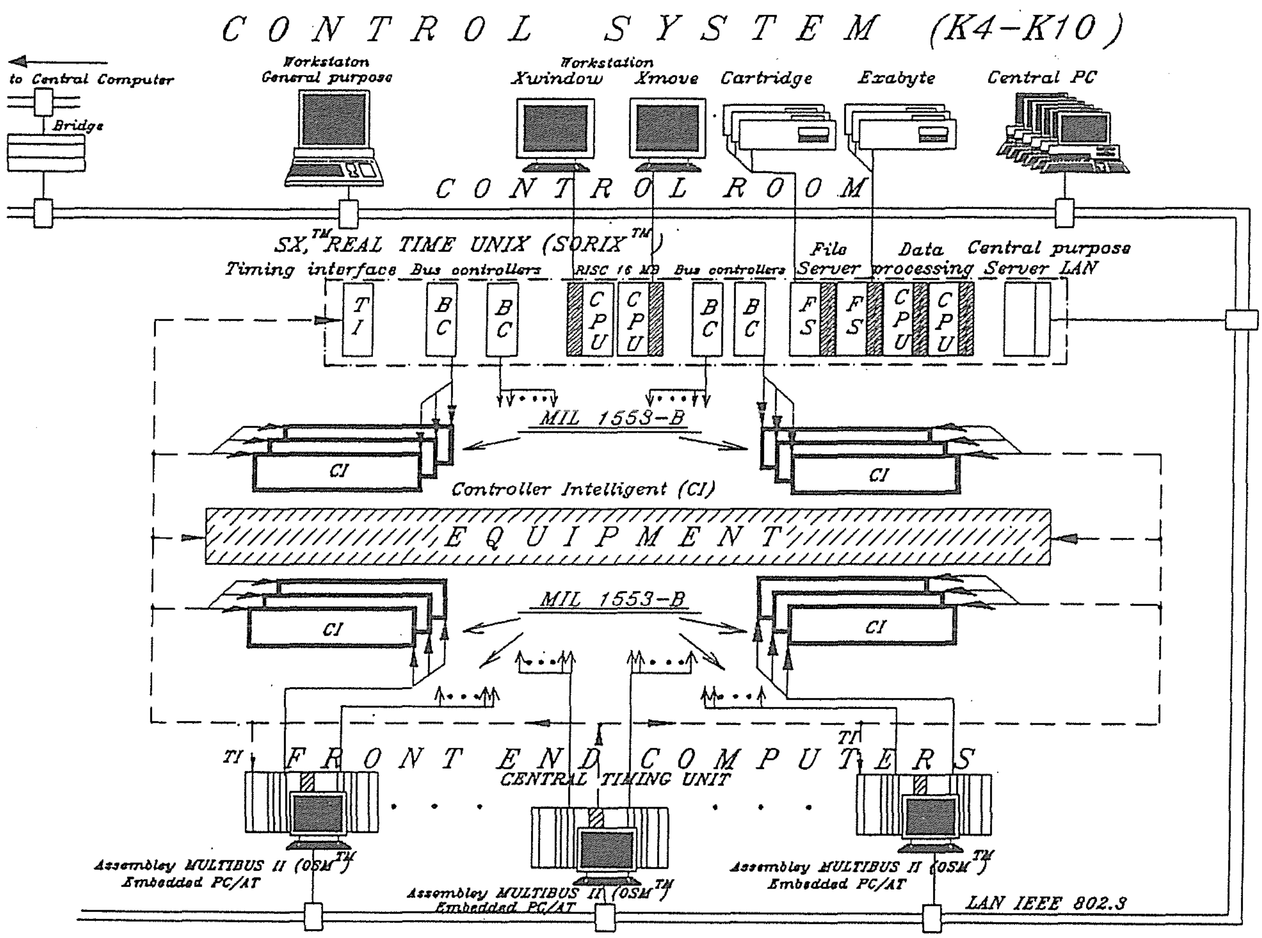

FIG. 1

In the project of the control system for the K4-K10 it is also planned to use such a kind of real time system for the lower control level. But taking into account relatively small dimensions of the accelerator rings of the K4-K10 (the perimeter of the K10 is about 200 m) and the transfer rate of 1 MByte/sec. at distances up to 300 m for the MIL-1553, the connection of the main node computers of the control system at the front-end level may be done without a LAN 802.5, directly on the system bus of the Multibus II with a transfer rate of 40 MByte/sec and full message passing mode. In such a way the possibilities of real time control are widened allowing for this purpose the use of interprocessor transfer in the Front-End Computing of the upper level.

The control system architecture of the K4-K10 allows the use of the standard operating system UNIX and SORIX for the node computers. The main programming languages are C at the system level and NODAL [8] at the application level. The software at the lower control level [2] has to be as short as possible (up to 10 KByte because at this level one may use 8 bit microprocessors) and has to provide a good reactivity: up to 250 interrupts per second with quite long messages on the MIL-1553 and up to 20 Kbyte/sec. All the software on the lower level is part of the system data base. It will be picked out together with all tables of parameter sets necessary for the real time operation and will be stored into the equipment controllers at the lower level.

III. CONCLUSION

The control system architecture for the accelerator complex K4-K10 represents an example of an open architecture system based on the use of control and communication software and hardware corresponding to international standards. Though the system designers have the possibility to introduce their own original technical solutions, the main effort will be directed to the software and hardware design concerning the interfacing part of the system, i.e. the hardware and software ensuring the application of system resources as some kind of a set of control facilities.

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