Ethernet Based Embedded IOC for FEL Control Systems

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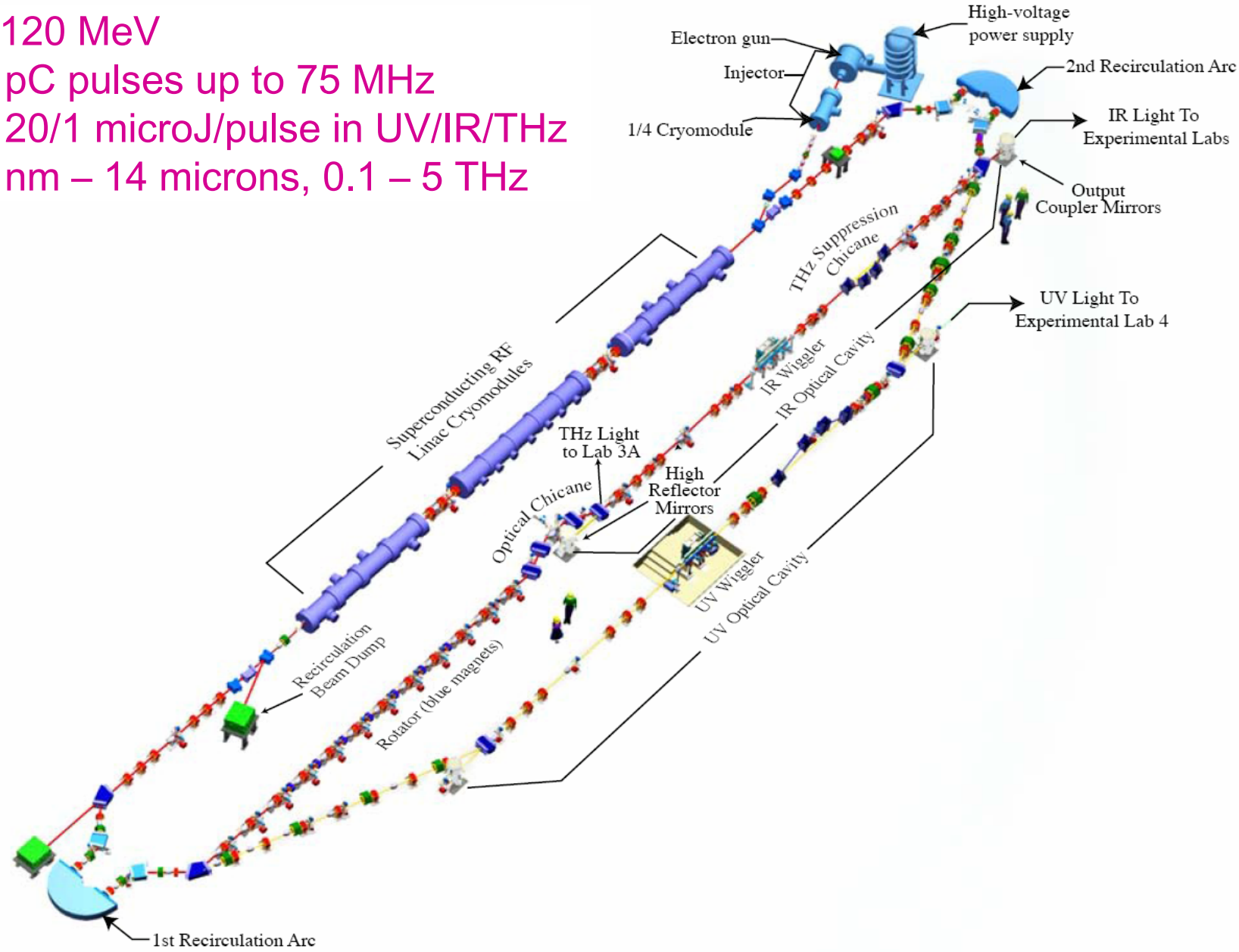
JLab FEL Energy Recovered Linac

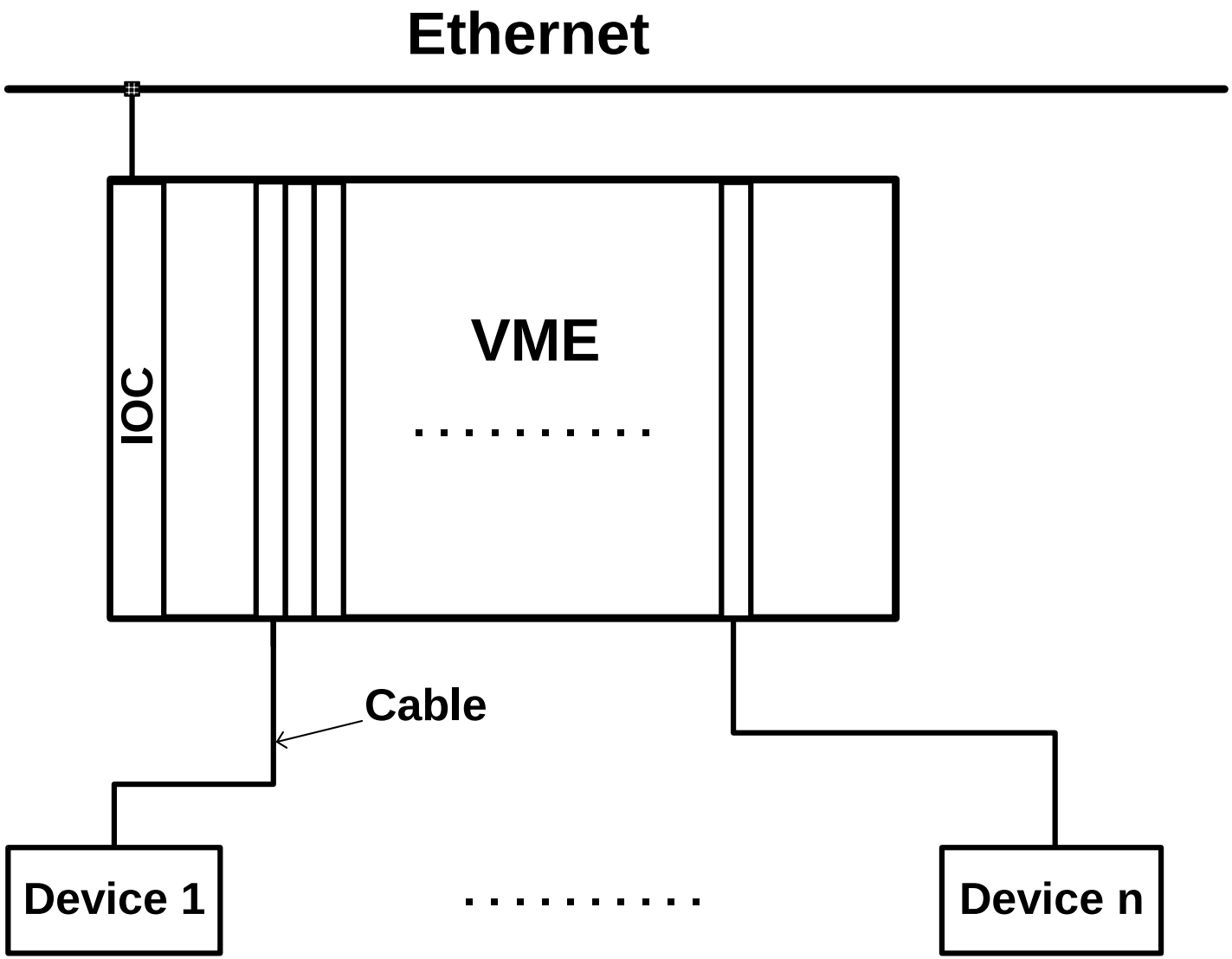
E = 120 MeV
135 pC pulses up to 75 MHz
20/120/1 microJ/pulse in UV/IR/THz
250 nm – 14 microns, 0.1 – 5 THz



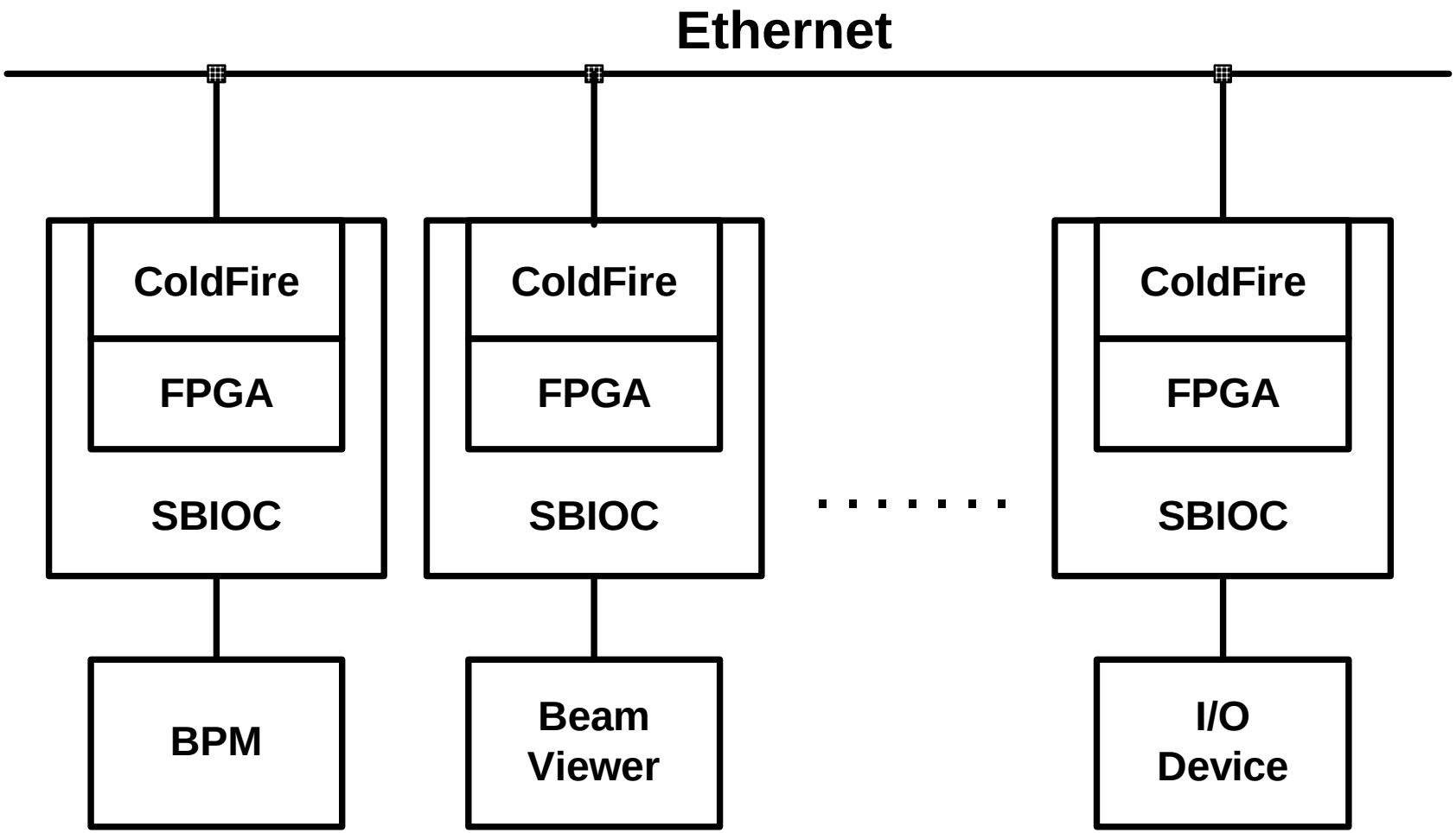
Motivation

- Additional channels for BPM and Viewer systems required
- The cost for expanding the current configuration is high
- FEL “master plan” is to move away from Crate-Based solutions involving licensed software
- Use distributed processors instead of VME IOCs
- Develop a new I/O connection as a “default” standard
- Embedded COTS Arcturus Coldfire Board chosen to start with
- Chose RTEMS as the real-time operating system for the IOC

Current VME IOC System



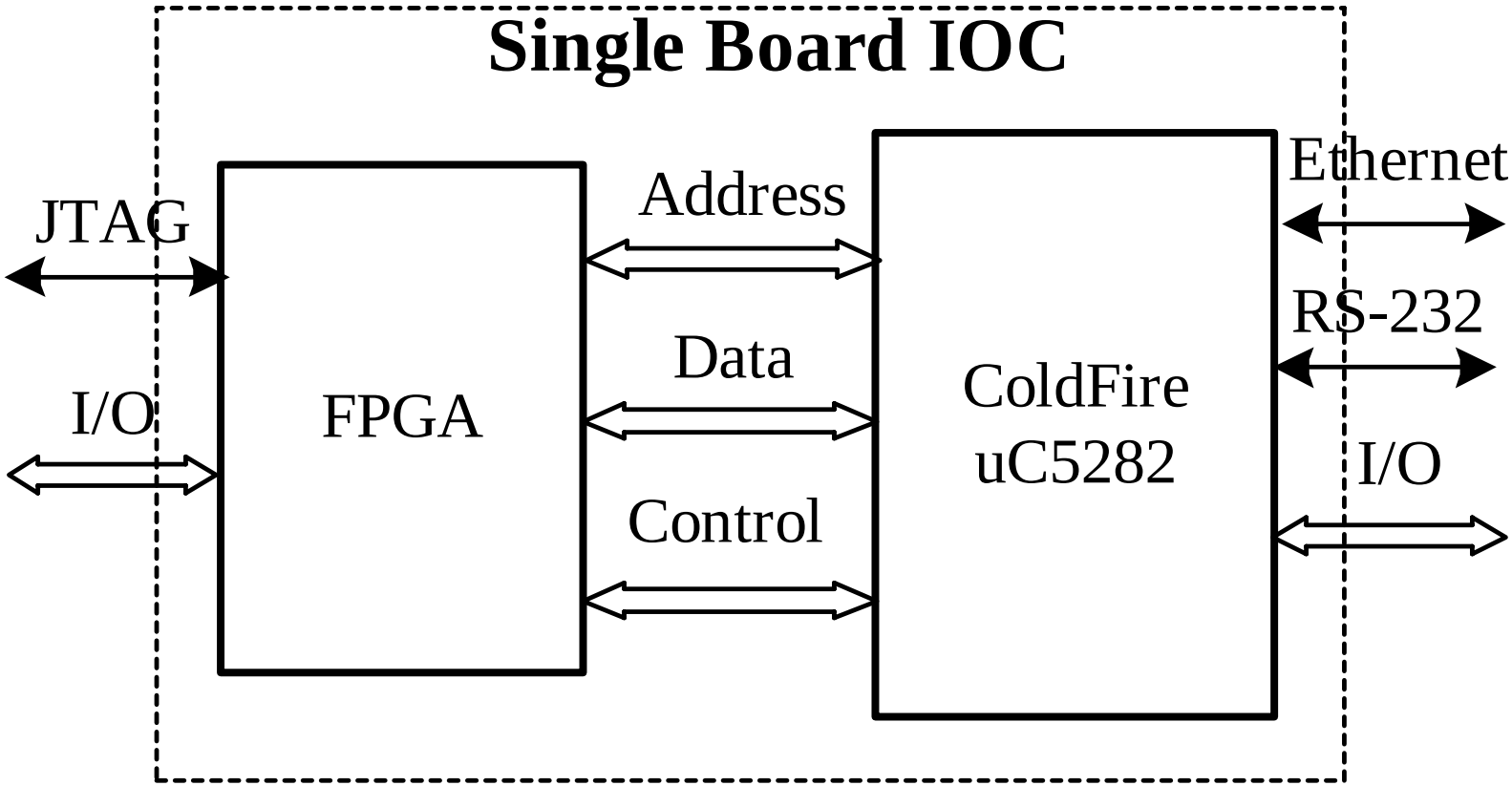
New System Design



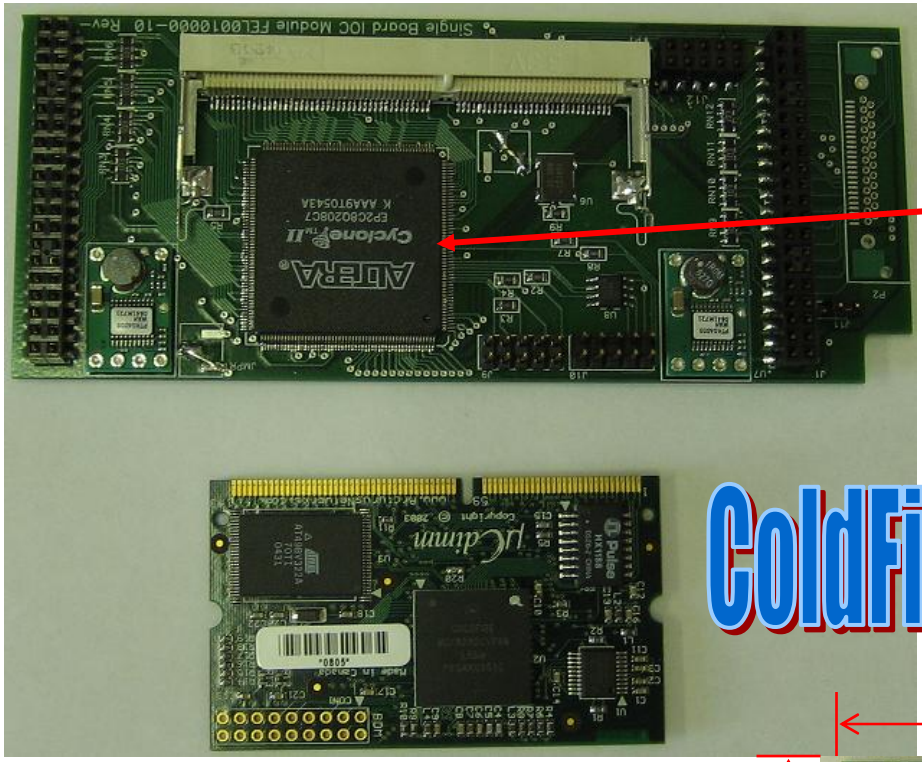
Single Board IOC (SBIOC)

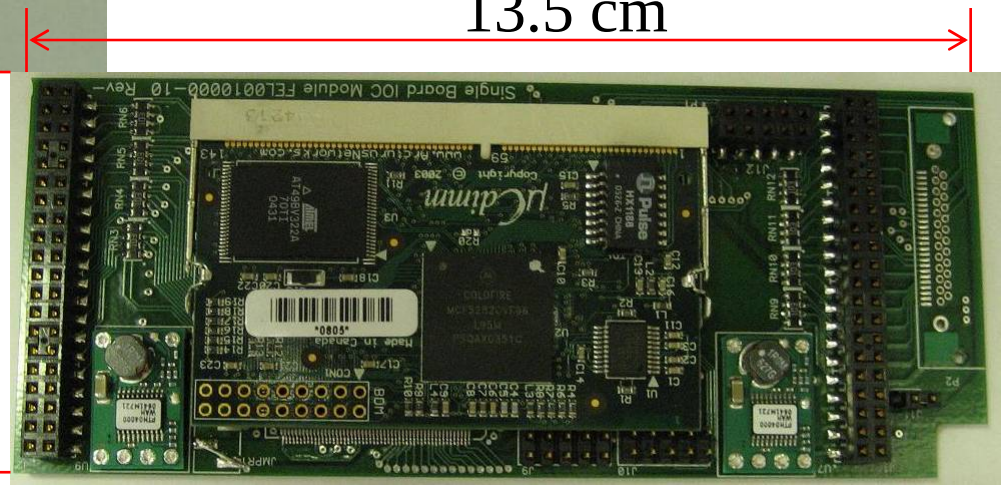
- Integrated a ColdFire uC5282 Microprocessor with an FPGA
- A standard footprint for the embedded IOC
- Provide abundant of I/O connectors
- Compatible with existing designs
- Stand-alone system
- Suitable for most of I/O controls
  - Beam Position Monitor
  - Beam Viewer & Video controls
  - Stepper motor controls

Block Diagram of the SBIOC



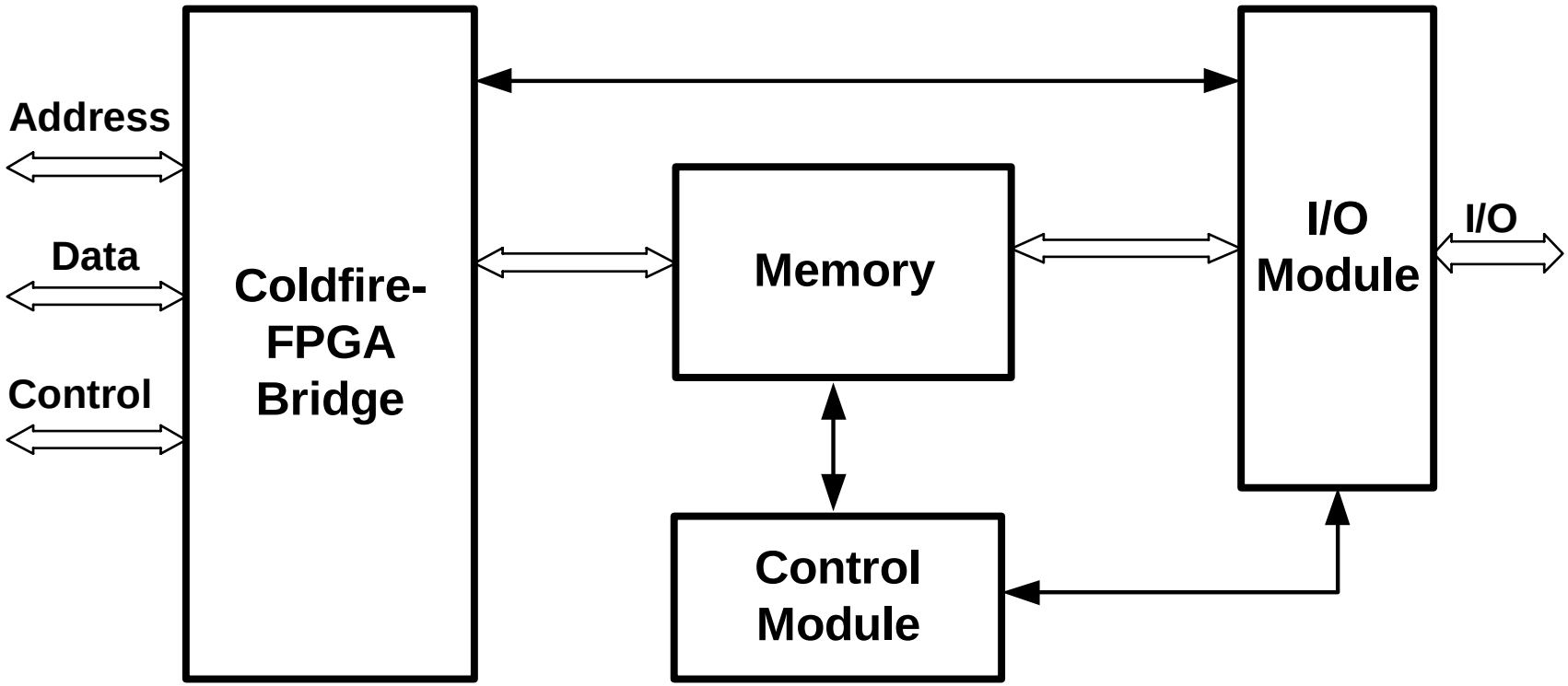
Pictures of the SBIOC



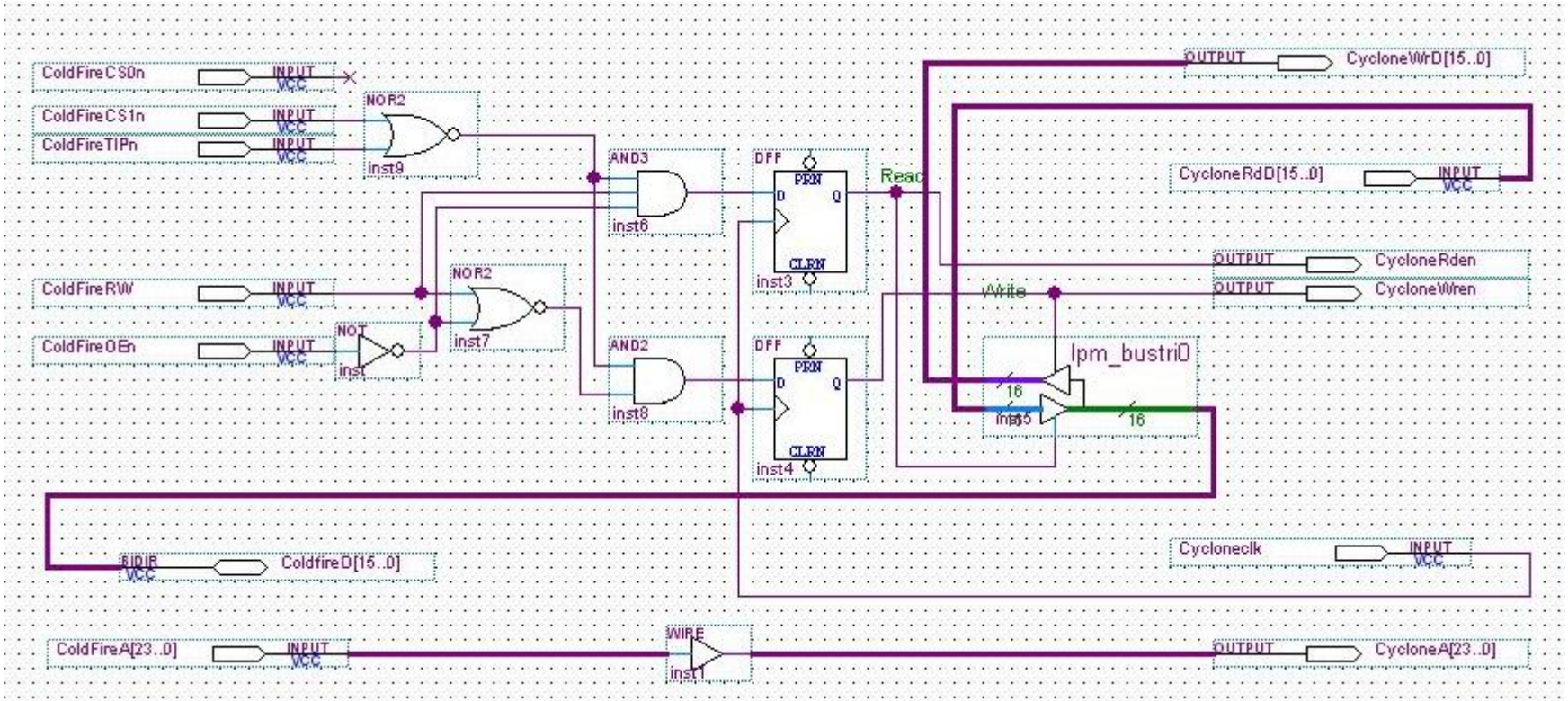


SBIOC Card

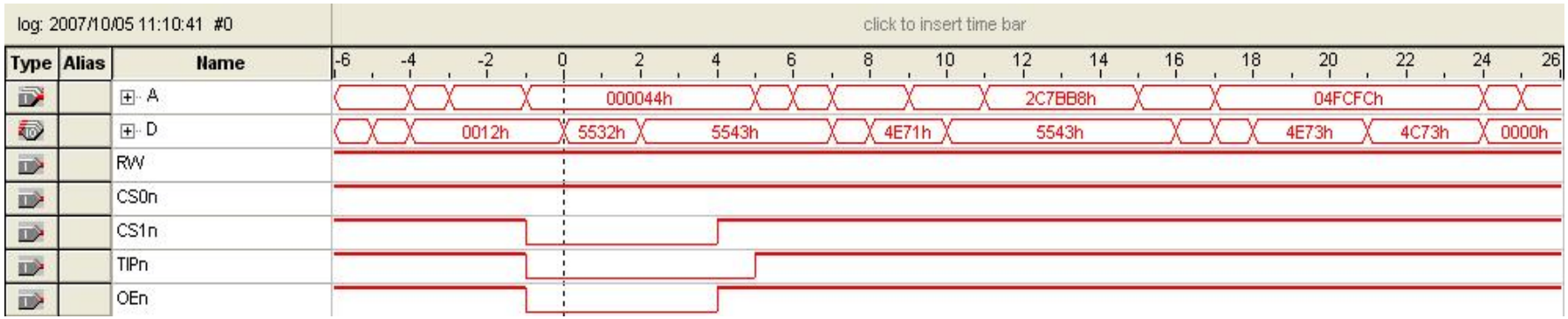
Modules on the FPGA



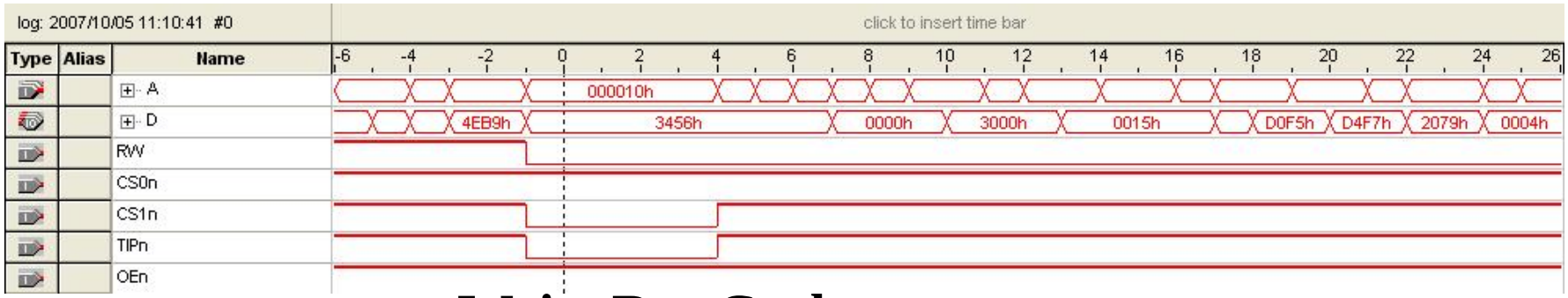
Circuit of the FPGA-ColdFire Bridge



Read and Write Cycles of the Bridge



Read Bus Cycles

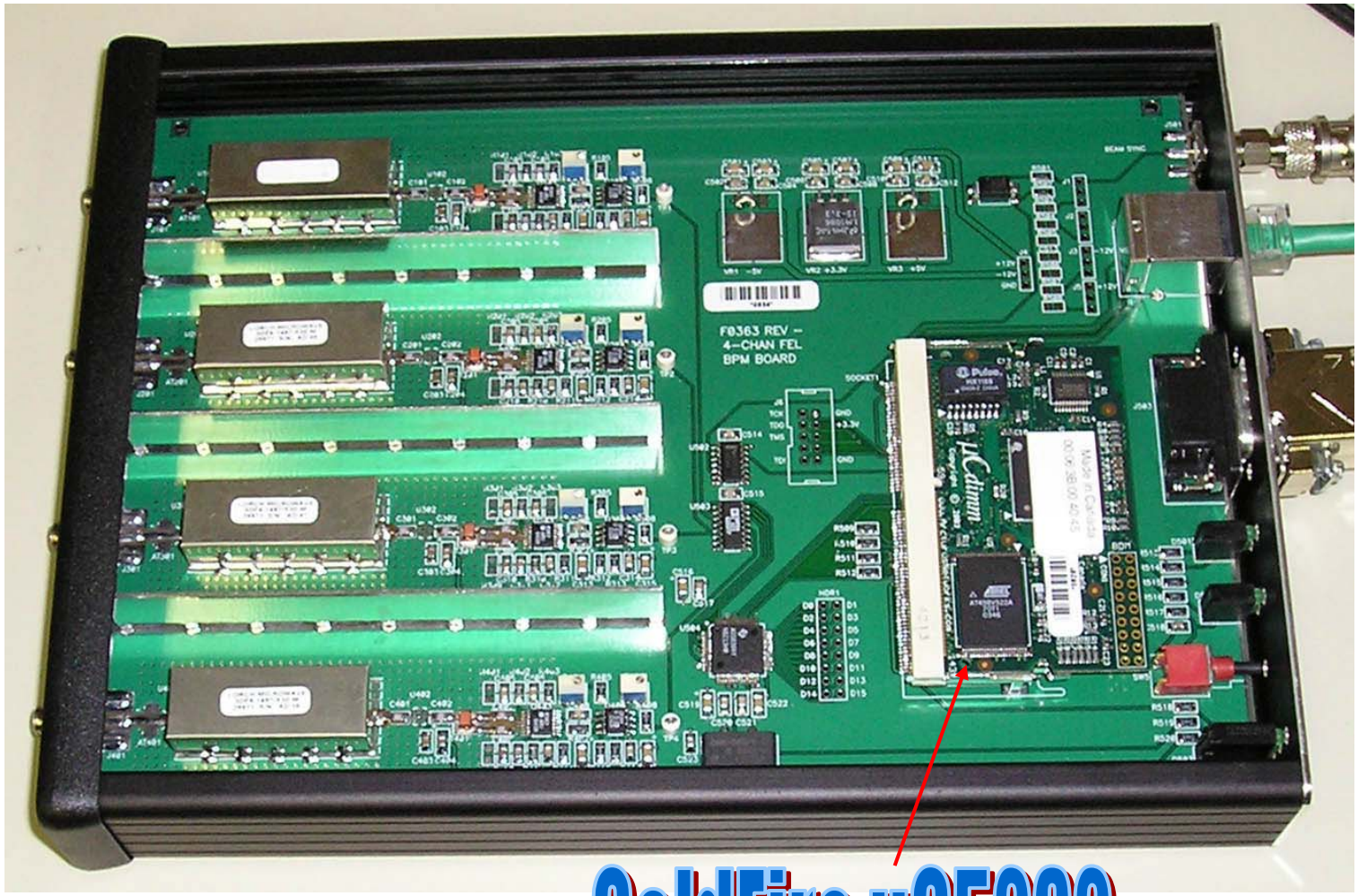


Write Bus Cycles

BPM Applications

- The first version of new BPMs have been running for 2 years
- They are very reliable, and easily maintained
- Throughput from the ADC is 100 Hz. This is a limitation
- New solution has to be found
- Use **Single Board IOC** to improve the performance
- Cut the cost. The cost of original configuration is $3000/BPM; the new system is $1200/BPM

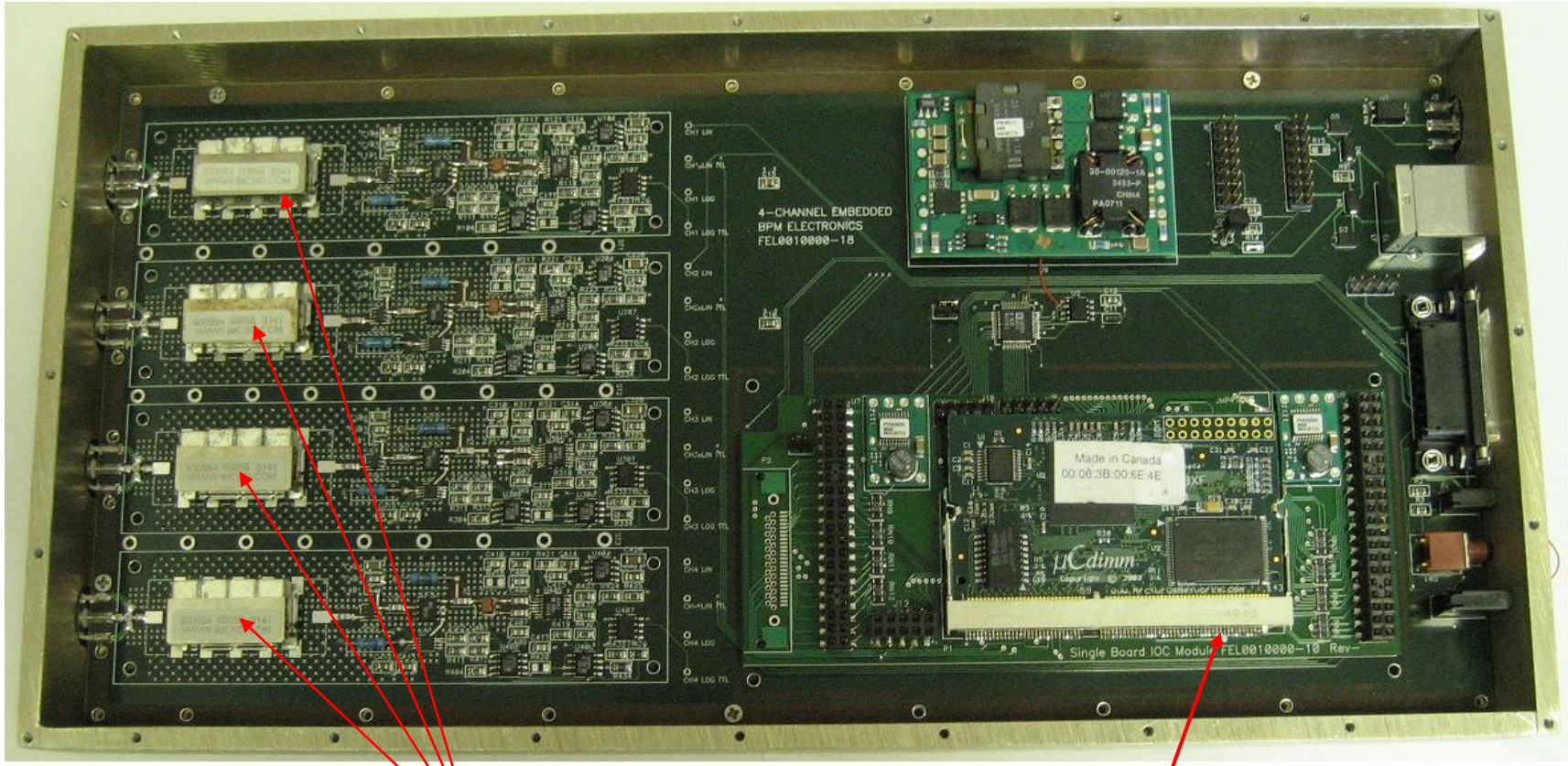
First Version BPM (without FPGA)



New Version BPM

* **FPGA Functions:**
  - Sampling ADC, Calculations (add & average)
  - Communication with the ColdFire processor
* **Goal: 100KHz throughput**
  – FPGA clock 20 MHz
  – ADC 1 MSPS throughput
  – FPGA sampling frequency up to 2 MHz
  – Memory block to save data
  – ColdFire processor read data through bus

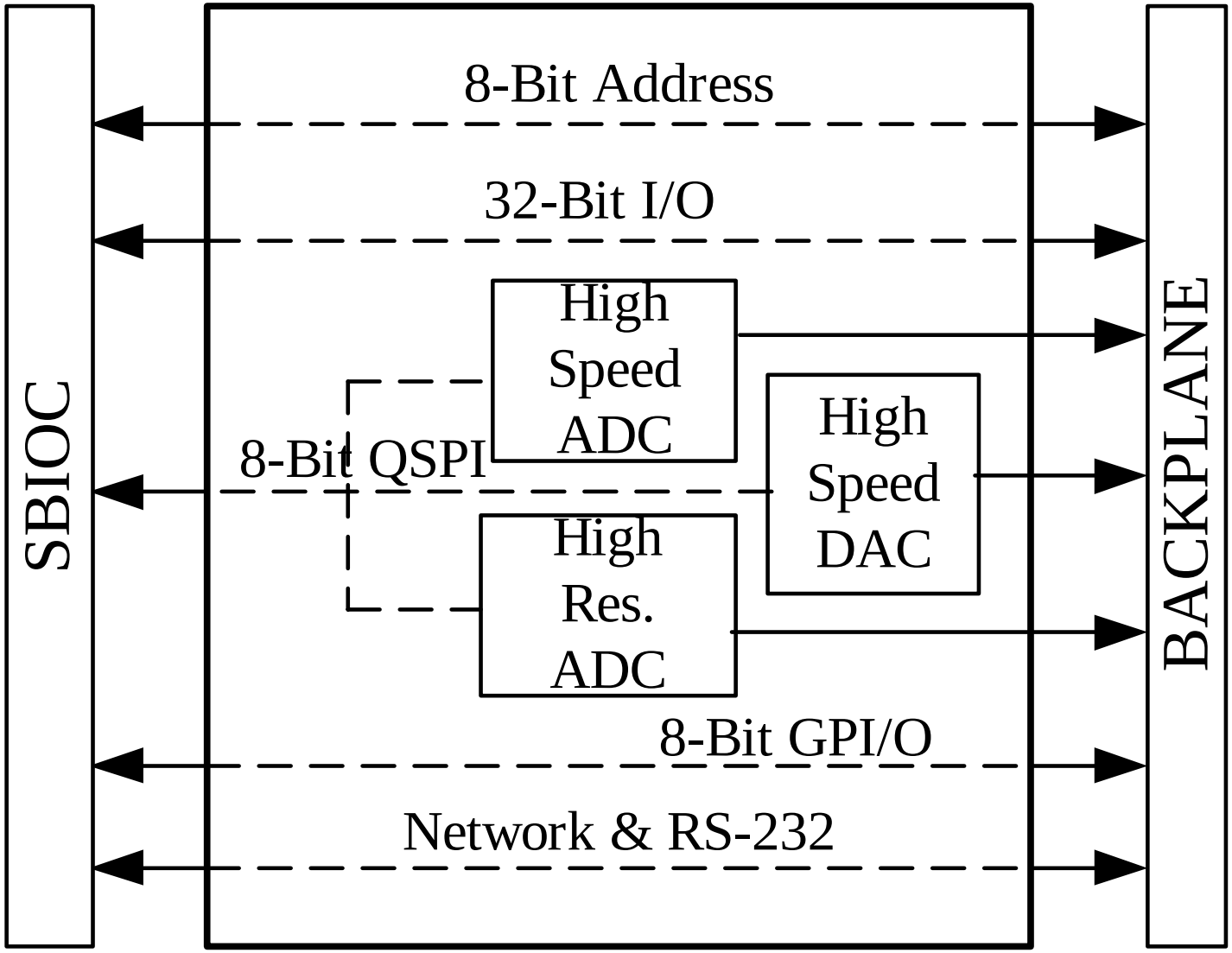
New Version BPM with the SBIOC



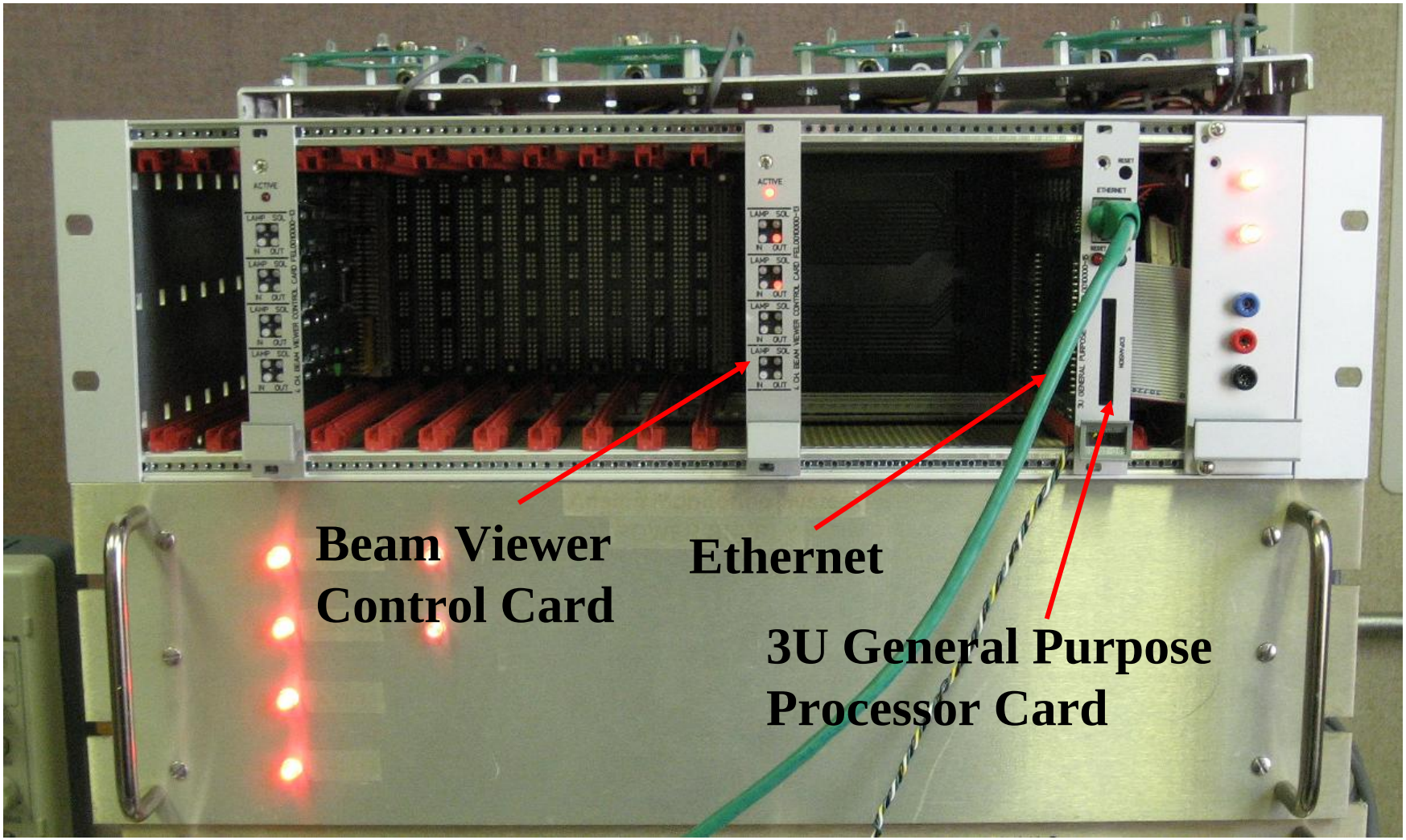
3U General Purpose Processor Card (GPPC)

- A Carrier board that provides a bridge between the SBIOC and other crates
- Pin-pin compatible with existing CAN bus Digital Signal Processor (DSP) card.
- Use resources from the SBIOC
- 96-Pin Backplane
- For Beam Viewer Controls, GC magnet power supply, HVPS Controller, Temperature monitoring system, Vacuum instruments.

Block Diagram of the 3U GPPC



3U GPPC for Beam Viewer Control



Software Applications

- RTEMS (4.7) Chosen as the real-time operating system for SBIOC
- EPICS R3.14 as the development toolkits
- Developed the EPICS applications for BPM, 3U GPPC, Beam Viewer control
- Use Software Quartus II to program the codes for the FPGA

Summary & Conclusions

- The first version of BPM based on embedded IOC had been running on FEL. It is reliable, and easily maintained.
- Setup the software
  - EPICS, RTEMS, Device support, Database
- Designed the Single Board IOC
- ColdFire uC5282 processor is a ideal choice for the embedded IOC
- Use RTEMS as the real-time operating system
- By distributing the IOC on front-end I/O devices, dramatically cut the cost of expensive cables.
- It is a novel configuration to use FPGA+uC5282+RTEMS for FEL diagnostics and controls upgrading

Acknowledgement

- Thanks
  - Eric Norum in Argonne National Lab for providing RTEMS tools and installation instructions.
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