Digital Phase Control System for SSRF LINAC

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Main Mile Stone of SSRF

- The ground breaking has launched in Dec.25, 2004
- Dec. 2004 ~ Apr. 2007: Building construction
- Dec. 2004 ~ Mar. 2008: Machine manufacture and assembly
- May. 2007 start to Commissioning LINAC with success
- Oct.2007 Preliminary commissioning Booster with sucess

As the third synchrotron light source, SSRF contains

1. 150MeV LINAC,
2. 3.5GeV booster
3. 3.5GeV storage ring.

Grounding breaking of SSRF Dec.25 2004

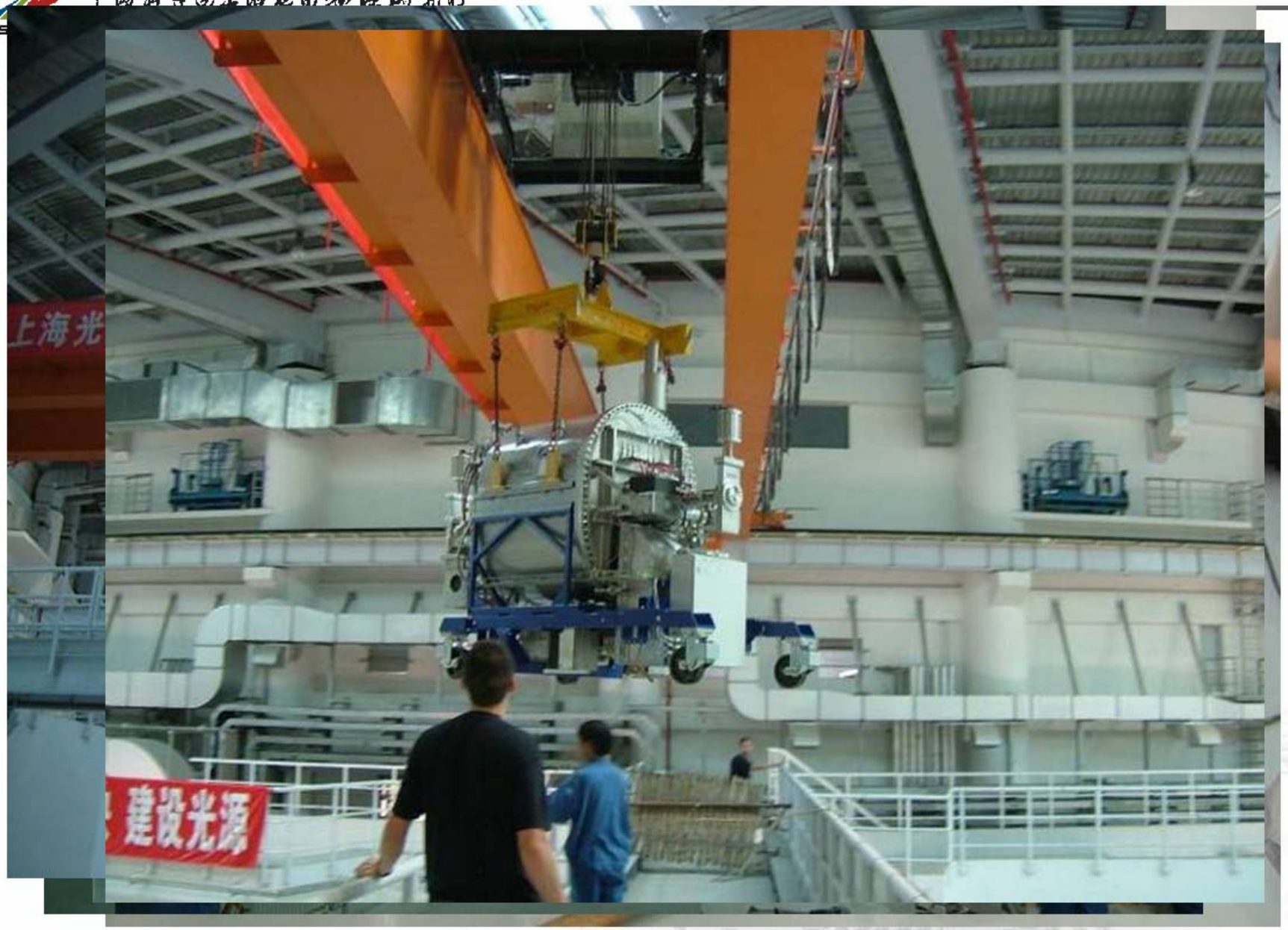
OCT.2004

2005

Dec. 2004 ~ Apr. 2007 Building construction

严格工艺 持续改进 崇尚科学 六求规范
上海建工 第七建

上海光源储存环设备安装正式启动
上海建工安装公司


上海光
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SCG
上海建工 第七建筑
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Linac Commissioning Finished

Linac Commissioning Finished

Linac Commissioning Finished

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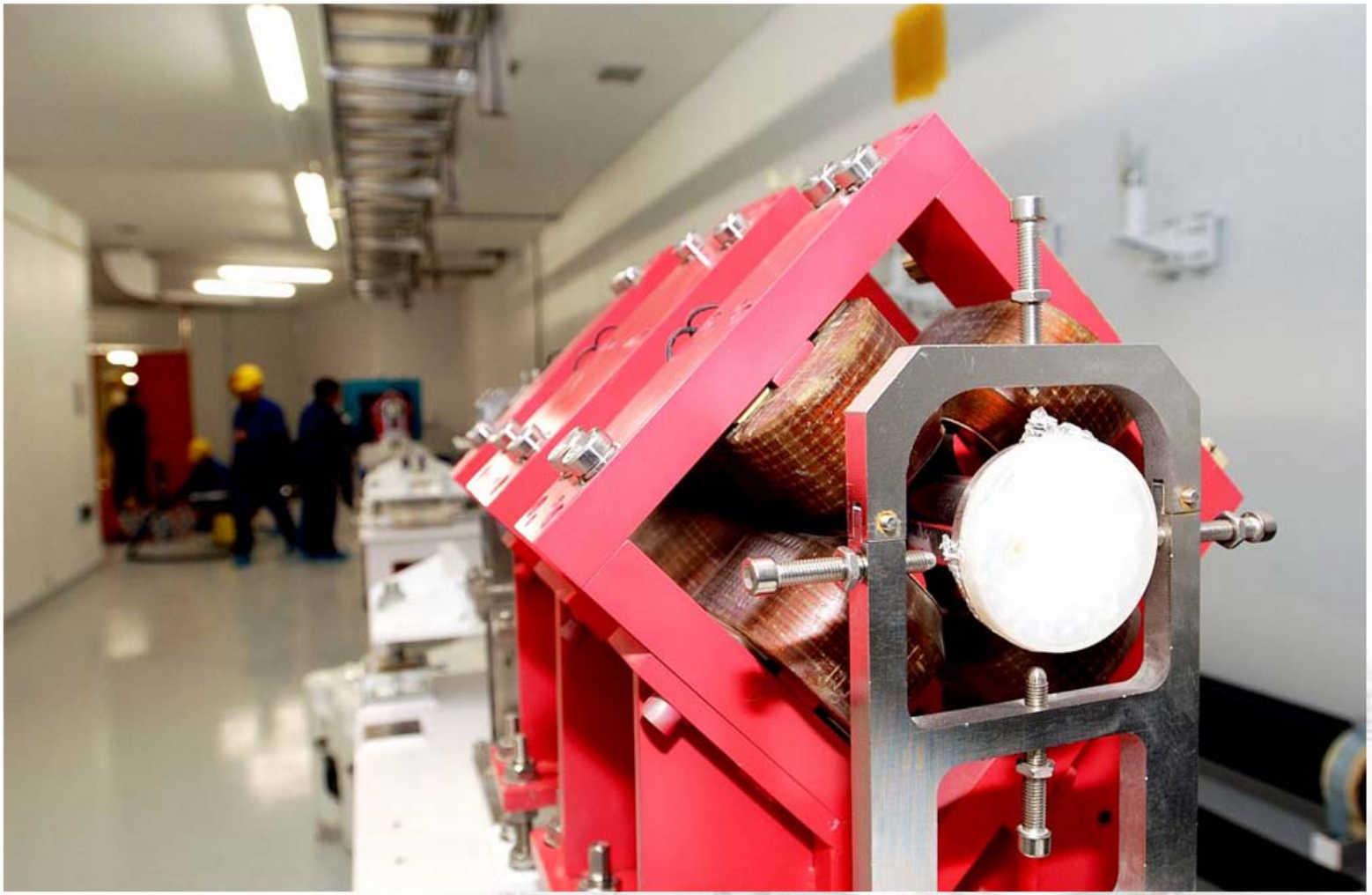
Linac Commissioning Finished



Linac Commissioning Finished

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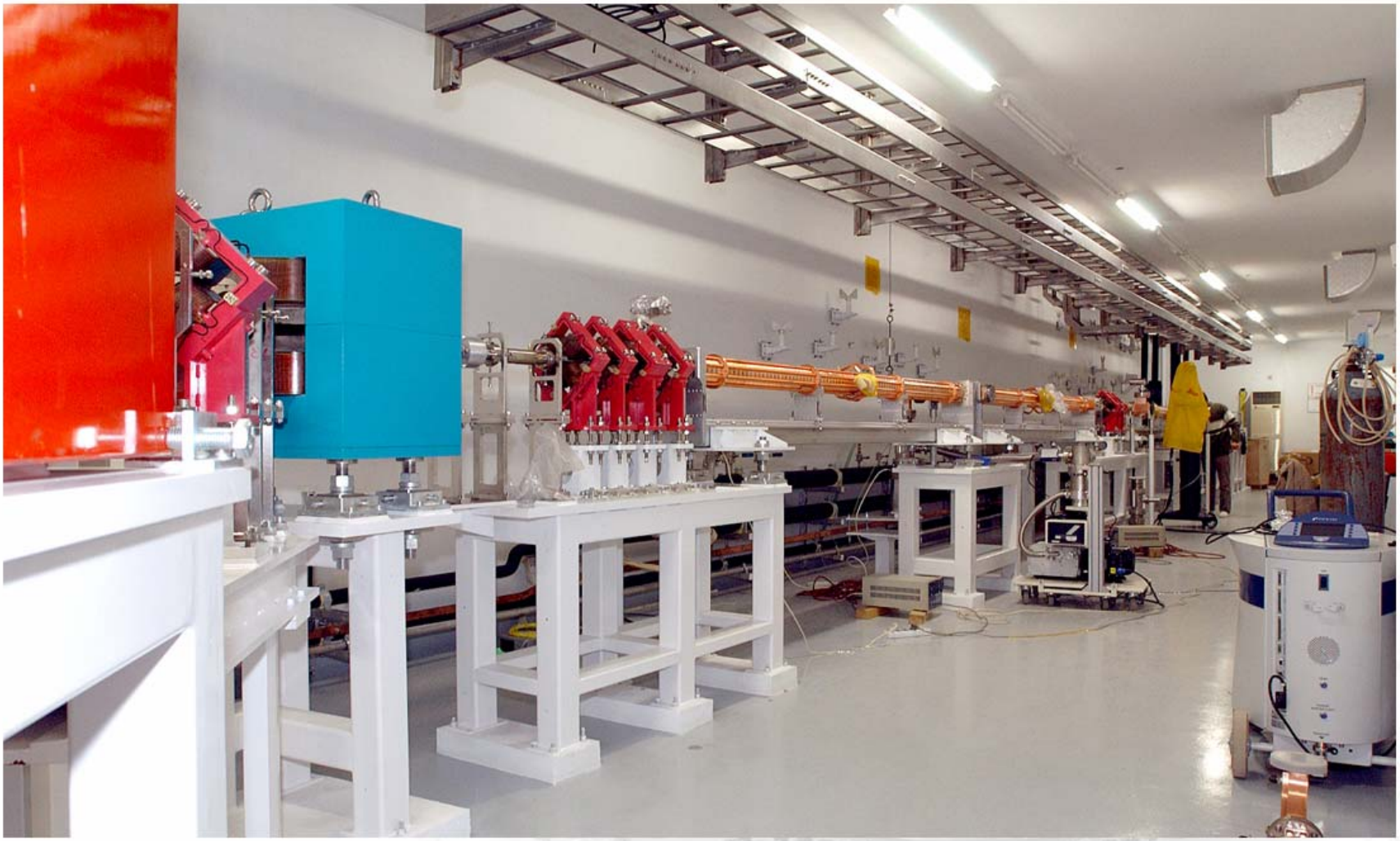
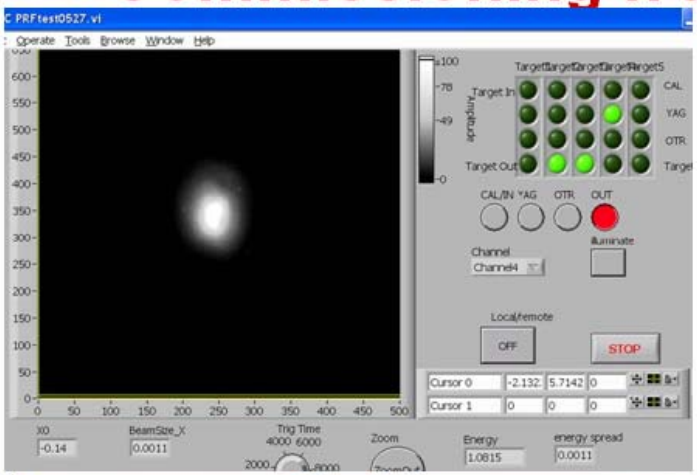


Linac Commissioning Finished

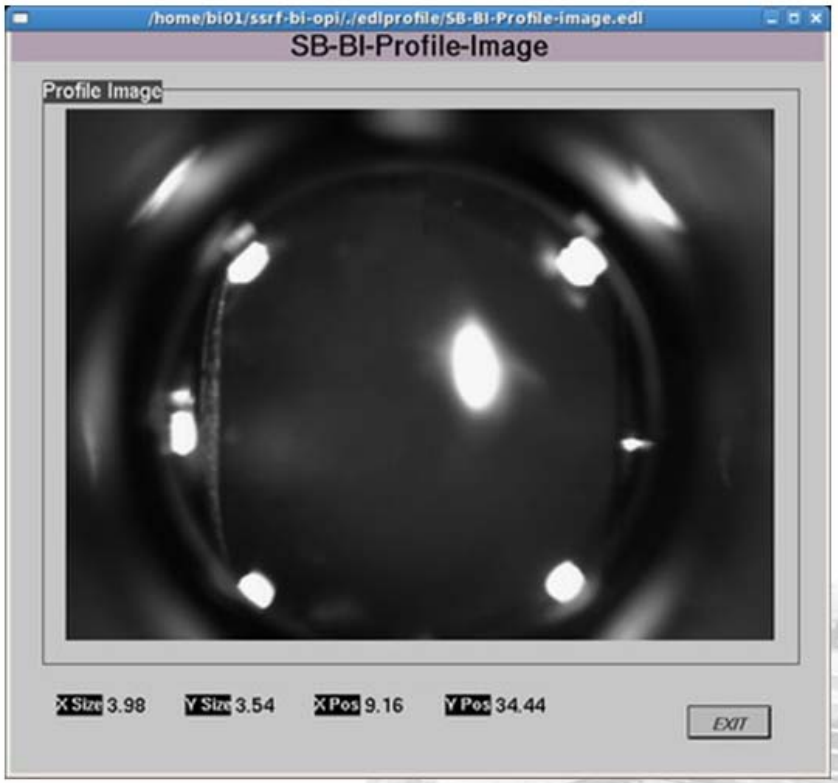
Commissioning from May 2007 & Operation



Booster have completed pre-commissioning

Booster, 2007-6

Milestone of commissioning Booster



- Sep.30 8:30 Start to commissioning
- Sep.30 21:58 Beam inject Booster

Oct.1 17:02 multi turns in Booster without RF

Oct. 3 4:00 AM Stored beam with RF

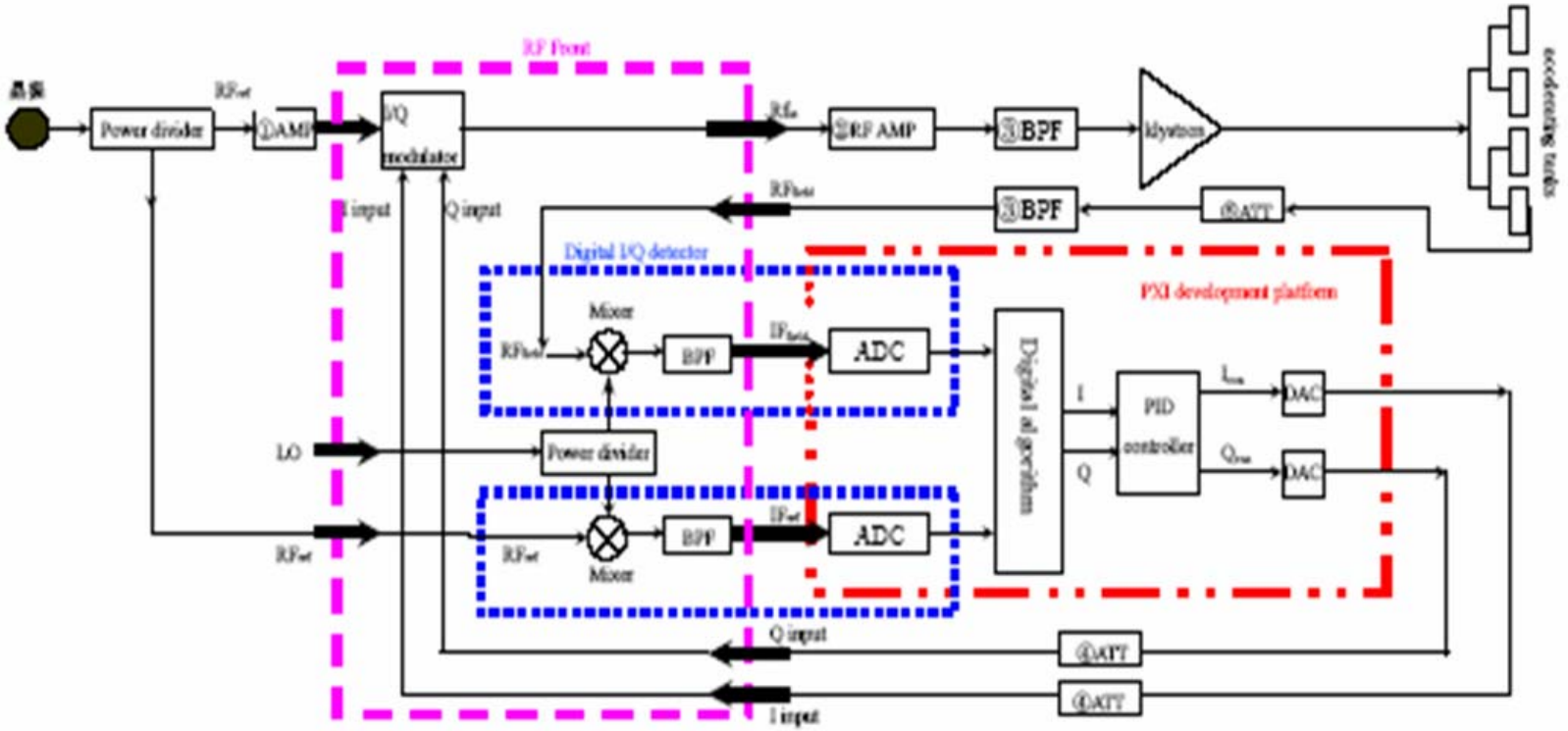
Requirement to phasing system

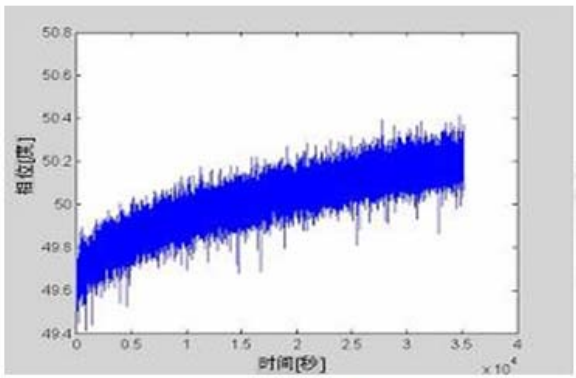
- **First Step: long term phase control**

  Keep stable beam inject from LINAC to Booster with stable phasing in long term operation . This step got success already.

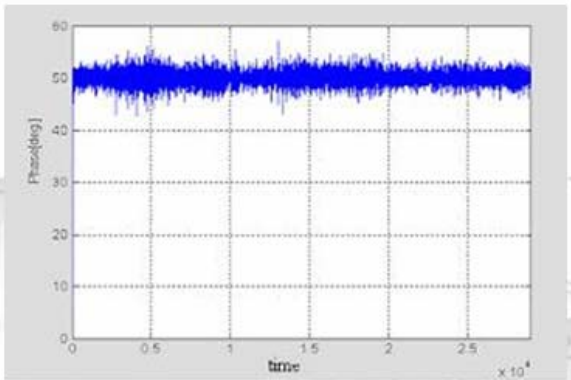
- **Second Step : (during inter-pulse)**

  To keep stable phasing in the Pulse decrease energy spread

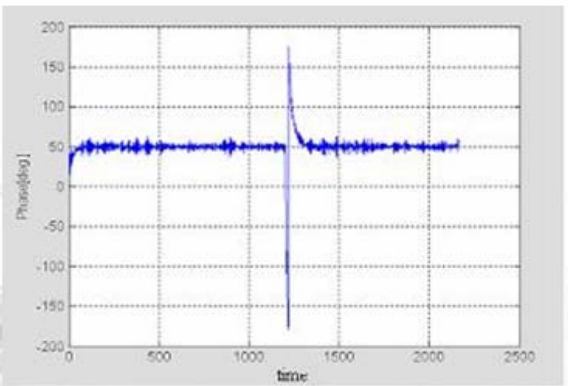




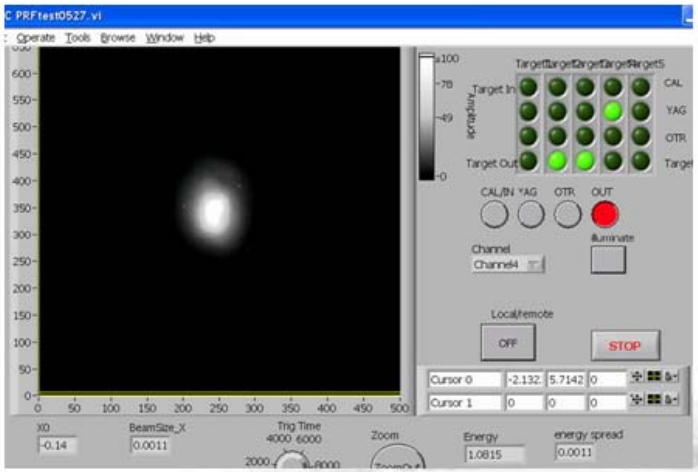
Turn off



Turn on



Cutting noise

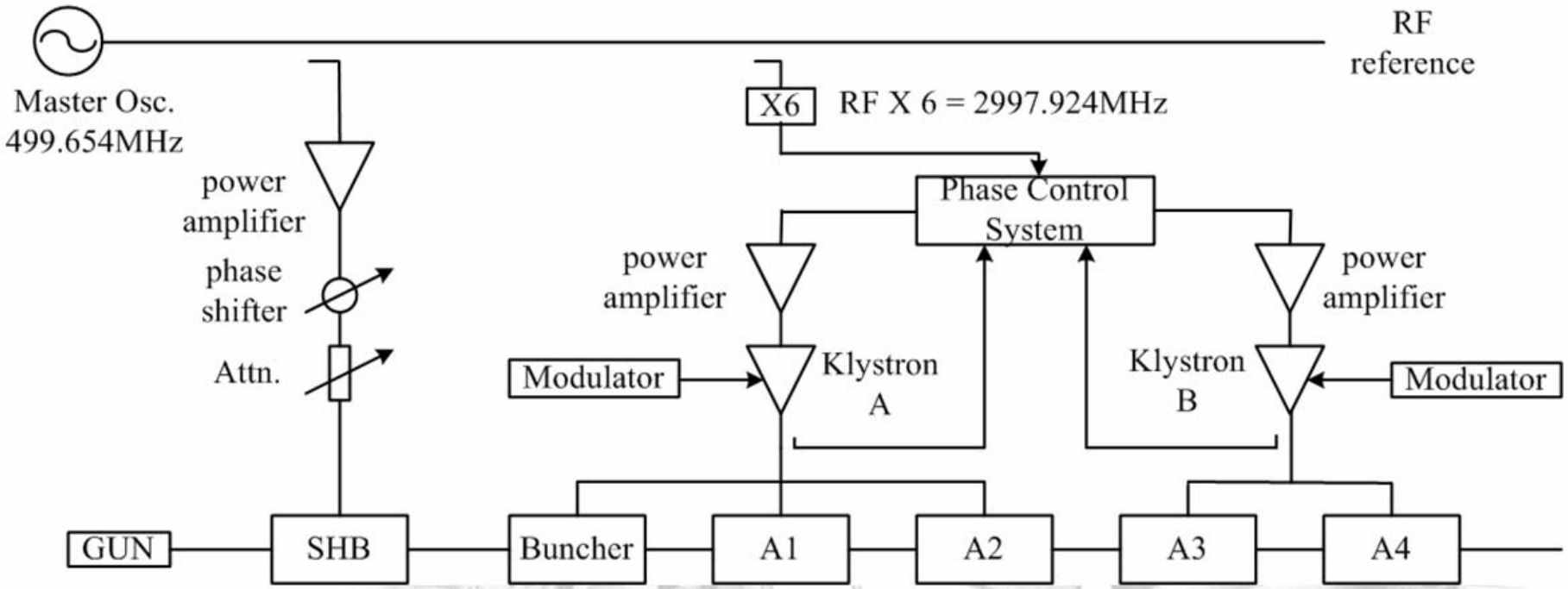


After turn on phasing system ,we got very stable beam inject into Booster .

Parameters of LIANC:

Energy（MeV）	100
Charge	
Single Bunch	1nC
Multi-bunch	100~300 ns, 3~5nC
Energy Stability	0.5%
Energy Spread	0.5% (rms)
Normalized Emittance	100 mm·mrad
RF frequency（MHz）	2998
Accelerator tube	4

Layout of LINAC:



RF phase stability:

- When SSRF is operated in top-up mode, LINAC will work in multi-bunch mode.

- In order to improve LINAC performance in multi-bunch mode, interpulse phase stability of klystron output should be considered.

- Base on the LINAC design, the requirement of RF phase stability is to control interpulse phase shift of klystron output within ± 1 degree. So phase control system is implemented in SSRF LINAC.

The design philosophy:

- Implement passive coaxial RF component to down-convert RF signal to IF signal, and up-convert IF signal to RF signal.

- Implement commercial products for ADC, DAC and clock management modules.

- Implement digital I/Q demodulation as phase detecting algorithm, and digital I/Q modulation as phase shifter.

The design philosophy:

- Implement feed-forward control to compensate interpulse phase shift of klystron forward signal.
- Implement FPGA for signal processing and control.
- Implement embedded computer and real-time operation system for iterative algorithm calculation in feed-forward control.

Layout of phase control system:

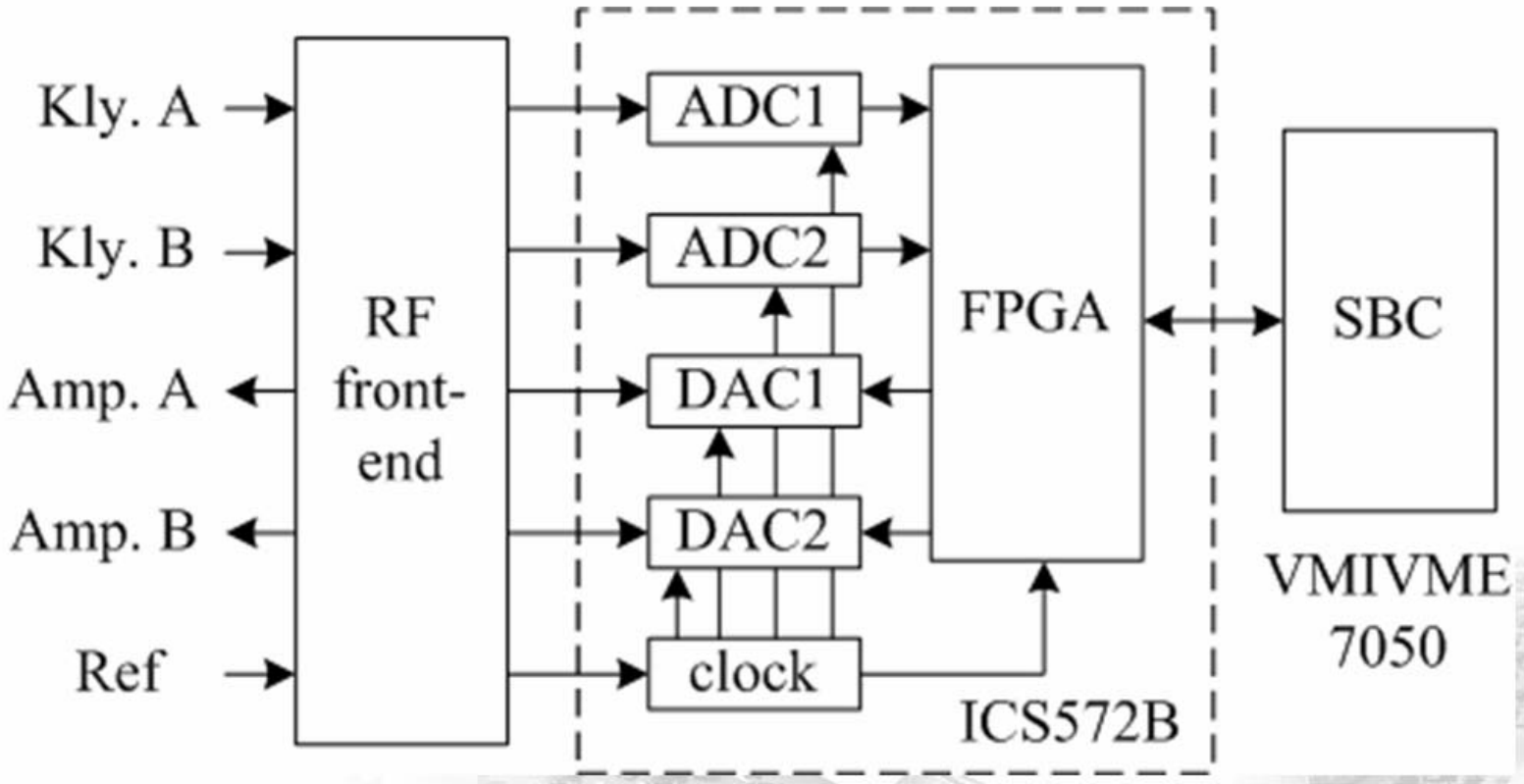
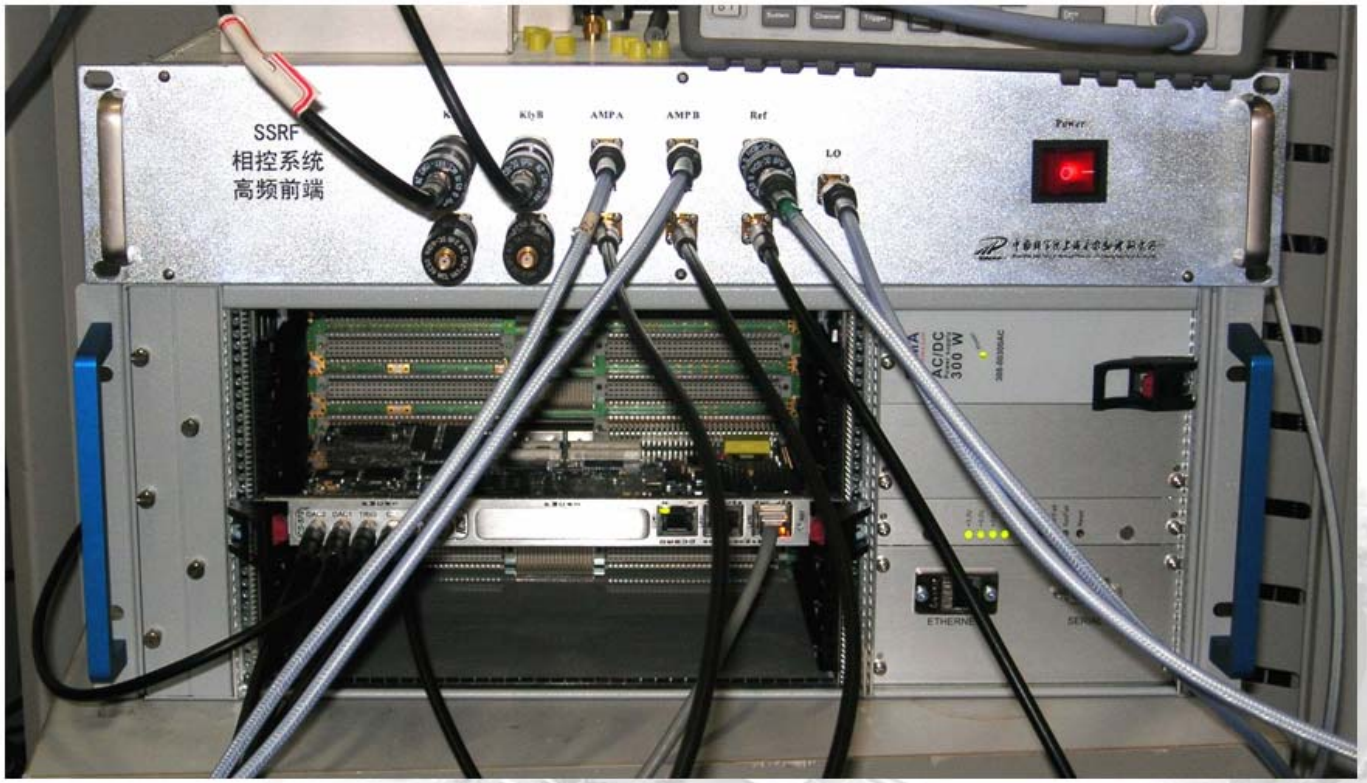
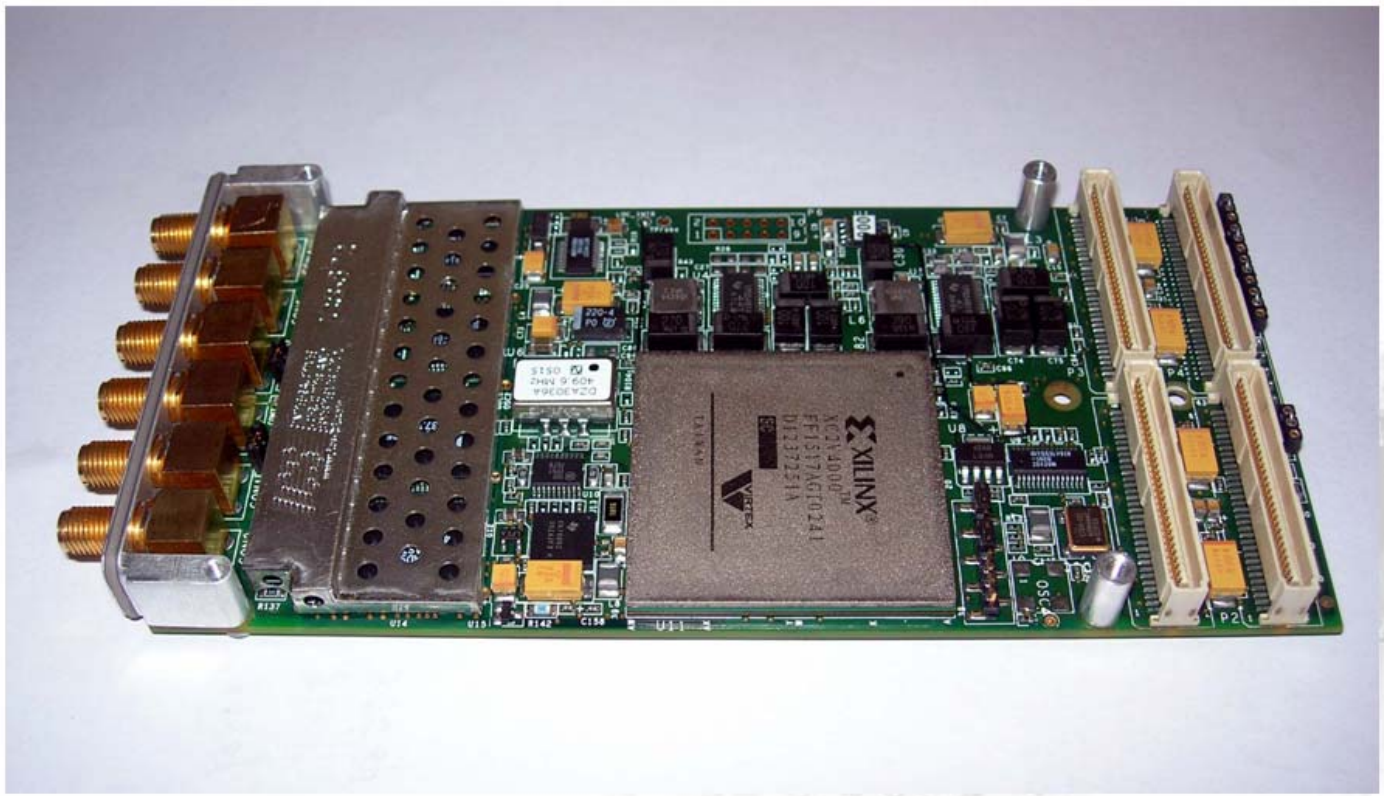


Photo of phase control system:



Components in phase control system:

- ICS572B: PMC module; two ADCs, two DACs, clock management and FPGA.

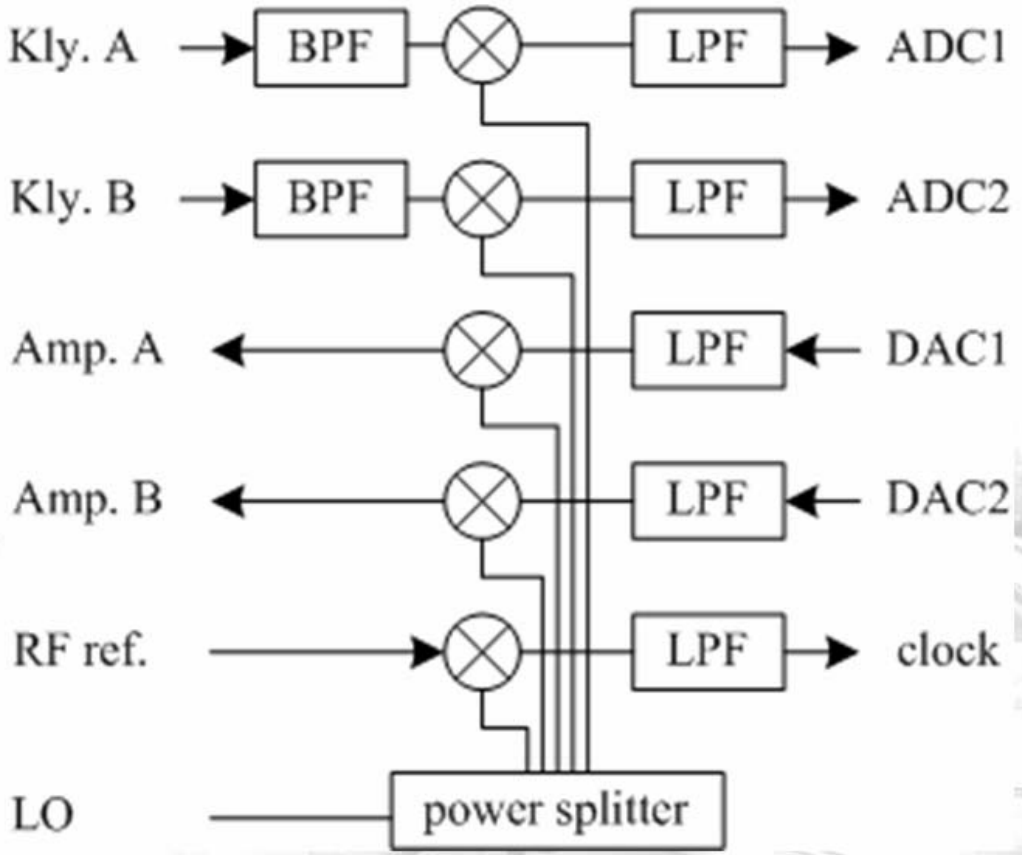


Components in phase control system:

- GE VMIVME 7050: VME single board computer, used for iterative algorithm calculation.

- RF front-end.

Layout of RF front-end:



RF front-end:

- Two klystrons forward signal is down-converted to IF signal (25.6MHz), sampled by two ADCs respectively.

- Two DACs outputs are up-converted to RF signal (2997.924MHz), used as power amplifier input.

- RF reference signal (2997.924MHz) is down-converted to IF signal (25.6MHz), used as input signal for clock management module in ICS572B.

Clock:

- In order to satisfy digital I/Q modulation and demodulation requirement, it is required for sampling clock to be synchronized with reference IF signal.

- In conventional design, RF distribution system will provide AD/DA sampling clock that is synchronized with reference IF signal.

- In our design, clock management module will provide this function, the complexity of RF distribution system is reduced.

Clock:

- Clock management module in ICS572B: TI CDC7005; 409.6MHz VCXO; passive filter for PLL.

- Generating 5 clocks which are synchronized with reference IF signal (clock management module input signal).

Two ADC sampling clocks (102.4MHz, four times of input signal);

Two DAC sampling clocks (204.8MHz, eight times of input signal);

One FPGA clock (25.6MHz), used for ADC sampling data alignment.

ADC:

- ICS572B includes two 14-bit ADCs (AD6645), and sampling frequency is up to 102.4MHz.
- ADC sampling frequency is 102.4MHz in phase control system, and work in simultaneous mode.
- Data from two ADCs directly send to FPGA, digital I/Q demodulation is done by FPGA.
- Latency for ADC is about 40ns.

DAC:

- ICS572B includes two 14-bit DACs (AD9857), and sampling frequency is up to 204.8MHz.
- DAC sampling frequency is 204.8MHz in phase control system.
- DAC contains digital up-converter, and frequency-tuning value of DDS is set to 1/8 in phase control system.
- Two DACs up-convert I/Q data to IF signal (25.6MHz).
- FPGA directly send I/Q data to two DACs simultaneously.
- Latency for DAC is about 510ns.

Signal processing:

- Signal processing includes digital I/Q demodulation, digital I/Q modulation, I/Q to phase conversion, phase to I/Q conversion, and FIR filter.

- Digital I/Q modulation is contained in DAC; additional parts are realized in FPGA.

- Phase detector (I/Q demodulation) and phase shifter (I/Q modulation) are all realized in digital signal processing mode, so the performance of noise rejection is improved.

Control:

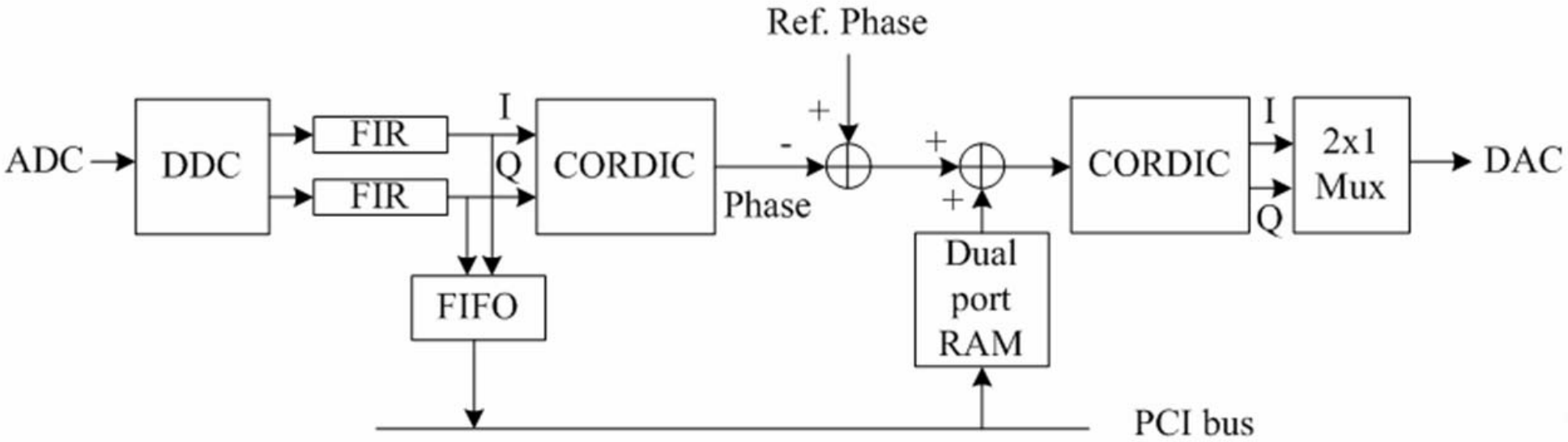
- Control includes feed-forward control and iterative algorithm calculation.
- Feed-forward control is realized in FPGA, and iterative algorithm calculation is done in software.

FPGA:

- FPGA is the key for digital phase control system.
- ICS572B contains a Xilinx Virtex-II FPGA (XC2V4000).
- In addition to parts of signal processing & control, FPGA contains data format conversion for DAC input, some registers and memory for data exchanging with software.
- Close-loop period of phase control system is about 40ns, so the data stream frequency of all parts in FPGA must be more than 25.6MHz.

FPGA:

- FPGA contains two identical channels that work simultaneously, one channel controls one klystron forward signal's phase respectively.



Layout of one channel in FPGA

FPGA:

- Digital I/Q demodulation: ADC sampling clock is four times of input signal, so digital I/Q can be attained by

$$\begin{cases} I(n) = [x(4n-3) - x(4n-1)]/2 \\ Q(n) = [x(4n) - x(4n-2)]/2 \end{cases}$$

FPGA clock is used to align four successive sampling data to generate a couple of I/Q data.

- FIR filters: 8 taps; used to compensate phase shift between I/Q caused by digital I/Q demodulation algorithm.

FPGA:

- CORDIC: 12 taps; used to I/Q to phase conversion and phase to I/Q conversion; the phase conversion accuracy is better than 0.1 degree.

- Feed-forward control: the phase difference is attained by comparing reference phase with sampled phase data; the phase of feed-forward control is attained by add phase difference with feed-forward phase vector in dual port RAM.

FPGA:

- 2x1 multiplexer: used to DAC input data conversion; convert parallel I/Q data to interleaved data stream.

- The latency of FPGA: 1 period for DDC; 1 period for FIR; 6 periods for CORDIC; 2 periods for feed-forward control; 1 period for 2x1 multiplexer.

- The total latency of phase control system is about 1us.

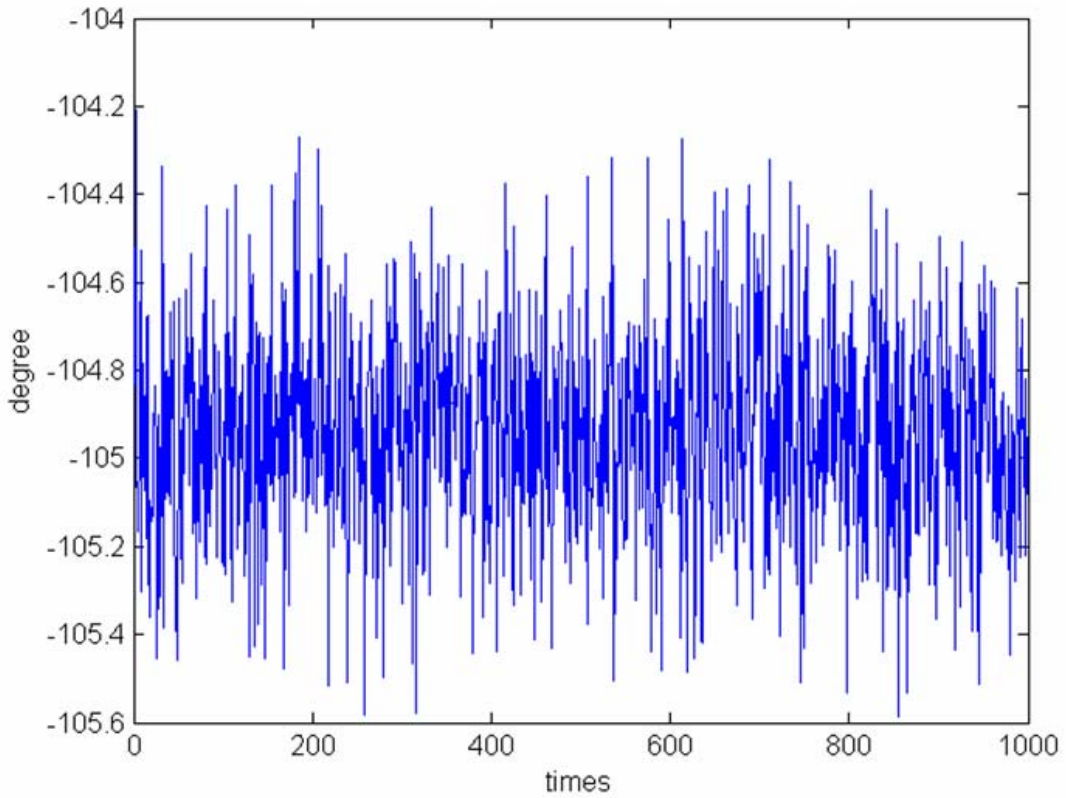
Software:

- Iterative algorithm calculation: under VxWorks operation system.

- At the end of one pulse, software is triggered by interrupt to read FIFO, which stores all I/Q data in the pulse.

- After iterative algorithm calculation, feed-forward phase vector is written to dual port RAM in FPGA.

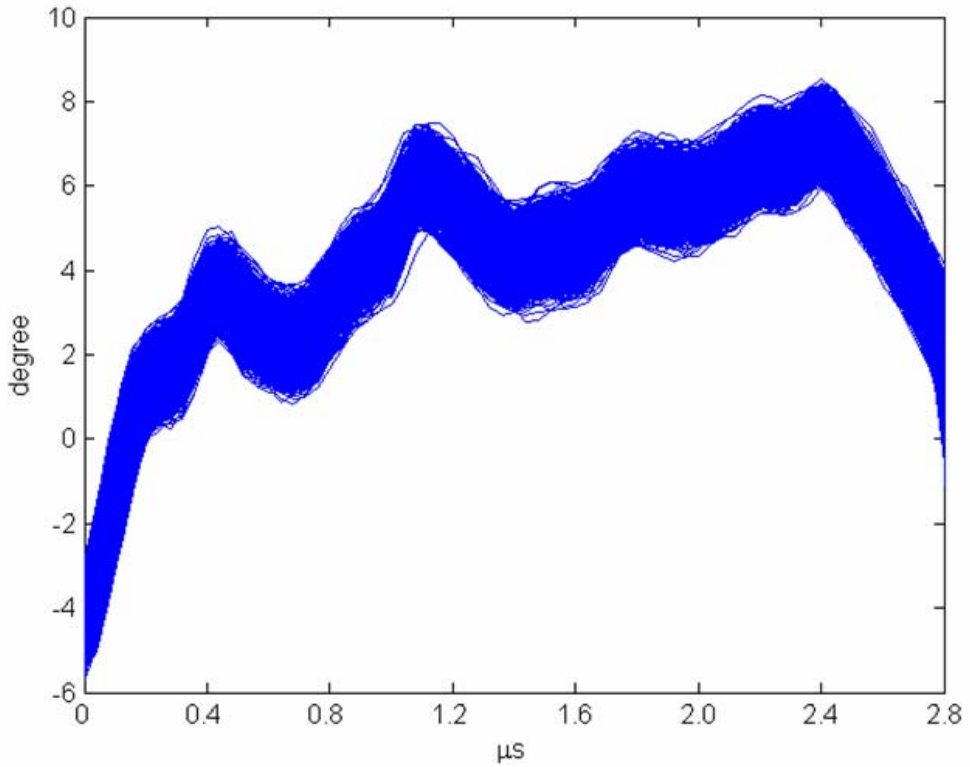
Preliminary Test:



The background noise of phase control system

- Tested in LINAC operation condition.
- RF reference signal is connected both Kly. A port and RF ref. Port in RF front-end.
- Data is acquired by measuring one point phase (2us after trigger rising edge) 1000 times.
- The background phase noise is within ± 0.6 degree.

Preliminary Test:



Interpulse phase of klystron forward signal

- Set phase control system in open loop mode.
- Data is acquired by measuring interpulse phase and amplitude 1000 times.
- Interpulse phase shift is more than 10 degree, phase control system is essential.

Conclusion:

- **The open-loop test indicated digital phase control system has ability to acquire interpulse phase of klystron output, so the feasibility of our design is proved.**

- **In the background noise test, noise of phase detector is within ±0.6 degree. Because ADC and DAC's clock source is same, phase noise of close-loop is within 0.1degree (caused by CORDIC). So the total phase noise will be within ±1 degree; the performance of close-loop could be foreseeable.**

Conclusion:

- **Due to the present commissioning stage for SSRF, there is no enough machine study time for LINAC. The close-loop of phase control system will be further tested in future.**
- **This is a helpful reference design for phase control system in next XFEL or CSNS.**
- **Next step will use feed forward method to keep flat phasing in pulse ,then to close loop to reach our goal.**

Thanks for your attention!

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