



The CERN LHC central timing

A vertical slice

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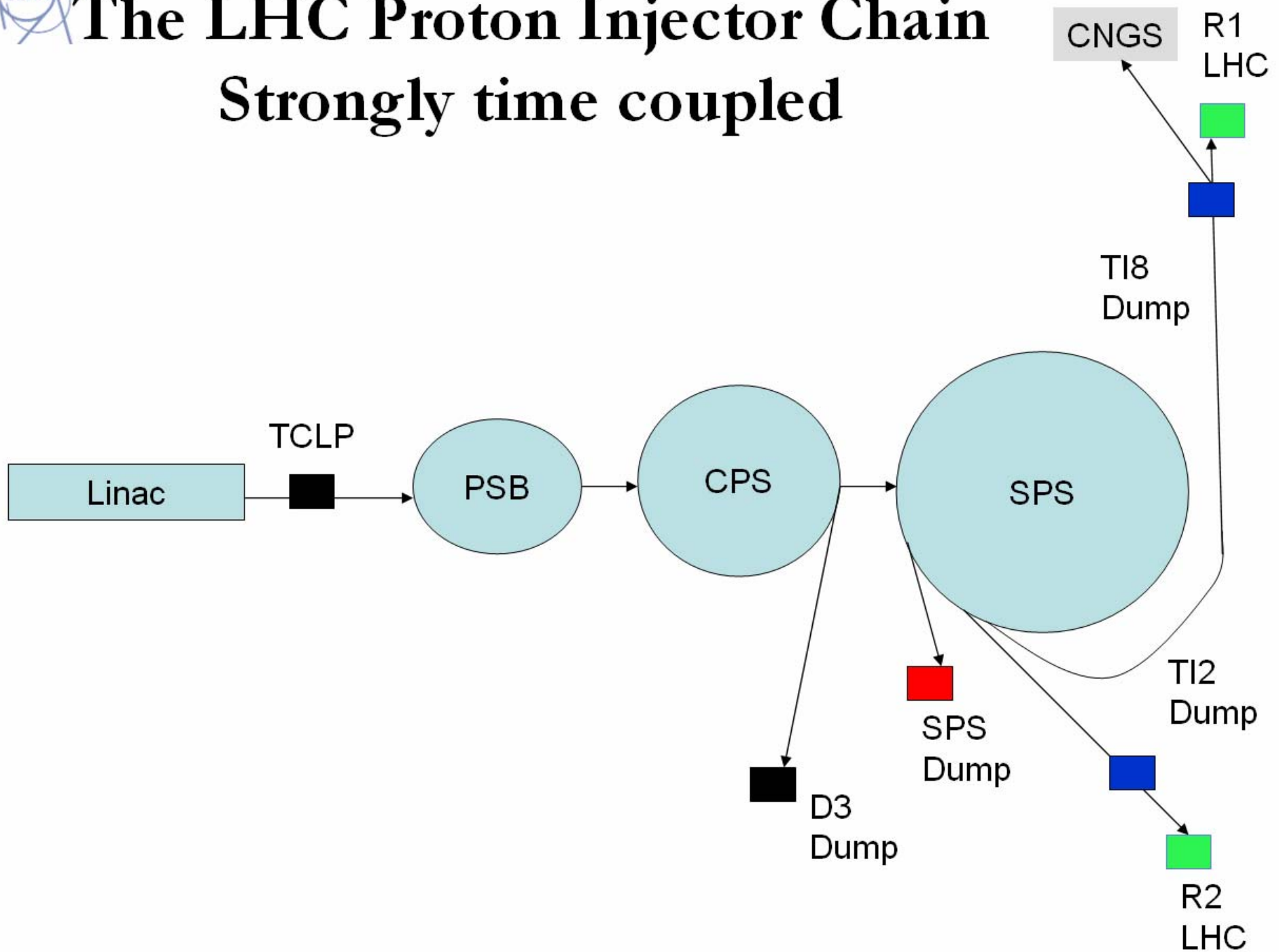
Talk layout

- [LHC Injector Chain Timing](#)
- Timing Distribution Overview
- Central Timing Overview
- Reflective Memory
- UTC Time and GPS
- The Multitask Timing Generator
- The Controls Timing Receiver Module
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- LHC Software Architecture and Event Tables



The LHC Proton Injector Chain

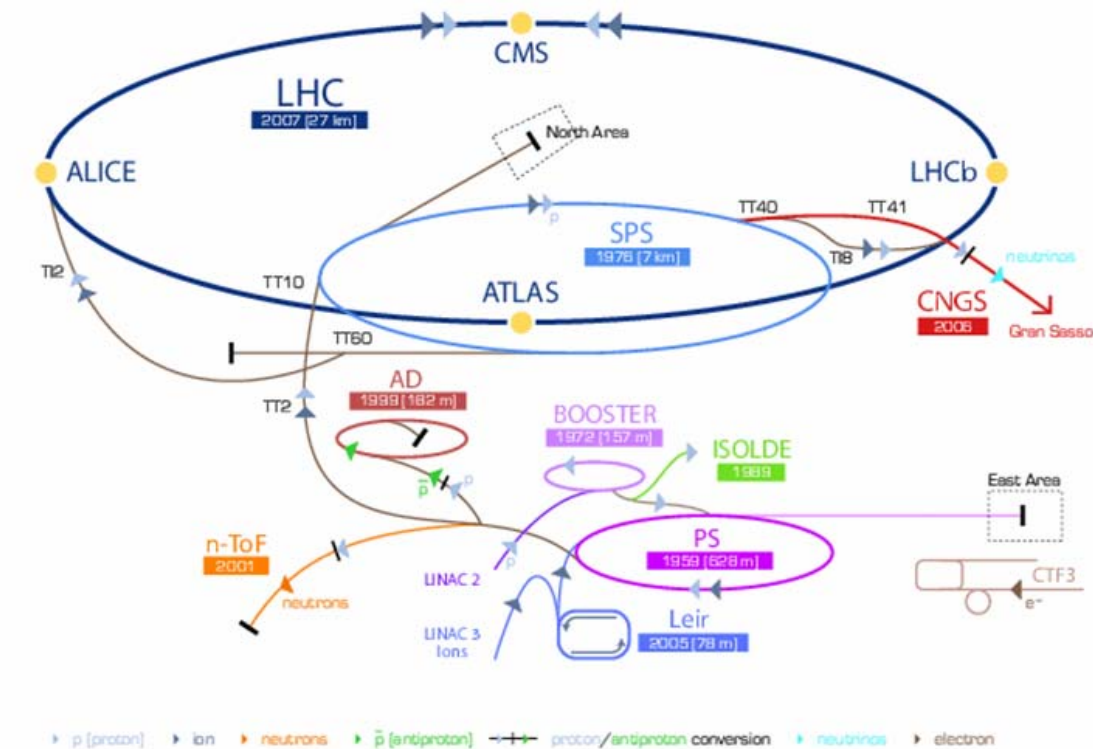
Strongly time coupled





CERN accelerator network sequenced by central timing generator

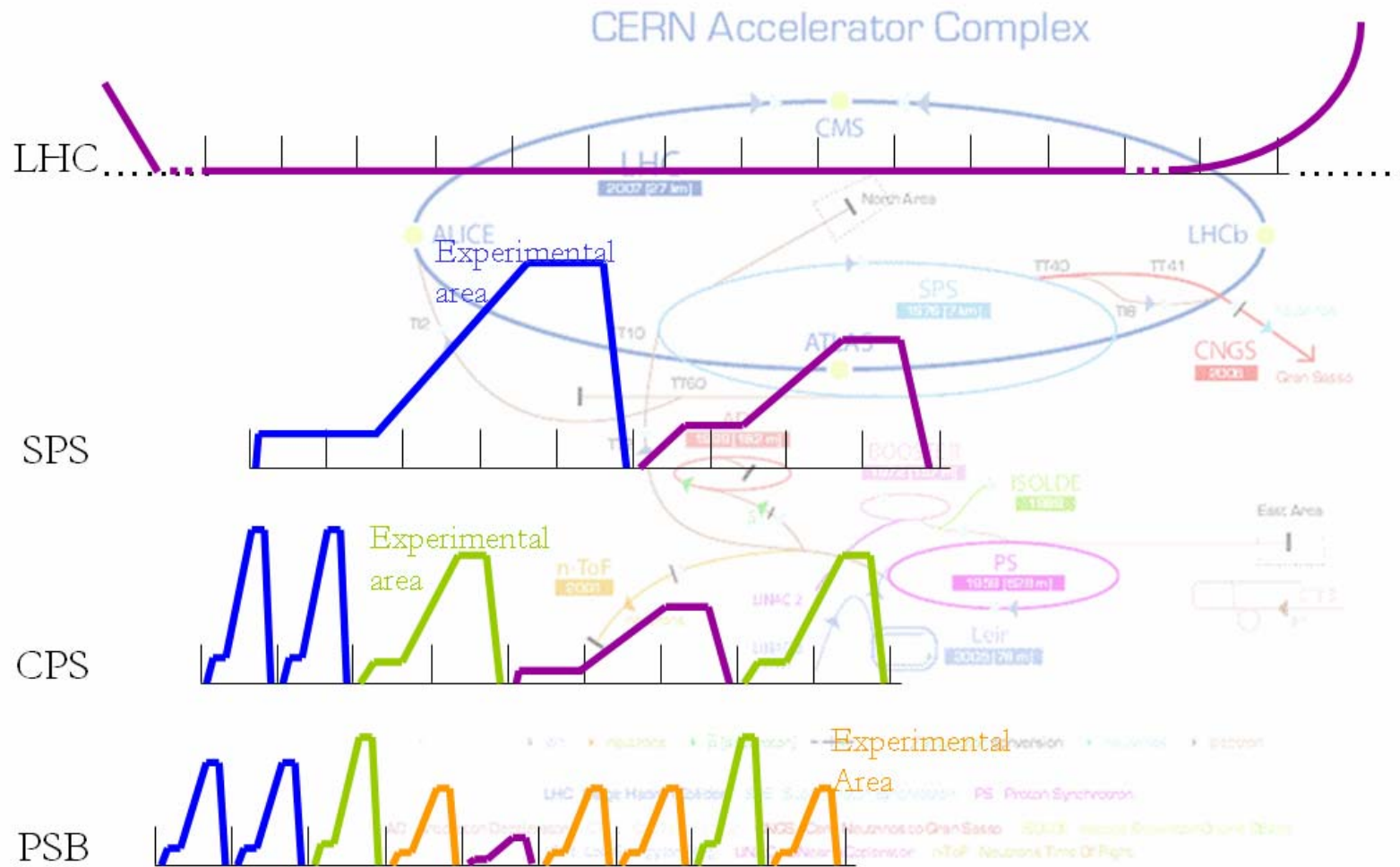
CERN Accelerator Complex



LHC Large Hadron Collider SPS Super Proton Synchrotron PS Proton Synchrotron
AD Antiproton Decelerator CTF3 Clic Test Facility CNGS Cern Neutrinos to Gran Sasso ISOLDE Isotope Separator OnLine Device
LEIR Low Energy Ion Ring LINAC LINear Accelerator n-ToF Neutrons Time Of Flight

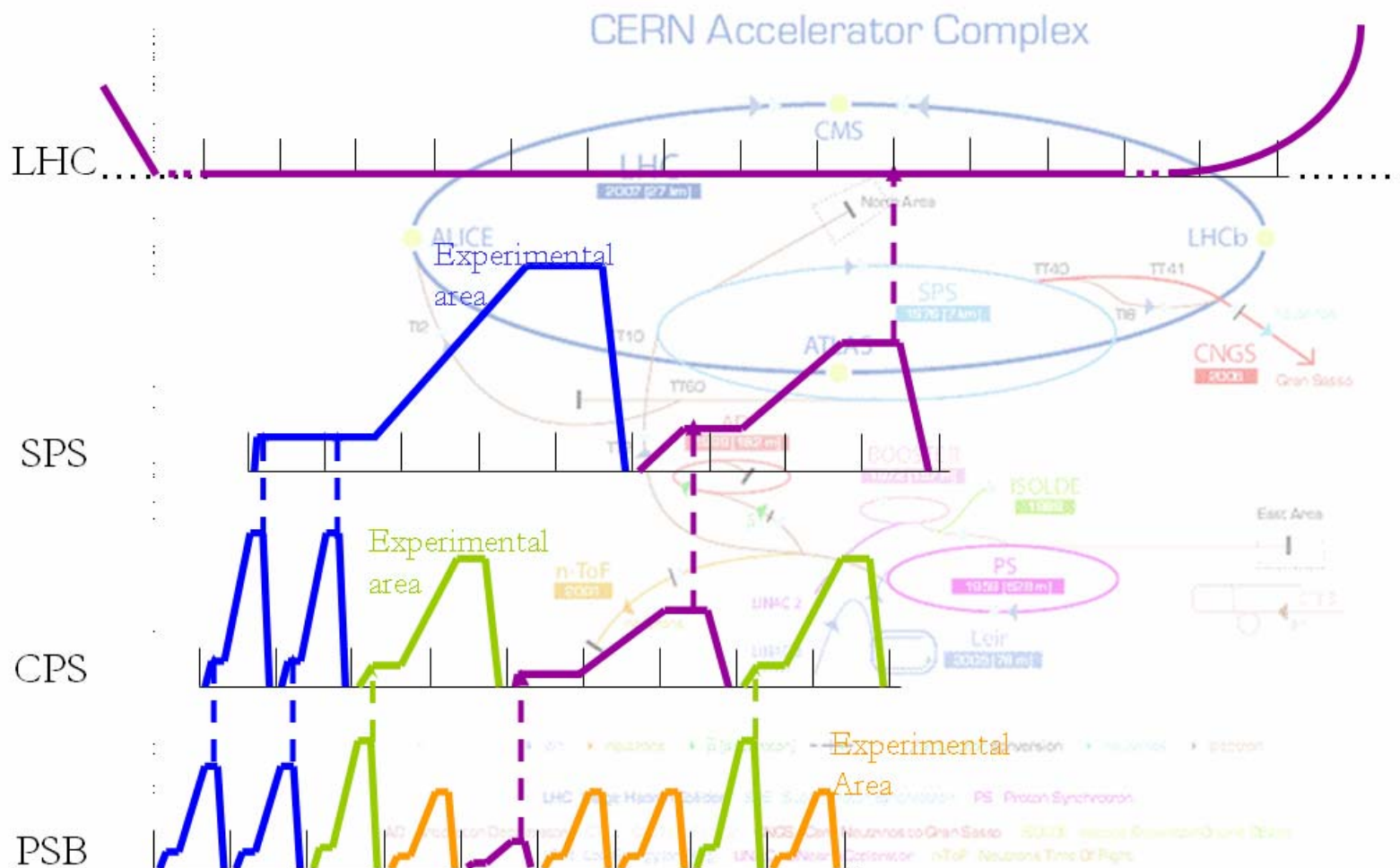


CERN accelerator network sequenced by central timing generator



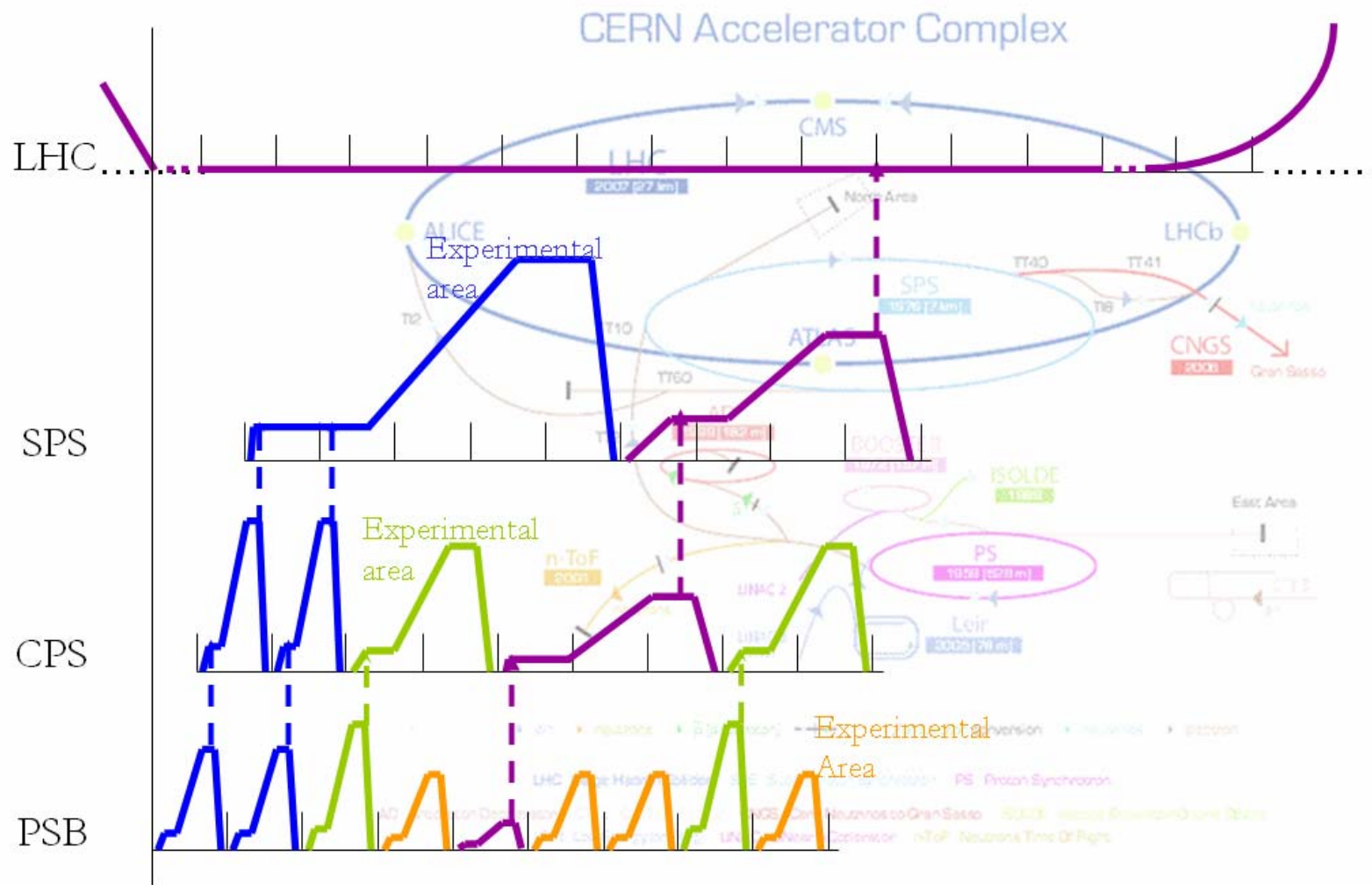


CERN accelerator network sequenced by central timing generator





CERN accelerator network sequenced by central timing generator





CBCM Sequence Manager

BEAM COORDINATION DIAGRAM EDITOR: Edit BCD /scrubbing SPS/

File Edit R.Checker Tools Specialist Help

Type

Description Rule violations Selection

General description

Name **scrubbing SPS**

Desc.

Created Mon Jun 02 07:02:20 Updated Wed Jun 11 13:54:16

Other informations

Bcd length $\uparrow\uparrow$ 20 $\downarrow\downarrow$

| | | | | | | | | | | | | | | | | | | | | | |
|---|-------|--------|--------|------|---------|------|------|---------|------|------|---------|------|--------|---------|------|--------|-------|------|------|-------|------|
| S | < 4 > | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | | |
| P | | | | | LHCTEST | | | LHCTEST | | | LHCTEST | | | LHCTEST | | | ZERO | ZERO | | | |
| S | | | | | LHCTEST | | | LHCTEST | | | LHCTEST | | | LHCTEST | | | ZERO | ZERO | | | |
| C | < 1 > | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| P | | | | | LHC | | | LHC | | | LHC | | | LHC | | | EASTB | | TOF | EASTB | |
| S | | | | | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO |
| P | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | | | |
| S | LHC | TSTLHC | ISOGPS | LHC | TSTLHC | ZERO | LHC | TSTLHC | ZERO | LHC | TSTLHC | ZERO | EASTB | ISOGPS | TOF | EASTB | ZERO | TOF | | | |
| B | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ZERO | ISOGPS | ZERO | ZERO | ISOGPS | ZERO | ZERO | | | |

Fault: Error detected. Can't strip Bcd for machine SPS Exception: cern.ps.cbcm.srvapi.SrvException: Cbcm Server Exception: Can't get parameter SPS.FILLHOLES; nested exception is: Cbcm Context Excepti

11/Jun/2003 13:54 User CPS.LABO.SUPERUSER RES PSPC8476:BCD editor:LABO.SUPERUSER... RChecker





The LHC Beam

The LHC timing is only coupled by extraction

LHC Injection plateaux

start-ramp event

Injection

Injection

LSA Beam request:
RF bucket
Ring
CPS batches

Extraction

Extraction

Extraction
Forewarning

Extraction
Forewarning

SPS injection plateaux

SPS Cycle for the LHC

CPS Batch 1

CPS Batch 2

CPS Batch 3

CPS Batch 4

PSB1 PSB1

PSB2 PSB2

PSB3 PSB3

PSB4 PSB4





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Timing Distribution Overview

- RS485 drop nets distribute timing around the CERN accelerator complex
- Long distance transmission over optical fibers
- One timing network for each accelerator
- Hundreds/Thousands of timing receiver modules distributed around the complex
- One timing generator drives one timing network



Timing Frames

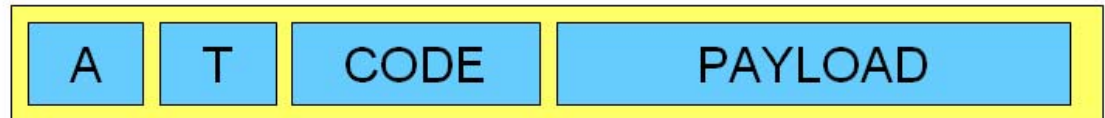
Millisecond

Millisecond



- Timing frames are Manchester encoded at 500kbit using a 1MHz clock.
- Each frame carries 32 data bits, parity, start and stop bits.
- One frame transmitted each 125 μ s, 8 per millisecond.
- The frame data is broken into bit fields

- 4 Bits Accelerator [A]
- 4 Bits frame Type [T]
- 8 Bits Code [CODE]
- 16 Bits Payload [PAYLOAD]



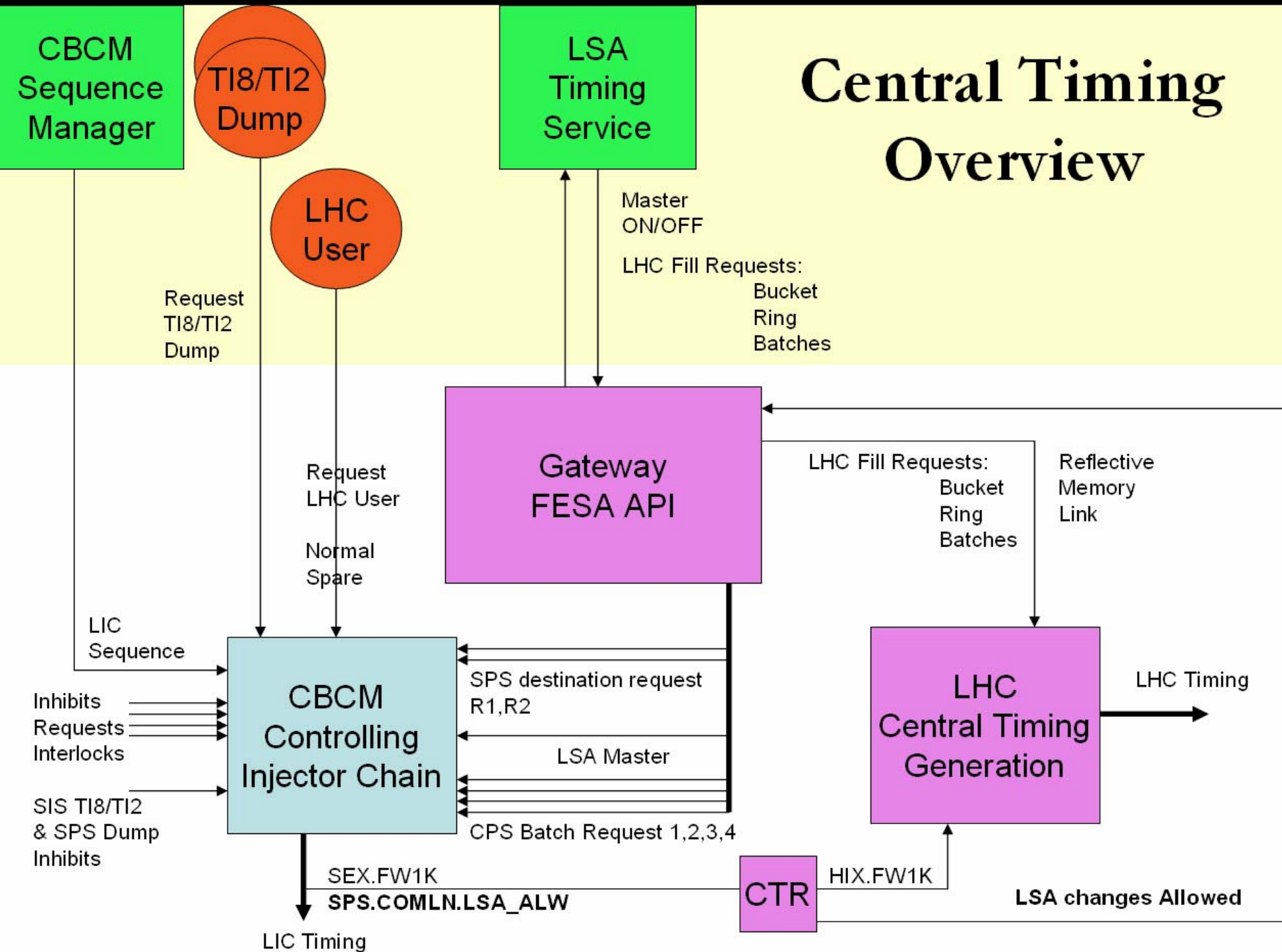
- Some frames are recognized by the hardware and cause special treatment
 - Two UTC frames carry the time of day in their payload
 - Millisecond frames are always sent in phase with the PPS
 - Telegram frames are stored in double buffers
 - Event frames cause counters to be loaded and triggered and may produce bus interrupts



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Central Timing Overview



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Reflective Memory

LHC Timing generator A



Identical
except
ID event

LHC Timing generator B



2Gbit/S
Token ring

VMIACC-5595
Single Mode
Hub



Protects token ring

64Mbyte
VMIPMC-5565
Reflective memory



LHC Gateway
Implements FESA API

Reflective memory:

A and B must always be
in the same state.
If no restrictions for
switch over



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GPS



Symmetricom CS4000 portable Atomic Clock

UTC Time and GPS

GPS
One pulse per Second

Symmetricom XLI

PLL
One pulse per Second

Phase locked 10MHz

Synchronization module in each timing generator crate
40MHz PLL

Basic Period 1200/900/600 ms

Advanced (100us)
One pulse per Second

Synchronized 1KHz (slow timing clock)

Phase locked 10MHz

Phase locked 40 MHz Event encoding clock

Control System

Event tables

MTT Multitask Timing Generator MTT

RS485 Timing

CERN UTC Time

Set once on startup & on Leap Seconds

UTC time (NTP or GPS)

External events

Timing receiver

PPS

10 MHz

1 KHz

40MHz

CTR

Delay

25ns steps





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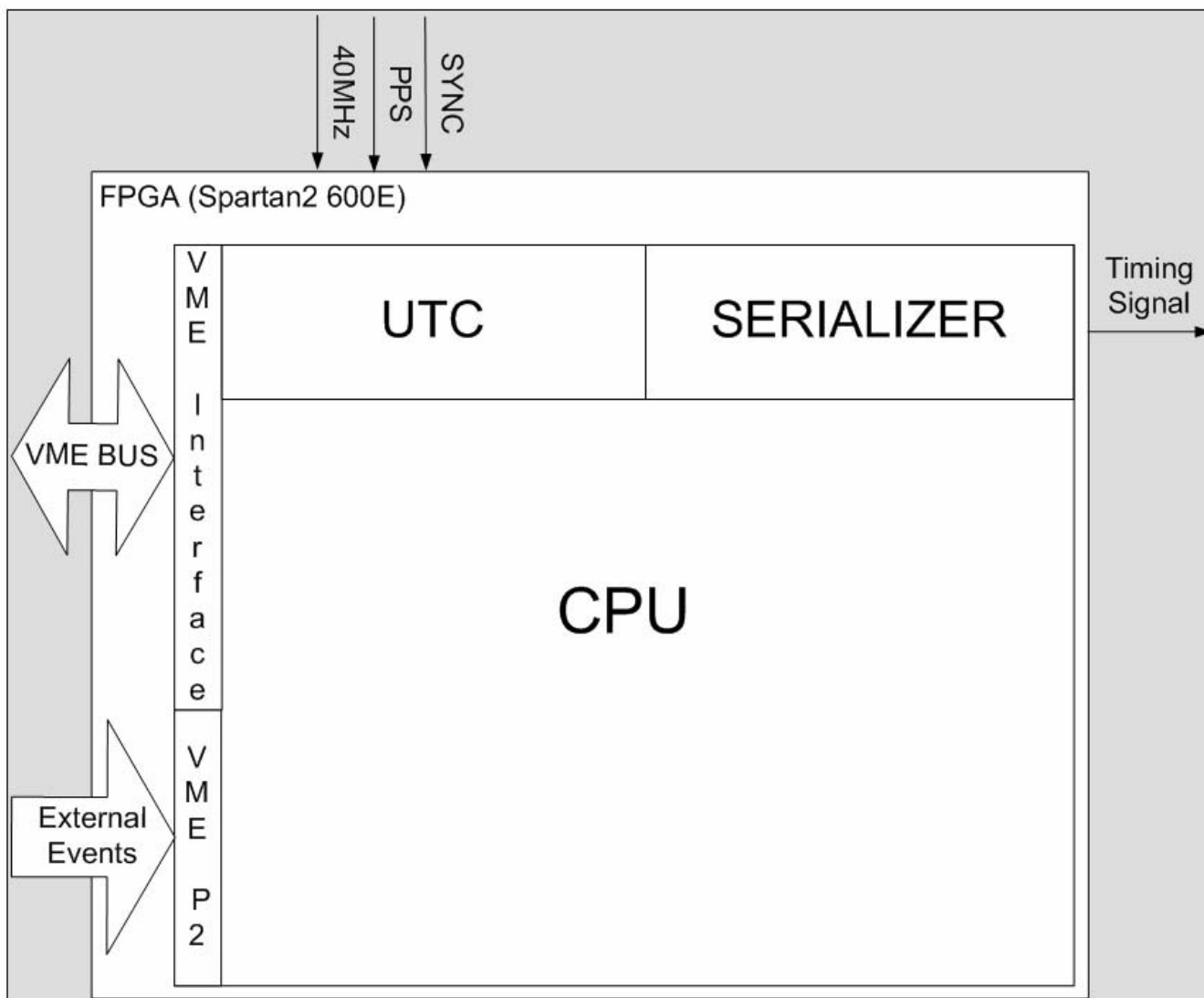


Multitask Timing Generator MTT

- **Hardware multitasking for 16 tasks**
 - 32 local registers per task
 - 218 Global registers
 - 6 Memory mapped IO registers
 - Timing frame out register
 - VME P2 in register ...
- **Host processor access to all registers**
- **Implements general purpose CPU**
 - Op-codes are triadic: AND SrcREG,SrcREG,DstREG – AND 0x7,VMEMP2,TMP
 - Arithmetic and logical
 - Move indexed, literal, register
 - Wait value, relative
 - Conditional branch
 - Interrupt host
- **Tasks defined from host via Task Control Block**
 - PC
 - PC Offset
 - Processor Status Word
- **Command and status registers allow host access to running tasks**



MTT hardware module



See: The LHC central timing hardware implementation
P. Alvarez, J. Lewis, J. Serrano CERN, Geneva, Switzerland

[This conference](#)



MTT External Events Task

```
strp:    % Start program and interrupt survey task
movb    TskStsRUNNING    LRegTASK_STATUS    % Say we are running
movb    ConsNOT_SET      LRegParRUN_COUNT    % Run forever
int     2                % Notify survey we are running
```

```
cont:    % Wait for the VME P2 bits and send out events accordingly
worv    ConsVMEP2_BITS    VMEP2            % Wait for VME P2 bits
movr    VMEP2            RegVmeP2          % Copy reg and clear bits
```

```
tdmp1:   % Test for dump ring 1
andv    ConsHX_DMPD1_BIT  RegVmeP2        LRegTEMP    % Test dump 1 bit
beq     tdmp2            % Go check for dump 2 bit
movv    ConsHX_DMPD1      EVOUT            % Send dump 1
movv    ConsHX_ENBPM1     EVOUT            % Re-enable after a dump
```

```
tdmp2:   % Test for dump ring 2
andv    ConsHX_DMPD2_BIT  RegVmeP2        LRegTEMP    % Test dump 2 bit
beq     tinj            % Go injection warning bit
movv    ConsHX_DMPD2      EVOUT            % Send dump 2
movv    ConsHX_ENBPM2     EVOUT            % Re-enable after a dump
```

```
tinj:    % Test for LHC injection
andv    ConsHIX_FW_BIT    RegVmeP2        LRegTEMP    % Test inject bit
beq     tpm1            % Go check for PM ring 1
movv    ConsHIX_FW        EVOUT            % Send injection forewarning
```

```
tpm1:    % Test for post mortem bit 1
andv    ConsHX_PM1_BIT    RegVmeP2        LRegTEMP    % Test PM ring 1 bit
beq     tpm2            % Go check for PM ring 2
movv    ConsHX_PM1        EVOUT            % Send PM-1 trigger
```

```
tpm2:    % Test for post mortem bit 2
andv    ConsHX_PM2_BIT    RegVmeP2        LRegTEMP    % Test PM ring 2 bit
beq     cont            % Go check for PM ring 2
movv    ConsHX_PM1        EVOUT            % Send PM-1 trigger (not PM-2)
```

```
jmp     cont            % Go wait for next P2 interrupt
```

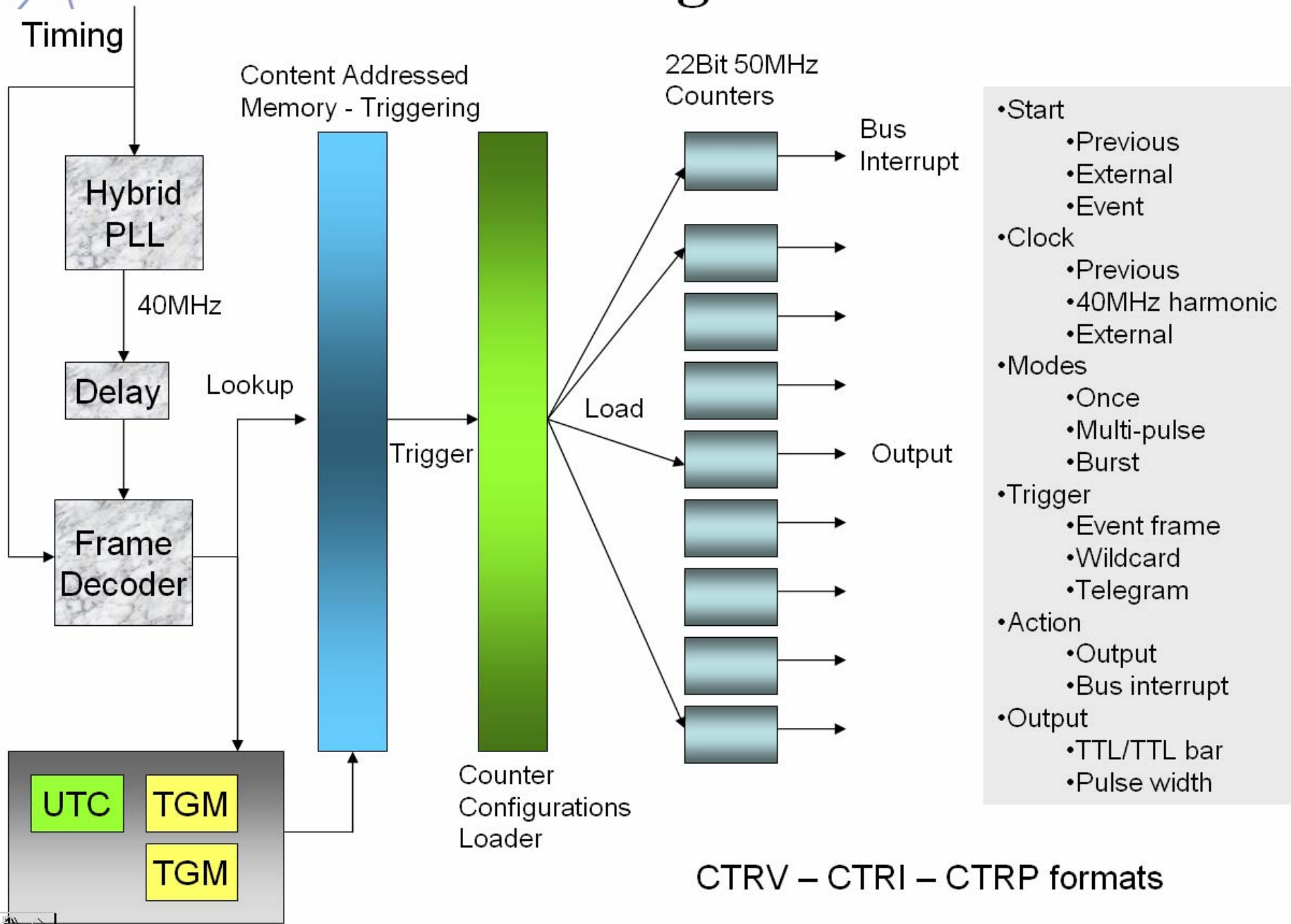


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Controls Timing Receiver CTR



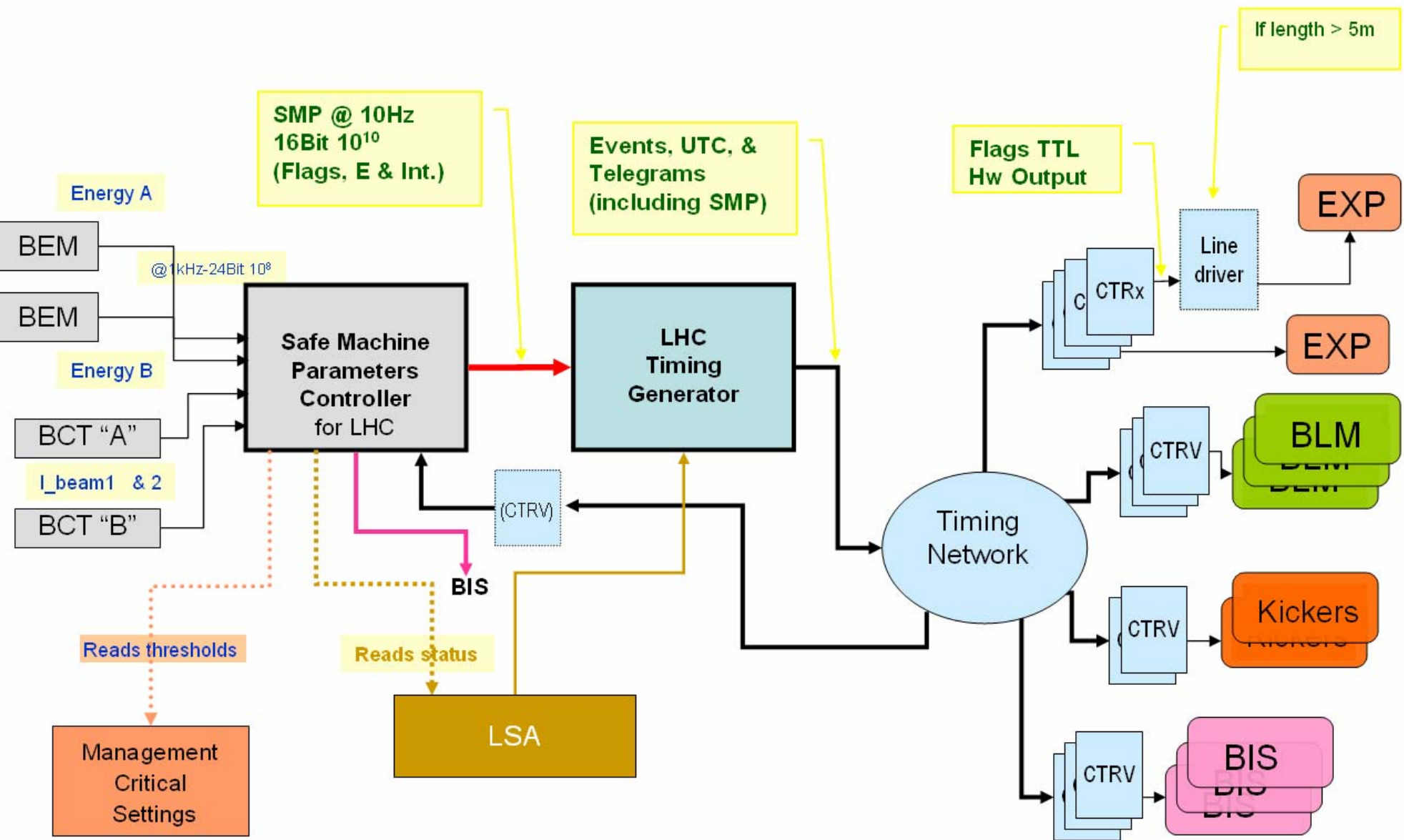


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Safe Machine Parameters Distribution





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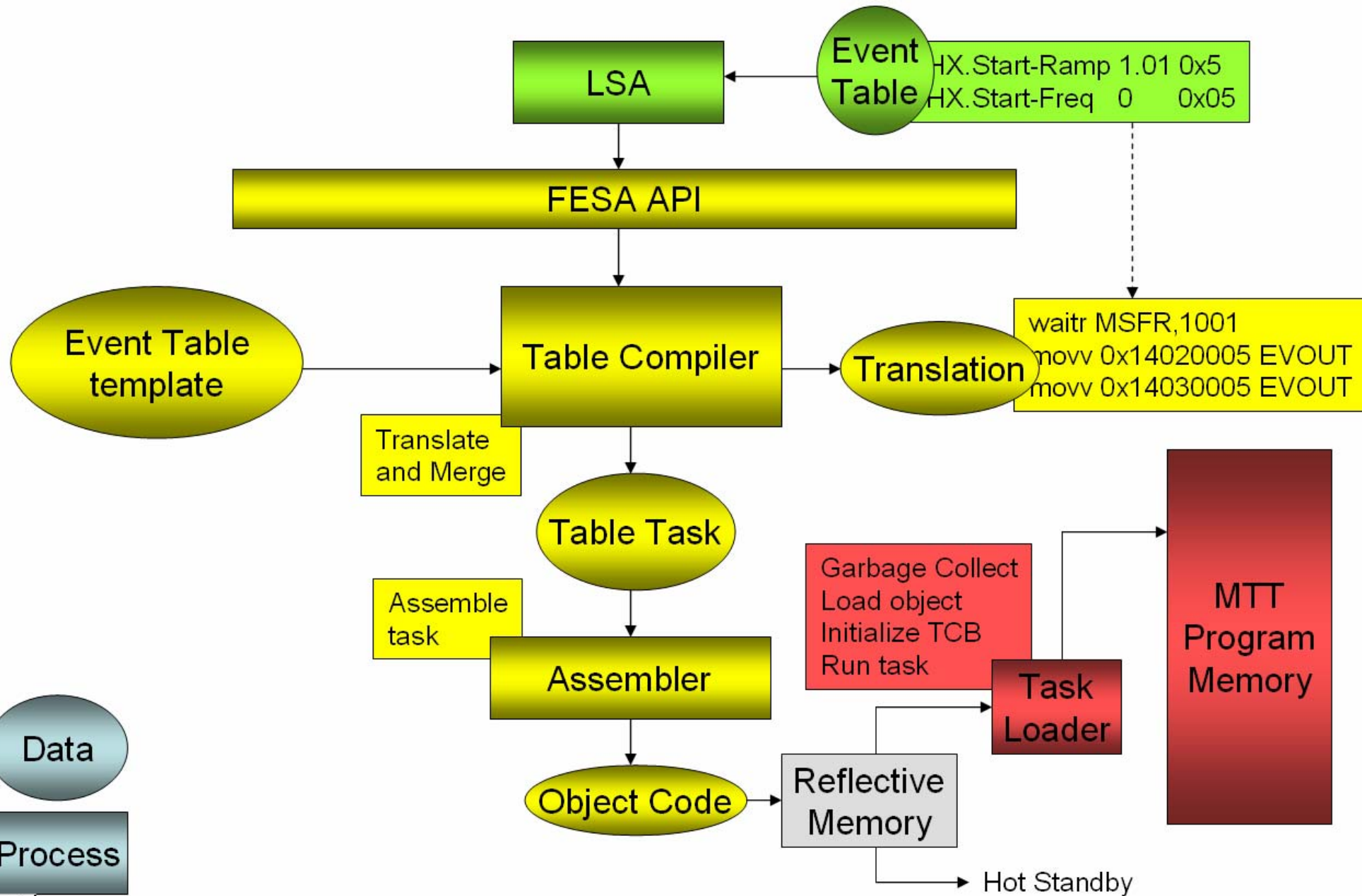
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LSA and FESA

- The FESA API is implemented on the LHC timing gateway
- Accesses timing generators across reflective memory
- Implements
 - Load or Unload event table
 - Get running tables list
 - Set event table run count and synchronization event
 - Stop or Abort event table
 - Set telegram parameters
 - Send event
 - Read status of tasks and MTT module



Event Table Processing



Conclusion

- Event tables model LHC machine processes.
- Reuse of existing timing boards was facilitated by using FPGAs and writing new VHDL.
- The LHC timing is monitored by hardware.
- Reflective memory has increased reliability.