ETHERNET BASED EMBEDDED IOC FOR FEL CONTROL SYSTEM

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Abstract

An Ethernet based embedded Input Output Controller (IOC) has been developed to upgrade the control system for the Free Electron Laser Project at Jefferson Lab. The embedded IOC, called the Single Board IOC (SBIOC), was integrated with a ColdFire embedded microprocessor and a Field Programmable Gate Array (FPGA) on a circuit board, which can be easily configured to control different kinds of I/O devices. The SBIOC provided features of a complete System-on-Module (SOM) as a stand alone system with abundant high speed I/O ports to couple with suitable devices. The software kits, Experimental Physics and Industrial Control System (EPICS) and Real Time Executive for Multiprocessor System (RTEMS), were chosen to work with our existing control system. The embedded IOC system has the features of a low cost IOC, free open source RTOS, plug-and-play-like ease of installation and flexibility.

INTRODUCTION

The Free Electron Laser Project at Jefferson Lab is an electron accelerator that provides intense, powerful beams of tunable infrared (IR) laser power. This complicated machine requires numerous control and diagnostic systems, some requiring high levels of precision. Currently most of the FEL systems are controlled, configured and monitored by a central VME based configuration. Some of the systems require the addition of new devices, but the extension needs expensive parts and cable. These VME crates currently control several different systems from one crate. This poses problems in that a fault in one system can impact the other systems, and also makes problem diagnosis more difficult.

The Ethernet based embedded system was proposed to solve these problems. The intention of this approach was to provide a localized solution for individual systems and components. Currently we have an embedded system installed with our latest revision of Beam Position Monitor (BPM) electronics [1][2]. The first version of the embedded BPM system has been successfully running in the field for over one and one half years. It has proven that the embedded controller is a low cost, reliable and easily maintained solution for our FEL control system upgrades. In order to provide more functionality and flexibility we designed the Single Board IOC, which combines the advantages of both a ColdFire microprocessor and a FPGA. The SBIOC was designed as a standard footprint for the newest version of the BPM electronics and other carrier modules, such as the 3U General Purpose Processor Cards, to perform more specific functions. More details of the system design will be presented in this paper.

SYSTEM DESIGN

The new system design is based on the Ethernet embedded distribution IOCs. Figure 1 shows the system layout. Each Single Board IOC was distributed on the front end devices around the FEL tunnel through an Ethernet connection. Comparing with central VME-based configuration, the new system would save lots of cable and connectors as well as independent localized solutions. Each Single Board IOC has a carrier board for the specific devices' functionality. Future plans include utilizing the IEEE 802.3, Power-over-Ethernet standard to transmit power, along with data, to the SBIOC and the front end electronic devices over the Ethernet network.

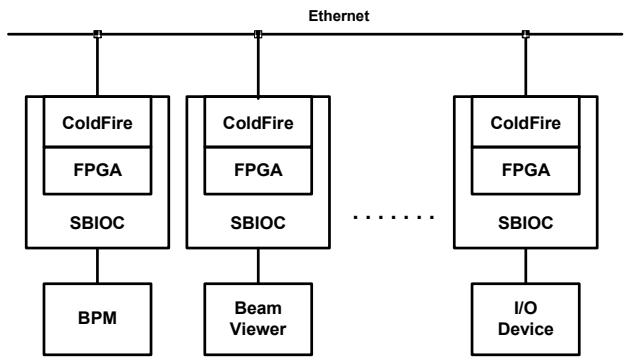

Figure 1: Layout of ethernet-based embedded IOCs.

Single Board IOC

The idea of Single Board IOC is to provide a standard foot print for the new embedded IOC. An Altera FPGA and a ColdFire uC5282 processor were integrated on a custom designed circuit board. FPGAs are very attractive for implementation into digital designs, because they have high component counts and provide enormous design flexibility with relatively low cost. The Arcturus ColdFire uC5282 processor is a complete "system on a module", which includes three basic highly integrated functional blocks, core processor, memory and Ethernet. The combination of the FPGA and the uC5282 processor makes the SBIOC suitable for all kinds of I/O control.

Figure 2 shows the block diagram of the SBIOC. The Altera Cyclone II EP2C8Q208 FPGA was chosen to connect with the ColdFire uC5282 processor. The interface between the FPGA and the ColdFire uC5282 processor includes a 24-bit address bus, a 16-bit data bus, and some bus control lines. A specific coded logic module on the FPGA, which is called the ColdFire-FPGA bridge, provides the functions of this interface. By setting up registers on the Chip Select Module of the uC5282 processor, the FPGA was mapped on the uC5282's

address space through the bridge and accessed as a peripheral. The address bus, data bus and control lines were coordinated by a communication protocol through the bridge.

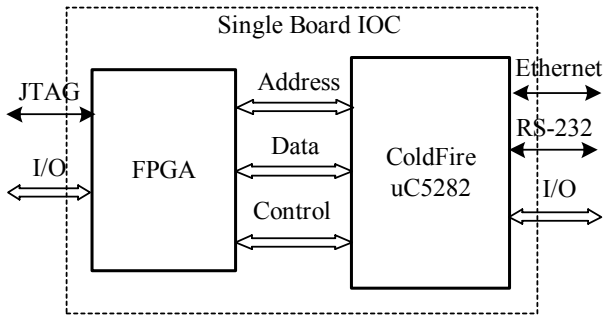

Figure 2: Layout of Single Board IOC.

The SBIOC has two 40-pin headers and that allows it to drop onto a carrier board as a module. Since the new board is pin-pin compatible with some existing designs, those systems can be upgraded without having to redesign the carrier card. The two 40-pin connectors have 48 I/O pins from the FGPA, 6 general purpose I/O pins and a QSPI bus from the ColdFire uC5282, and other auxiliary I/O bus. JTAG was used to program the FPGA and upload the code on an EEPROM device connected with the FPGA.

The JTAG port also could be used to debug large number of nodes in the FPGA with the Logic Analyzer, provided by Quartus II, when the FPGA is running. Figure 3 shows the picture of the SBIOC card with the FPGA underneath the uCdimm ColdFire uC5282.

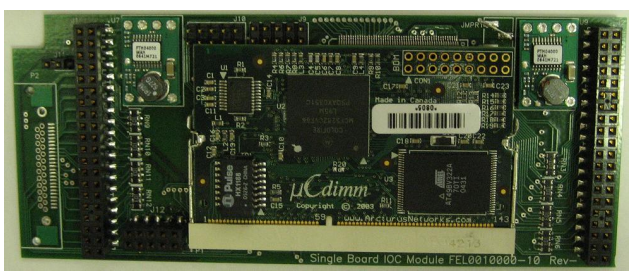

Figure 3: The picture of Single Board IOC.

BPM Control

The new version of BPM electronics uses the SBIOC to sample four channels of each BPM can. Figure 4 shows the picture of the new BPM electronics with the Single Board IOC card. The FPGA directly collects the data from the ADC at the maximum ADC throughput. A relatively high speed 16-bit sampling ADC, AD7655, was used to obtain a throughput of 1 MSPS. 16-bit data from all four input channels are parallel sampled from the ADC to the FPGA. By controlling the Multiplexer Select and Data Channel Selection signals, all of the data from four channels; X+, X-, Y+, Y-, that can be read to the FPGA with a maximum sample rate of 500 KHz for each channel. The sampled data is then stored in a memory block on the FPGA. The ColdFire uC5282 processor reads the data from the memory through the data bus and executes all the calculations and calibrations with an EPICS sequencer. The BPM can either be triggered by an external beam sync signal or self-trigger according the intensity of the beam current. By using the SBIOC, this BPM will have fast throughput and better position resolution. It is also possible that we can provide some beam diagnostics that we were not available with the current system.

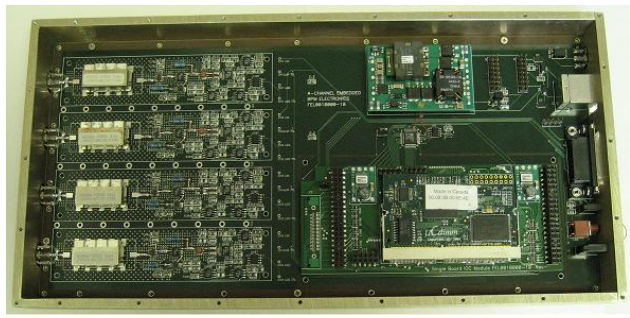

Figure 4: The picture of the new BPM.

3U General Purpose Processor Card

The 3U General Purpose Processor Card is the carrier board that provides a bridge between the Single Board IOC and the electronics used in several different systems. The block diagram of this board is shown on Figure 5. This card was designed to be pin to pin compatible with a DSP card that we have used to control some systems, such as the Temperature Monitoring Crate and the Sextapole Magnet Power Supply Control Crate. When designing this card we utilized as many resources from the SBIOC as possible to truly have a generic I/O card that would be configured for specific applications. The I/O available from this card through the 96-Pin backplane connection is illustrated below and is as follows:

- 40-bit digital I/O
- 8-bit address line
- 8-bit QSPI bus
- 6-channel high speed ADC
- 10-channel high resolution ADC
- 4-channel high speed DAC
- Ethernet and RS-232 communication

We have designed other controls around this 3U General Purpose Processor Carrier Card such as Beam Viewer controls, GC magnet power supplies, HVPS controller, and vacuum instrumentation. Each of these systems utilizes various I/O pins from the 3U General Purpose Processor Carrier Card, the only difference is the function of the software in the SBIOC. By altering the software of the SBIOC we have a generic processor card that can be deployed within various stand-alone systems.

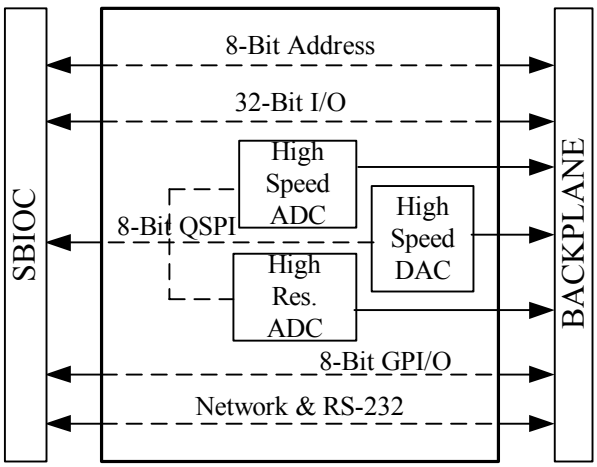

Figure 5: Layout of 3U general purpose processor card.

Software Design

Open source software tools, RTEMS [3][4] and EPICS [5], were chosen as the real-time control systems for the embedded IOCs. RTEMS version 4.7 and EPICS R3.14 were installed on a Linux machine, where the IOC applications were created. By cross compiling with the EPICS, the RTEMS kernel, the IOC device support, and the databases could be downloaded into the embedded IOC. The firmware could be loaded on the memory of the IOC through Ethernet, when the IOC is running. So, it makes it easy to update the application without shutting down the machine and taking the SBIOC out of the field. The embedded IOC can be remotely rebooted from a host machine through Channel access. We have completed the applications for BPM electronics, 3U General Purpose Processor Card, and Beam Viewer control. More applications are planned for development for other systems.

CONCLUSIONS

The prototype of the Single Board IOC has been designed and built. The functional codes for the FPGA were programmed and the uC5282 processor could access the FPGA through the address bus and data bus. The SBIOC was tested with the BPM electronics, and we will design it into the next version of the BPM electronics. The 3U General Purpose Processor card was designed to provide a carrier board for the SBIOC and will be used to upgrade some other control systems for the FEL.

The Ethernet based SBIOC integration of an FPGA with a ColdFire uC5282 processor provides a new configuration for the upgrade of our FEL control and diagnostic systems. By using the open source RTEMS and EPICS real-time control system, there will be no license hassles and creating a cost reduction. By moving the IOCs to the front end, we cut the cost of expensive cables. The SBIOC will make the system more powerful and flexible, and it will improve the performance of FEL control and diagnostic systems. This configuration has the potential for use in other accelerators and light sources.

ACKNOWLEDGEMENTS

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