

HARD- AND SOFTWARE OF THE ATLAS PIXEL DETECTOR CONTROL SYSTEM

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ABSTRACT

For the ATLAS experiment at the LHC, CERN, a pixel detector is under construction. Its operation will require more than 10000 channels with a much higher number of parameters which demand monitoring and control. On the hardware side this implicates the necessity of economic solutions, while on the software side efficient methods are required to build clearly structured user interfaces. We describe the various hardware elements, but concentrate on customer designed components like the interlock matrix and a supply and control system for the on detector part of the optical link.

The core of the control software is based on 'PVSS', a commercial supervisory control and data acquisition system. To allow parallel work for the developers and to provide the operator with user friendly interfaces, the overall control system is split into sub-projects. Front end integration tools establish the connection to the hardware and allow the experts to configure the different hardware channels. During operation non-experts will use the system integration tools, which provide a detector oriented view. A tree structure allows the navigation through the virtual detector. Furthermore we report on an interface to the data acquisition system and a 'ROOT' based histogramming interface which can be used for a detailed analysis of the control system.

THE PIXEL DETECTOR

The Pixel detector of the ATLAS (A Toroidal LHC Apparatus) experiment is a segmented silicon-based semi-conductor detector. While the barrel section consists of three cylindrical, concentrically mounted shells, equipped with staves to carry the detector modules, the end caps consist of three identical discs per side to install the detector modules. Taking into account the modularity of the services and power supplies, bi-staves, half staves respectively disc sectors are the relevant segments for the detector control system (DCS).

The detector module is the smallest independent unit which DCS can act on. Each module owns 16 front end chips which connect the pixel sensors with the read-out electronics and which are supervised by a module controller chip. The data transfer is handled by optical links which connect the detector modules to the off-detector read out system.

THE HARDWARE OF THE PIXEL DCS

The 1744 detector modules and their related readout chains require several supply voltages for their operation. A good compromise between the number of required channels at an economically acceptable level and individually controllable detector modules had to be found. Further main components of the DCS hardware are the temperature and environmental monitors and a related interlock system.

The Embedded Local Monitor Board

The Embedded Local Monitor Board (ELMB), developed by the ATLAS DCS group, is a multi purpose, low cost I/O device to monitor and control various hardware components [1]. Each ELMB provides up to 64 multiplexed ADC channels and 24 digital I/O-lines. Its CAN (Controller Area Network) bus interface and an OPC (OLE for Process Control) server provided by the ATLAS DCS group allow the integration into the higher level DCS software.

One group of required channels in the pixel DCS accounts for the large number of temperature sensors that are used throughout the detector volume. The majority of those is formed by the module thermistors. Additionally the monitoring of the environment and of other temperature sensitive components needs more ADC channels. All devices are equipped with 10 k Ω negative temperature coefficient thermistors (NTC) and their readout is based on the use of the ELMB.

The control of our custom made DCS hardware is based on the usage of the ELMB, see below.

The High and Low Voltage Supplies

Each module needs three floating voltages: two low voltages for the operation of the analogue and digital part of the module's front end electronics and one high voltage for the depletion of the sensor. The module high voltage (700 V, 4 mA) is directly provided by power supplies made by the vendor "iseg" (Rossendorf, Germany) and follows the modularity of the disc sectors / half staves, thus supplying 6 or 7 modules each.

Due to the high requirements concerning the stability of the low voltage, custom made low voltage regulators are used for both low voltage channels. These regulators are fed by commercial low voltage power supplies (12V, 11.5A) of the vendor "W-IE-NE-R" (Burscheid, Germany). One W-IE-NE-R channel supplies 6 to 7 regulator channels.

While the HV system owns a CAN bus interface, the low voltage system comes with a TCP/IP interface, which allows the integration into DCS via OPC servers.

The Regulator System

To protect the front end chips, which are fabricated in deep-submicron technology, against transients, remotely programmable regulator stations are installed as close as possible to the detector modules. This radiation hard system has been developed by the INFN Milano [2]. The regulators compensate for the large voltage drops on the low mass cables in the detector active volume and in parallel provide an individually adjustable control of the low voltage lines for each detector module. The core of the system is built by the ST regulator LHC4913 from ST Microelectronics (Catania, Italy), which can provide a maximum current up to 3 A and accepts input voltages up to 14 V. Using digital trimmers, the output voltages can be adjusted. The control is based on a FPGA (XC4036XLA-09HQ240C) from Xilinx (San José, USA), while the communication to the outer world is established by ELMBs.

The SC-OLink

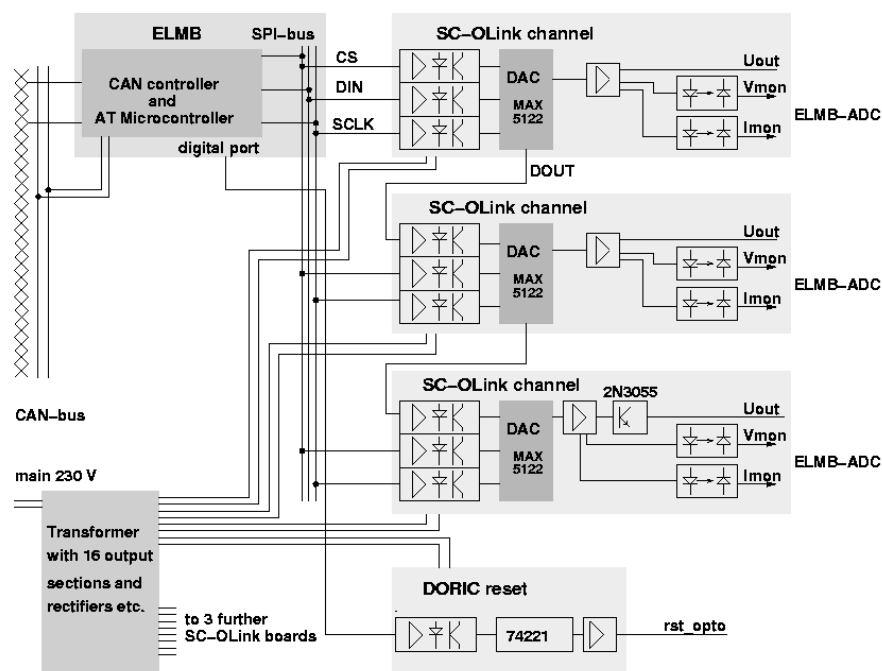


Figure 1: The Supply and Control System for the optical link

Besides the power supplies directly involved in the module powering scheme, additional power supplies are needed for the operation of the optical read-out. The electrical information is transformed

into light-signals that bridge the bigger part between the detector and the counting room (about 100 m). On the detector side the conversion takes place on the opto-board which needs three different operating voltages with outputs between 5 to 20 V and 20 to 800 mA. All three are provided by custom made power supplies called "Supply and Control for the Optical Link" (SC-OLink). Whilst the SC-OLink delivers two voltages directly to the loads, the third one with a higher power output is supplied via the regulator system.

Figure 1 shows the design of the SC-OLink. Using individual transformer lines, opto couplers and a one channel DAC MAX5122 from MAXIM (Sunnyvale, USA), the floating circuit is realized. Additionally one control signal per opto-board is delivered, which allows a reset of the board. Monitoring and control of the SC-OLink are given by the usage of the ELMB.

The Interlock System

To protect the sensitive electronics against heat ups and the operators against risks due to infra-red laser light, a hardware based interlock system is under development. Especially the performance of the sensitive detectors can deteriorate significantly by overheating, therefore each detector module is equipped with its own temperature sensor. All temperature signals are fed to the home-made interlock box [3], which creates in case of high temperatures a logical signal, for further processing. The electrical design of the interlock box is based on a comparator circuit, whose thresholds can be adapted by simply exchangeable resistor networks. This development is radiation tolerant and compatible to the ELMB, which is used for parallel monitoring.

Adding up the signals from all temperature sensitive equipment and from all laser boards results in 2100 lines, which must be logically combined and then split onto 1000 power supply channels and laser related circuits. The core of the interlock system is given by the flash FPGA (ATA075) from Actel (Mountain View, USA). As the required number of I/O lines is even for an FPGA quite high, 28 interlock matrices are defined to handle parts of the detector. This interlock system will always ensure that no more hardware components than needed are switched off and that the rest of the detector remains operational.

THE SOFTWARE

While all temperature channels are only monitored by DCS, all other channels provide a two-way communication in terms of reading and setting values. Therefore most channels that are integrated in the DCS account for more than one parameter, leading to a total sum of 35000 parameters that need to be managed by DCS.

For the automatization of the DCS, the commercial PVSS (Prozessvisualisierungs- und Steuerungssystem) environment will be used, which is a SCADA (Supervisory Control And Data Acquisition) software solution from ETM (Eisenstadt, Austria).

To prevent loss of information, PVSS is able to store process variables in "data point" structures. These structures consist of data points (DPs) and data point elements (DPEs). In our case a DP always is a structure, like a folder, and a DPE can be a further structure or a value like float, bool etc.. All DPs and DPEs can be archived during run-time.

PVSS offers the possibility to split the DCS software into several independent sub-projects that can be developed in parallel. In a short overview the three main building blocks of the Pixel-DCS will be presented here. The first is the Frontend Installation Tool (FIT) which is responsible for the communication with the DCS hardware like power supplies. The second building block is the System Integration Tool (SIT) that is basically managing all monitoring and control aspects inside PVSS. Further fields of work from the software point of view are the DAQ-DCS Communication (DDC) which is responsible for the whole communication between the DAQ (Data AcQuisition) and the DCS world and the enhancement of the histogramming facilities.

Functional versus Geographic Approach

In the following paragraphs the terms "functional" and "geographic" are used. Functional in this context means that the classification of the hardware follows certain device types, whereas geographic stands for a classification of the hardware following the detector structure. The two examples below show how a high voltage power supply is accessed using both approaches:

- “Functional”: Example: a power supply belongs to the group of high voltage supplies
 - Access via: “IsegHV18.Channel3”
- “Geographic”: Example: a Module has a high voltage supply
 - Access via: “Module4.HV”

Front End Installation Tool

Before monitoring and control of the physically connected hardware components can begin, these components have to be included into DCS using the Front End Installation Tool. To allow hardware-access for other PVSS-based DCS applications, the FIT creates so called “hardware data points” inside the PVSS-project’s data point structure. Each connected device is represented by a corresponding data point containing all relevant device information such as voltages and currents in form of data point elements.

Besides being the underlying layer for all other hardware-communicating DCS components, the FIT also provides panels to monitor and control the devices through direct access to the hardware data points (functional approach).

The first FIT developed by the authors is able to monitor and control the different kinds of ELMB setups that differ in the use of the analog and digital I/O channels. An additional FIT is able to integrate iseg power supplies, while current developments lead to the integration of the “Back of Crate”-card (BOC, see figure 2), which is a part of the optical read-out chain, and to a FIT for the W-IE-NE-R power supplies.

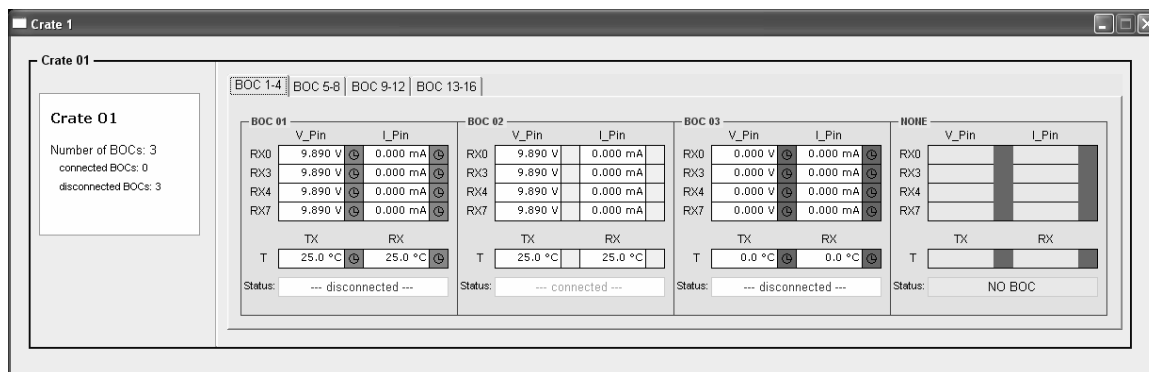


Figure 2: Panel of the Front End Integration Tool for the Back-of-Crate cards

System Integration Tool

The above mentioned variety of hardware channels has to be managed in an efficient and user friendly way. Therefore the SIT restructures the hardware components that have been included into the DCS by the FIT in a geographical way.

In order to do so, all hierarchy levels of the detector (modules, half staves, bi-staves) have to be connected to the correct supply and monitoring channels. This process is completely analogous to the physical cabling of the on- and off-detector hardware.

In contrast to the functional oriented FIT the System Integration Tool builds up a second data point structure consisting of “software data points”. Those data points represent the detector modules or half staves and have to be connected with the hardware data points created by the FIT.

The integration of the supply and monitoring devices into the software data point structure can either be done by loading configuration files or by configuring the system manually. For the latter case the software provides geographically structured panels where the user can set up the system in an easy to use graphical environment. The principle of this manual configuration is shown in figure 3.

Once the integration of the devices into the SIT is finished, all relevant monitoring and control functionality is available directly through the SIT. As mentioned above, the SIT follows the detector hierarchy and therefore it resembles a virtual detector that can be accessed either by browsing a tree-

like structure or through a simplified graphical representation of the detector. By doing so the user avoids the necessity of knowing the connection between the on- and off-detector hardware and all information belonging to the selected detector part is available in a single panel.

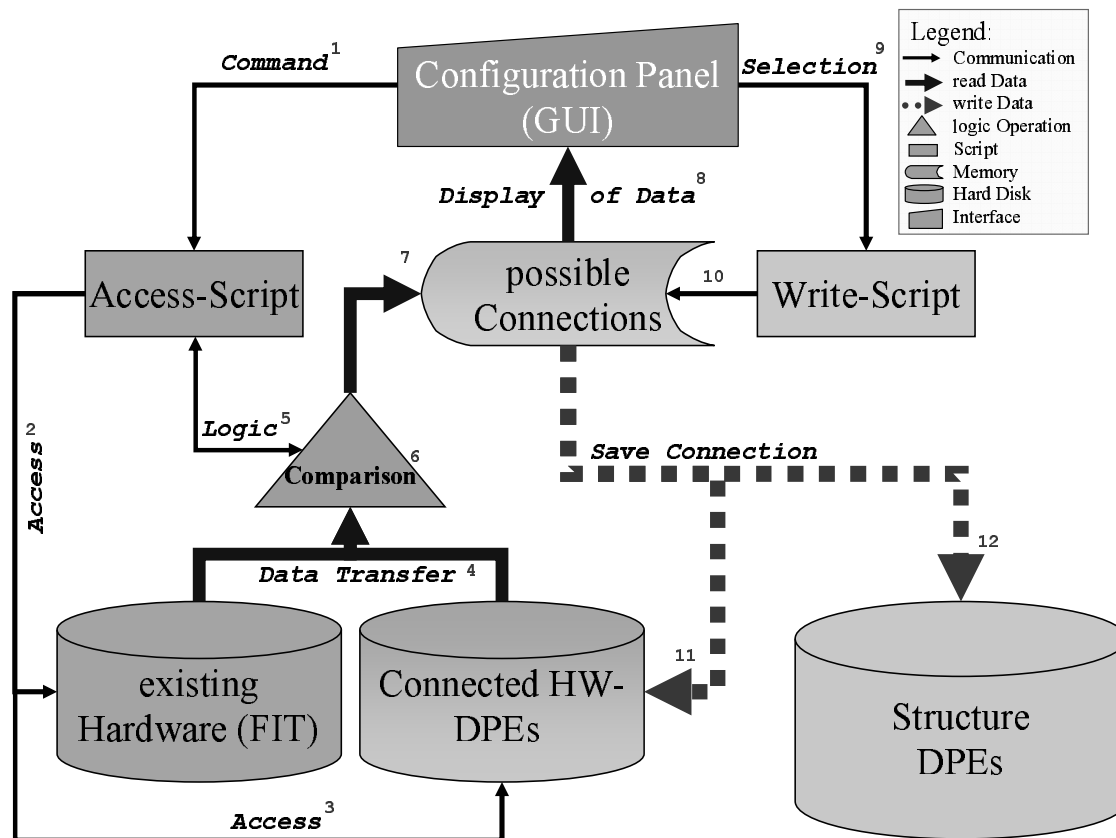


Figure 3: Configuration using the System Integration Tool

The DAQ-DCS Communication

From the operation point of view the pixel detector needs two program packages to work together: the Data Acquisition (DAQ) and the DCS software. Besides the pure data taking capability, the DAQ software will also be responsible for starting / stopping of data taking runs that might be necessary during normal detector operation, or in the latter case due to a critical detector condition.

Therefore it is important to be able to transfer information from DAQ to DCS and vice versa. The DDC package, developed by the ATLAS DCS group [4] offers three transfer types (data, messages and commands), which for example are needed for the BOC-interface, and thus has been chosen for this task.

According to the pixel detector needs, the DDC facilities have been adapted. In particular the operation of the optical data transfer requires a reliable communication between DAQ and DCS. A first pixel specific DDC application was tested successfully during a long term test beam period in 2004 [5].

The ROOT-Interface

Despite the various tasks that are related to the integration of the on- and off-detector hardware, another main task of the DCS software will be the monitoring and control of all connected devices. Whilst most of the required functionality is covered by PVSS itself, the trending capabilities of the SCADA software are limited.

Therefore the high energy physics analysis tool "ROOT" [6] has been chosen to be used for ATLAS Pixel DCS trending purposes. In order to do so, a software interface had to be written based on the already existing PVSS-ROOT interface [7] provided by Viatcheslav Filimonov (CERN, ATLAS DCS).

Using the interface one is able to generate trends and histograms without the need of having PVSS installed on his PC as long as a TCP/IP connection to the DCS PC is given. An easy to use graphical user interface has been implemented based on a ROOT panel. This panel allows the display of static graphs (value vs. time) and dynamic trends (value vs. time) created by any numerical PVSS data point element. Further static and dynamic histograms (value distribution) and relation plots (value vs. value) are offered.

SUMMARY AND OUTLOOK

Following the roadmap leading to the final construction of the ATLAS pixel detector at the LHC in 2007, the Pixel DCS is now able to monitor and control a big part of the used hardware components that have all reached production readiness status. The custom made regulator system, the SC-OLink and the Interlock system allow the control and adjustment of the operation parameters for small detector segments. Their designs combine adaptation to detector specific requirements and budget constraints.

The question of how to manage the large number of hardware-connections and process-parameters involved has been answered by introducing the geographical approach. Additionally the communication between the DAQ- and the DCS-world has been established and a ROOT based interface has been implemented, offering enhanced histogramming facilities.

For the future extensive tests with larger parts of the real detector are foreseen. This will give the possibility to further develop the Pixel DCS hard- and software and helps to ensure the full DCS capability.

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