



# The development of a 128-channel ultra-low noise trans-impedance amplifier system

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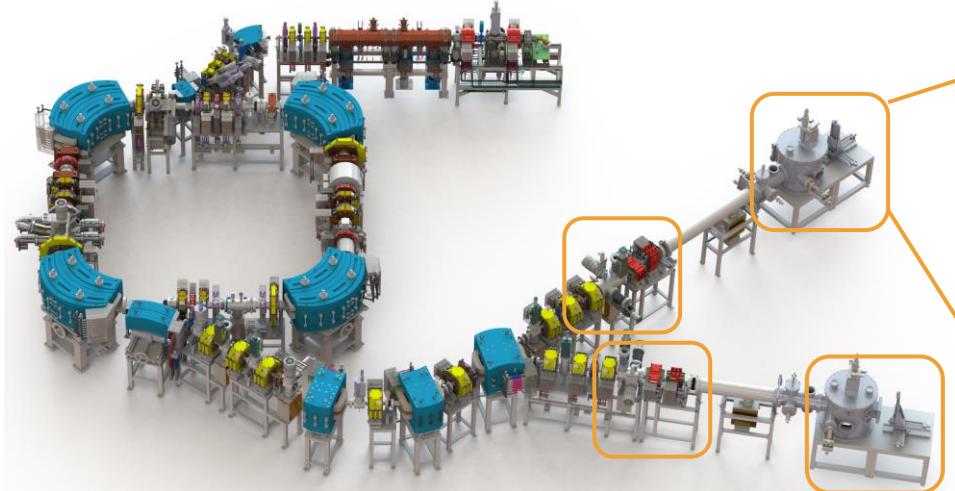
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# Background and Significance

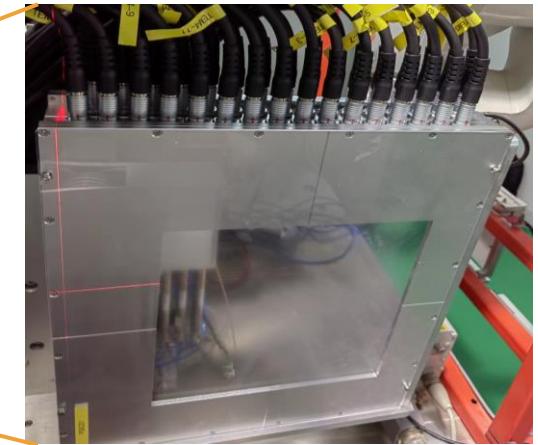
## Proton Radiation Effects Facility



## PREF's terminal



## MSIC: Multi-strip Ionization Chamber



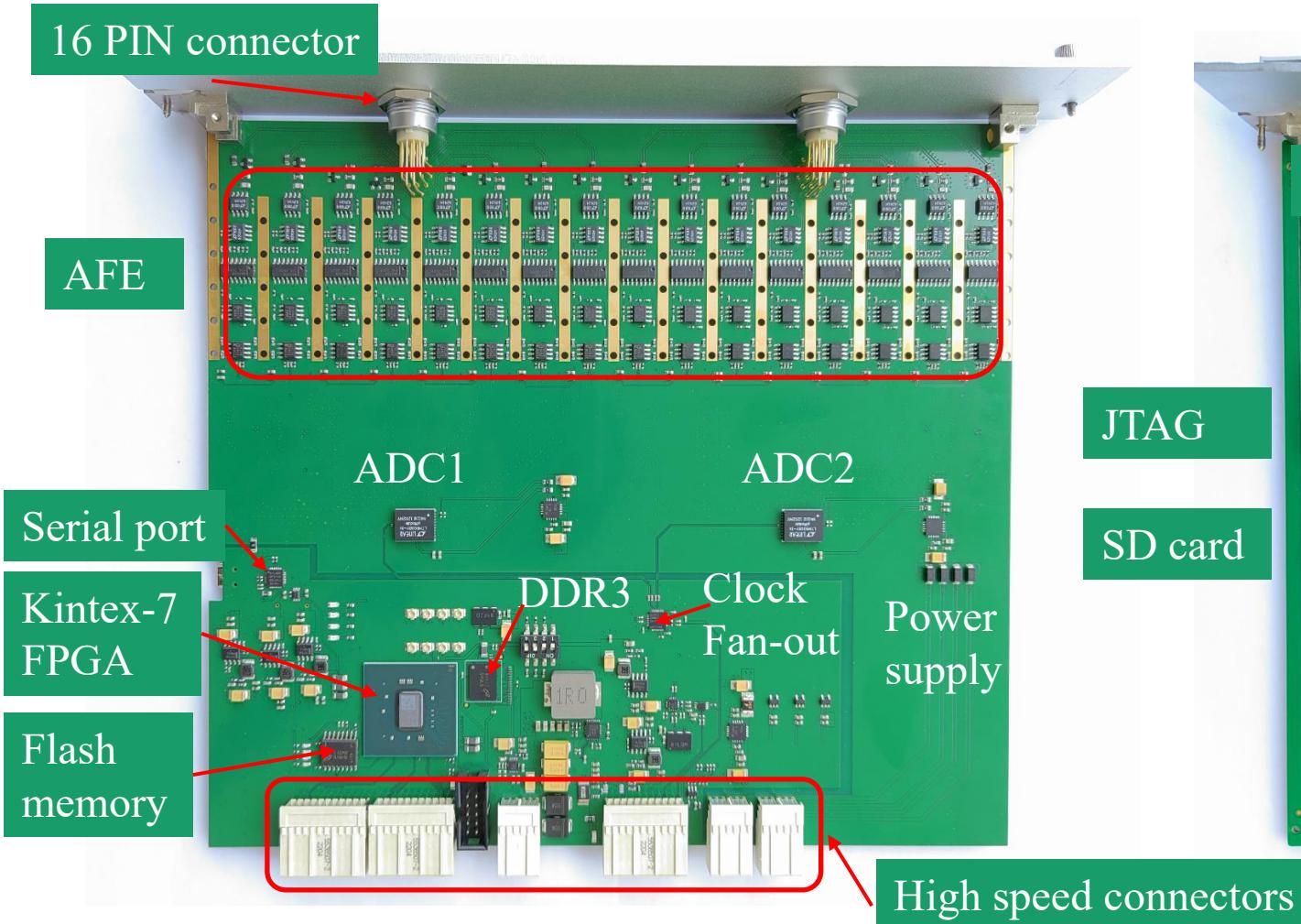
Parameter	Value
Number of channels	128 ( $16 \times 8$ )
Measurement range	25 pA ~ 1.8 $\mu$ A
Analog bandwidth	1 kHz
Sampling frequency	60 MHz

## readout system

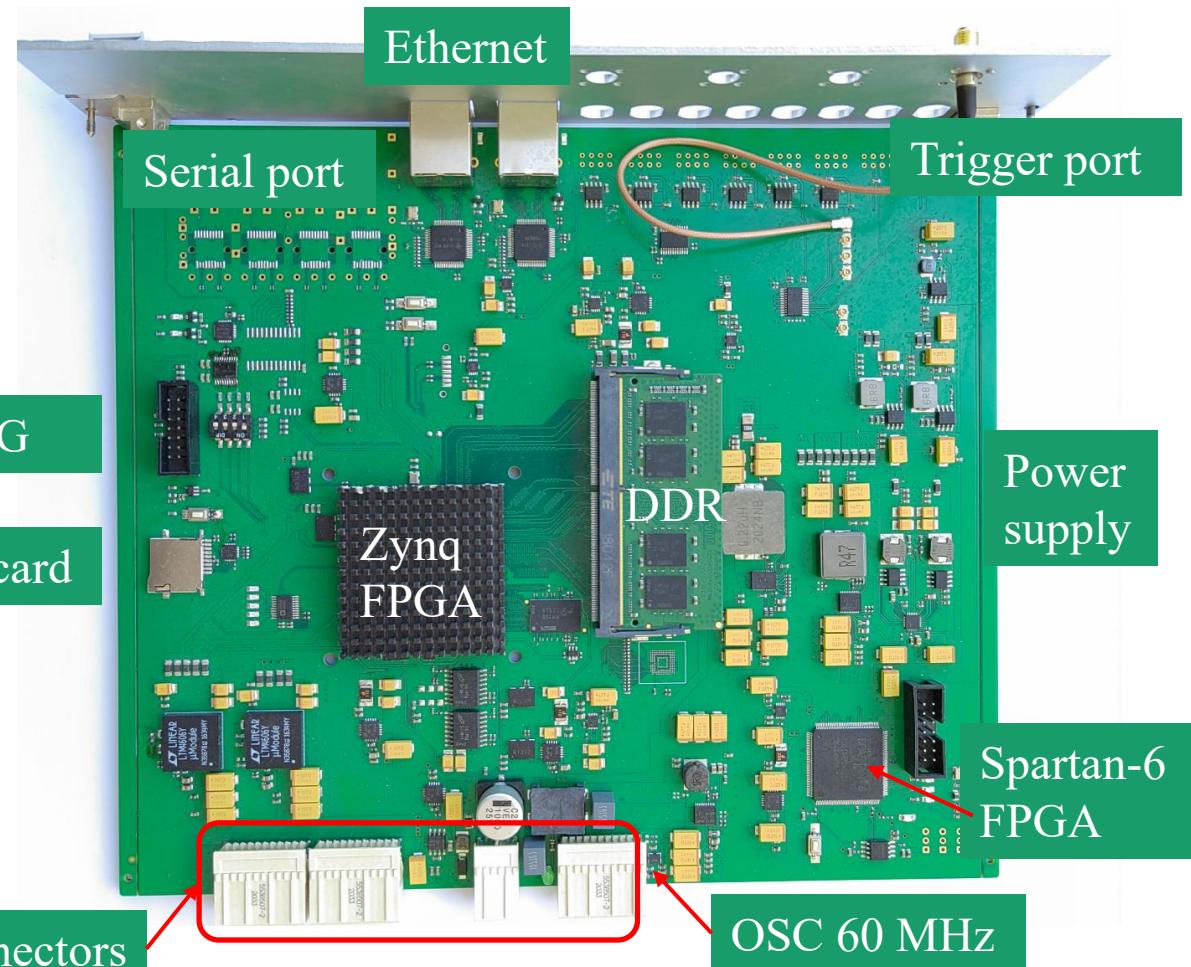


# System Structure

Data acquisition board and AFE

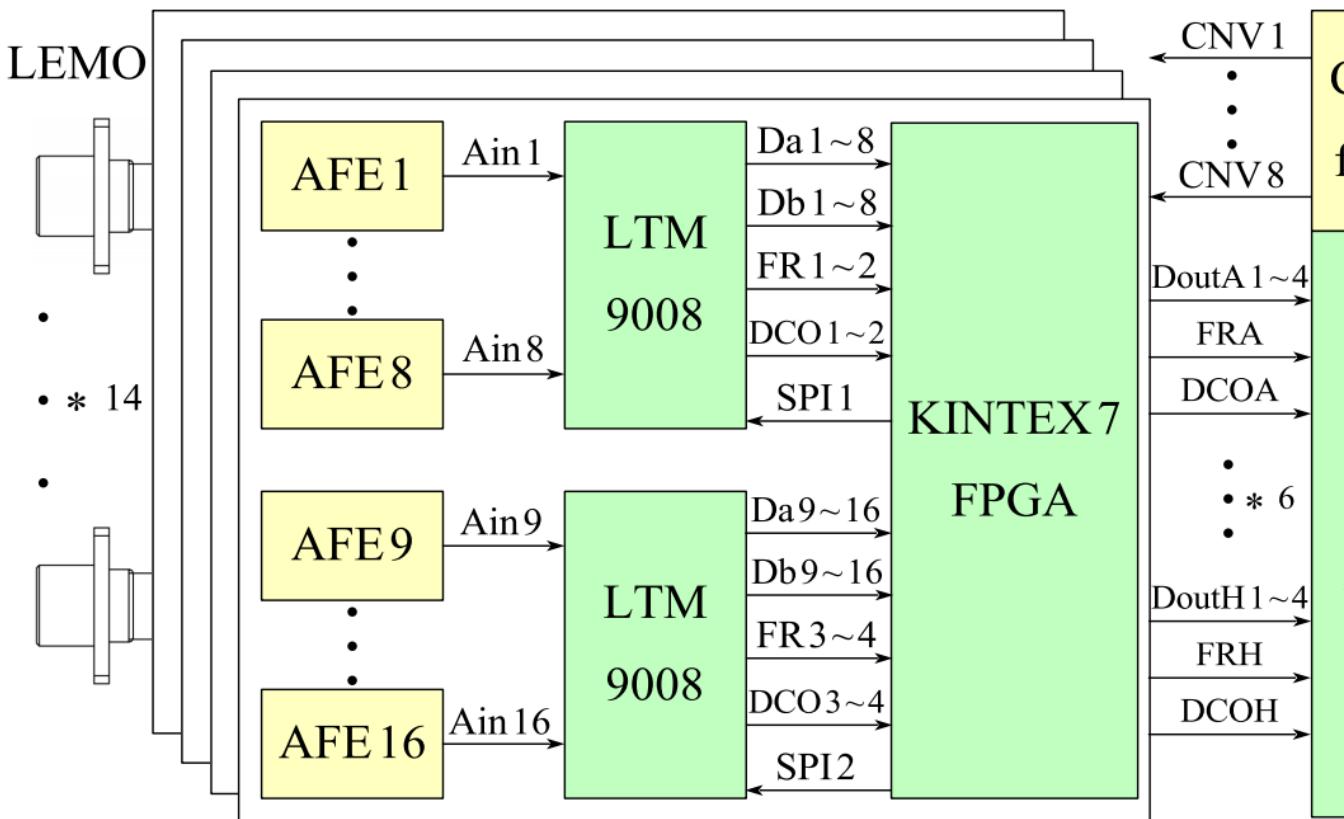


Data processing board



# System Structure

Data acquisition board and AFE\* 8



Data processing board

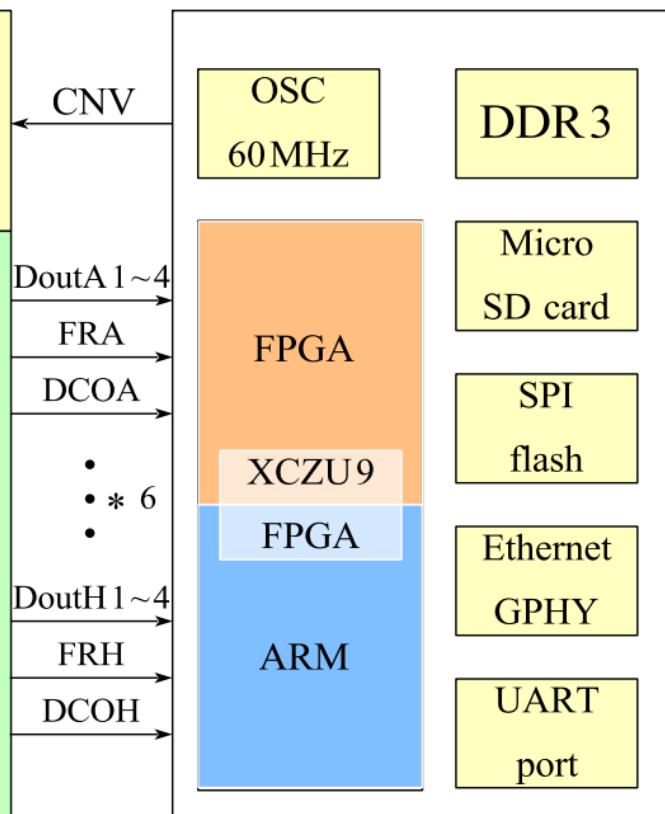
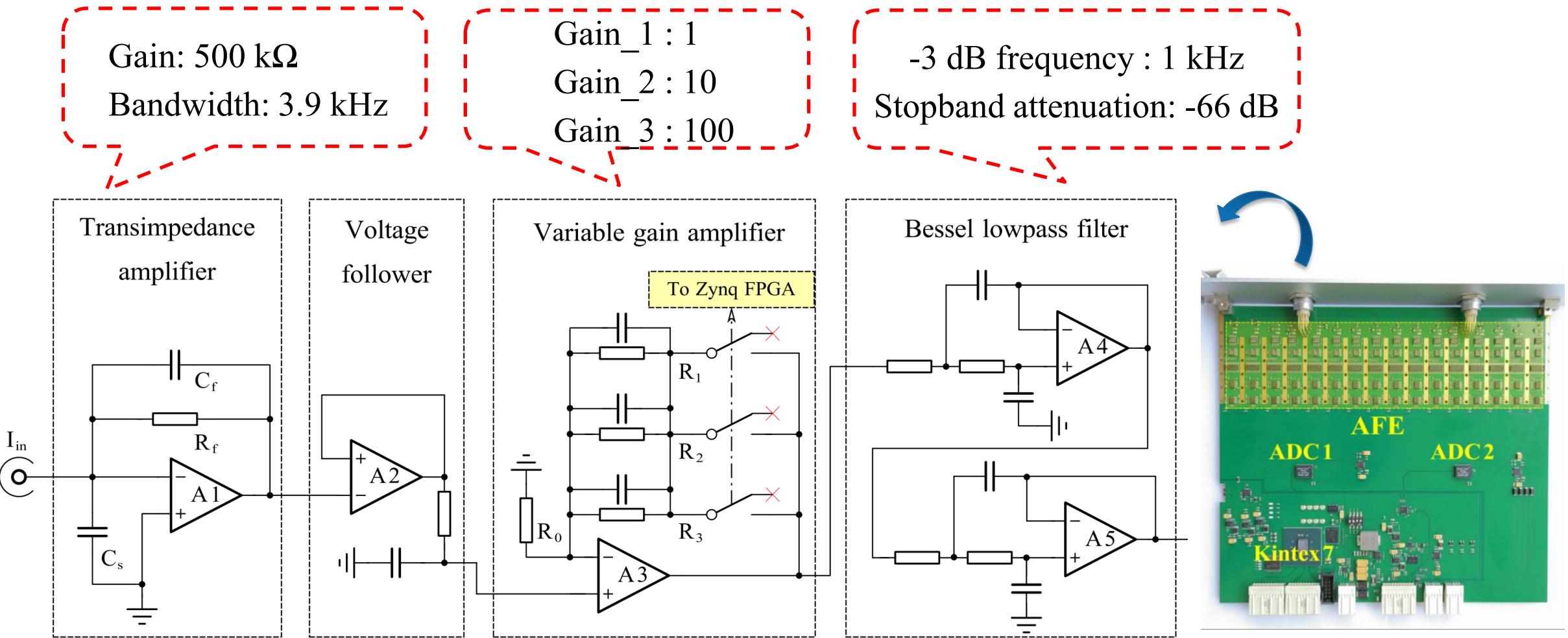


Diagram of this multi-channel readout system

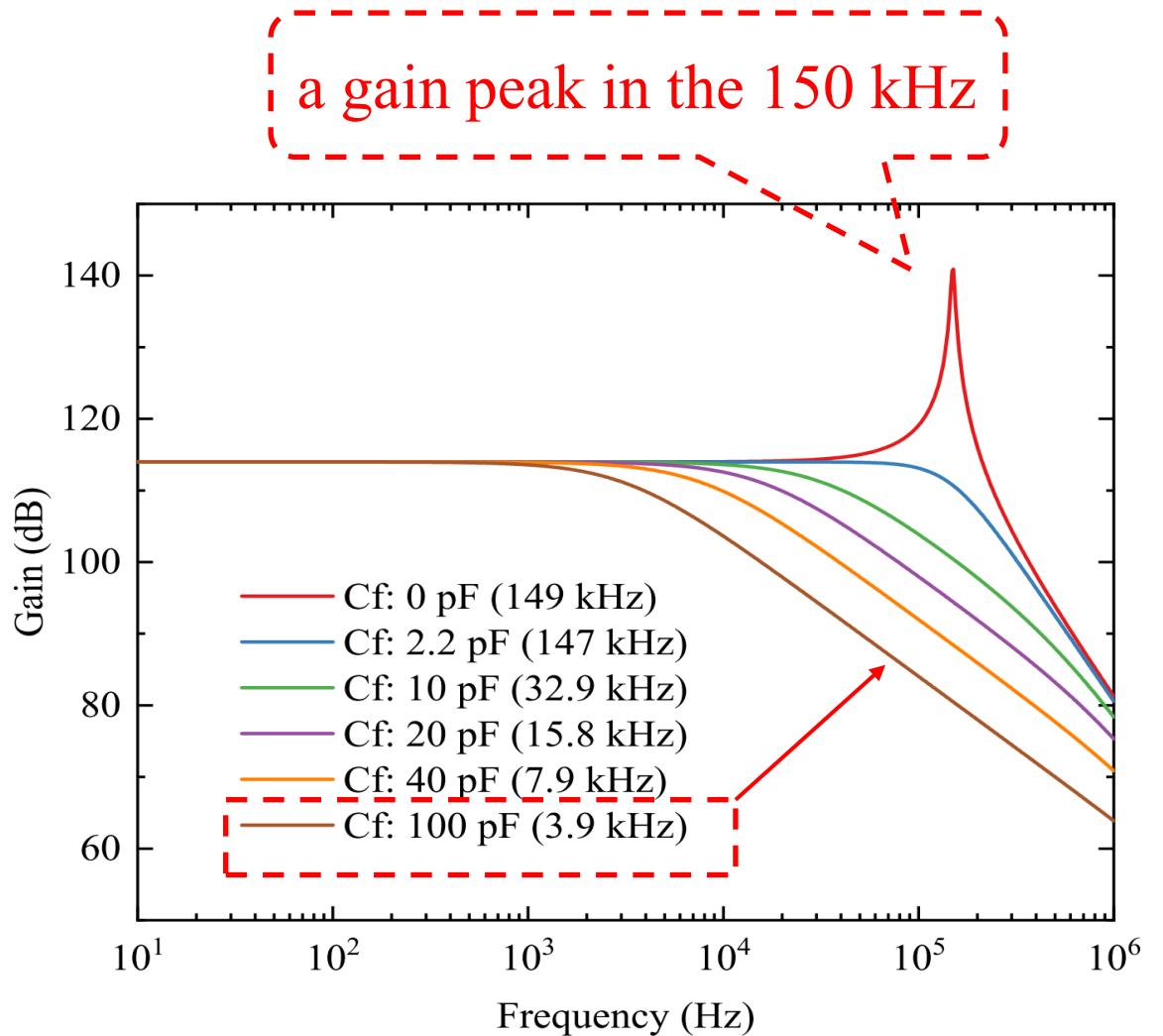
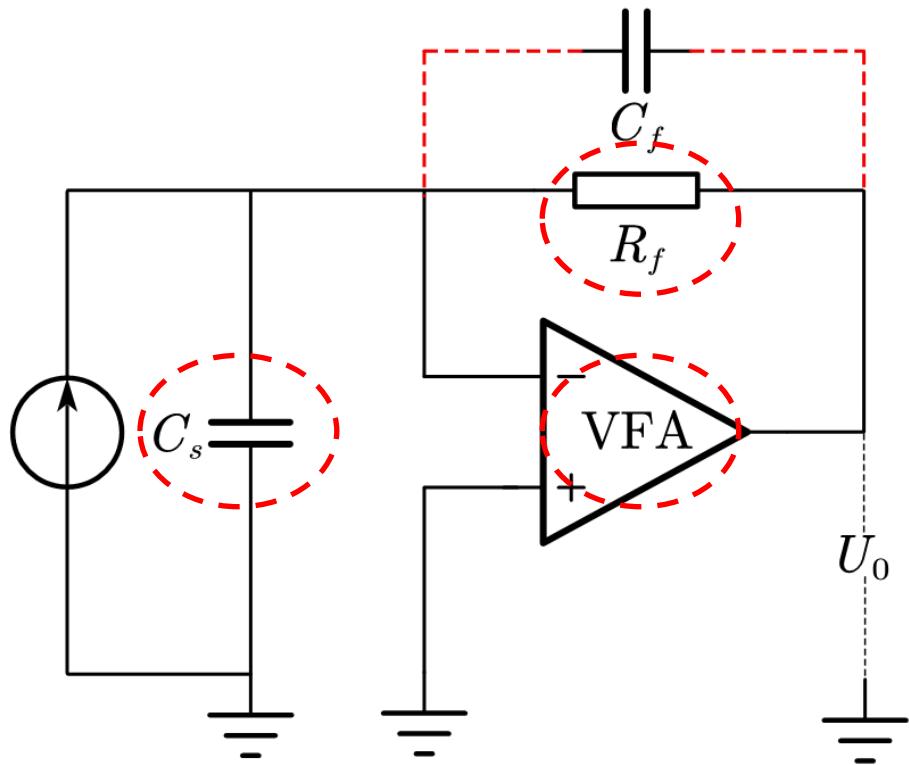
# Analog Front-end Electronics



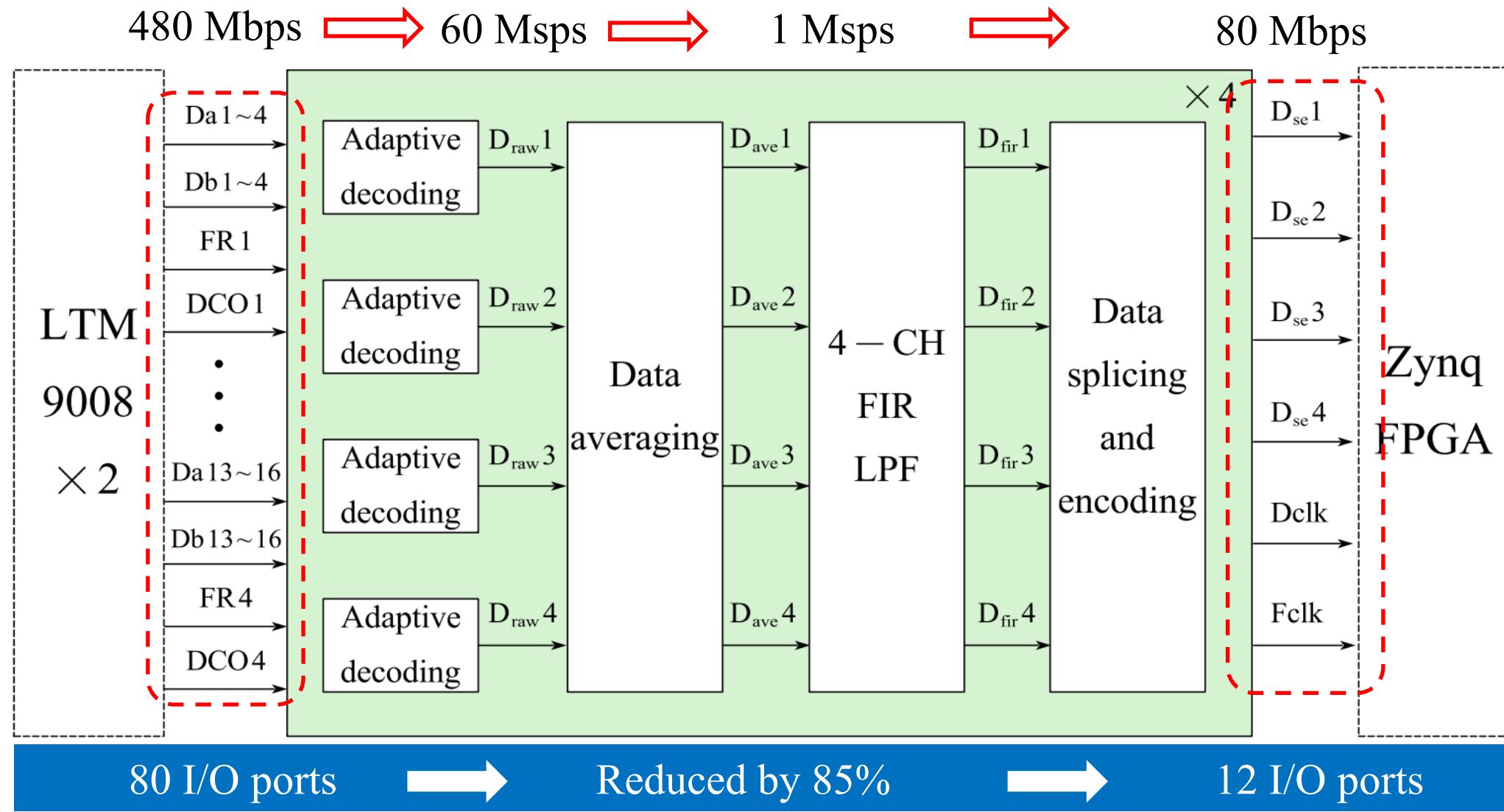
Block diagram and the PCB board diagram of the AFE

# TIA Circuit with the feedback capacitor

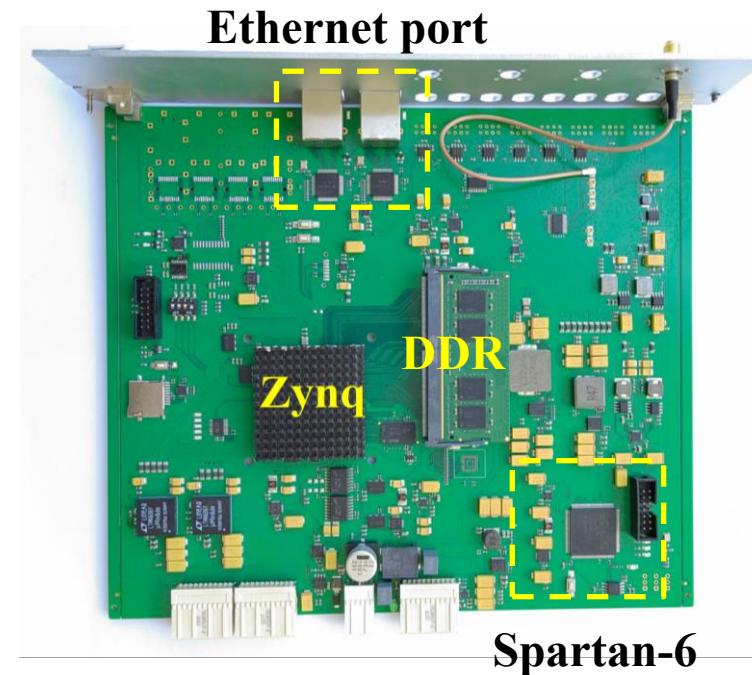
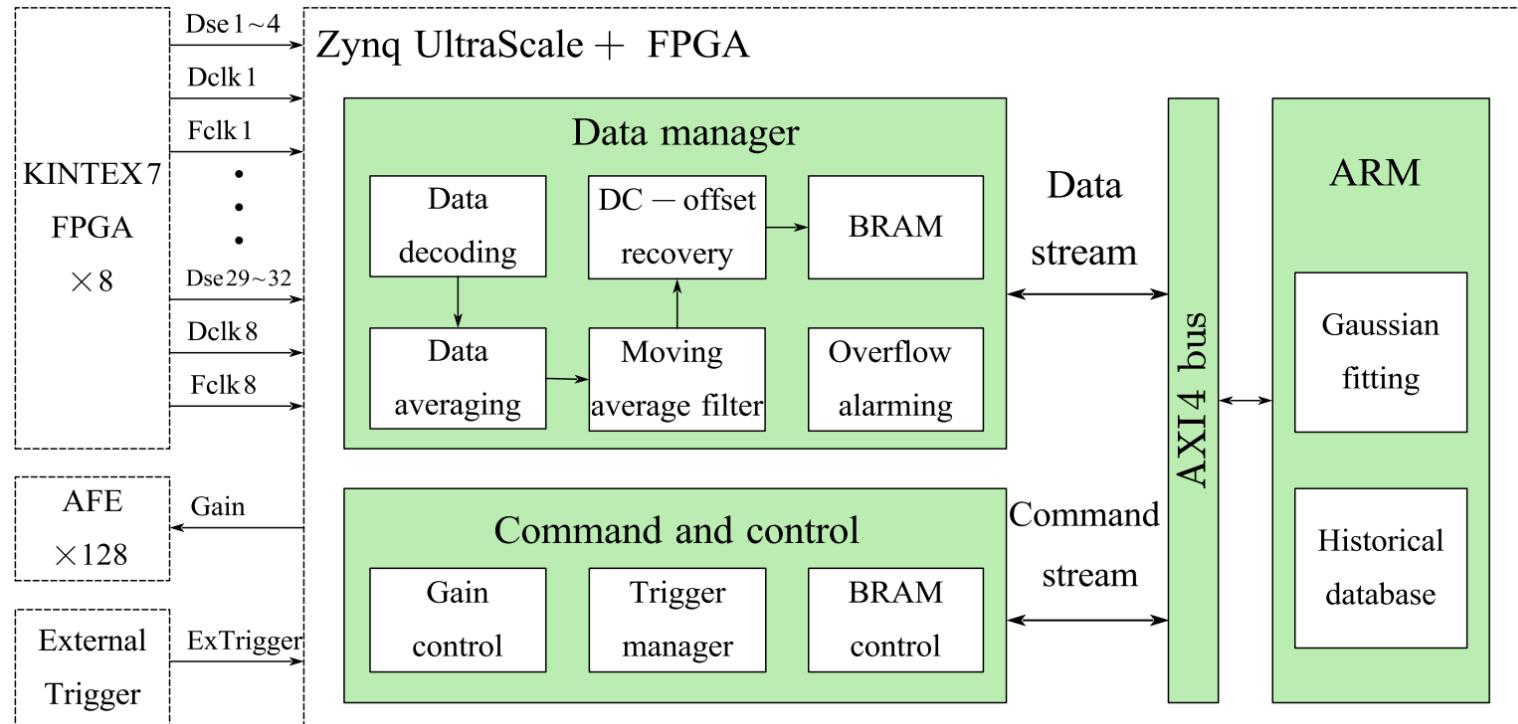
$$C_f = \frac{1}{4\pi R_f f_{GBWP}} (1 + \sqrt{1 + 8\pi R_f C_s f_{GBWP}})$$



# Firmware of the Kintex-7 FPGA

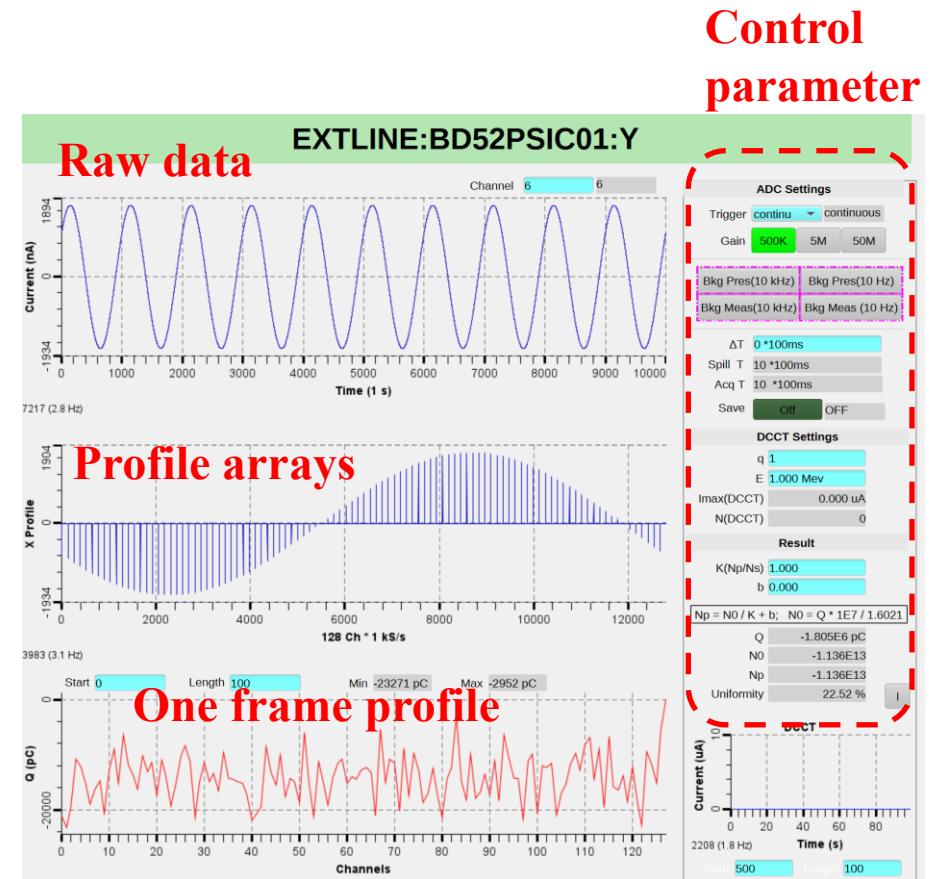
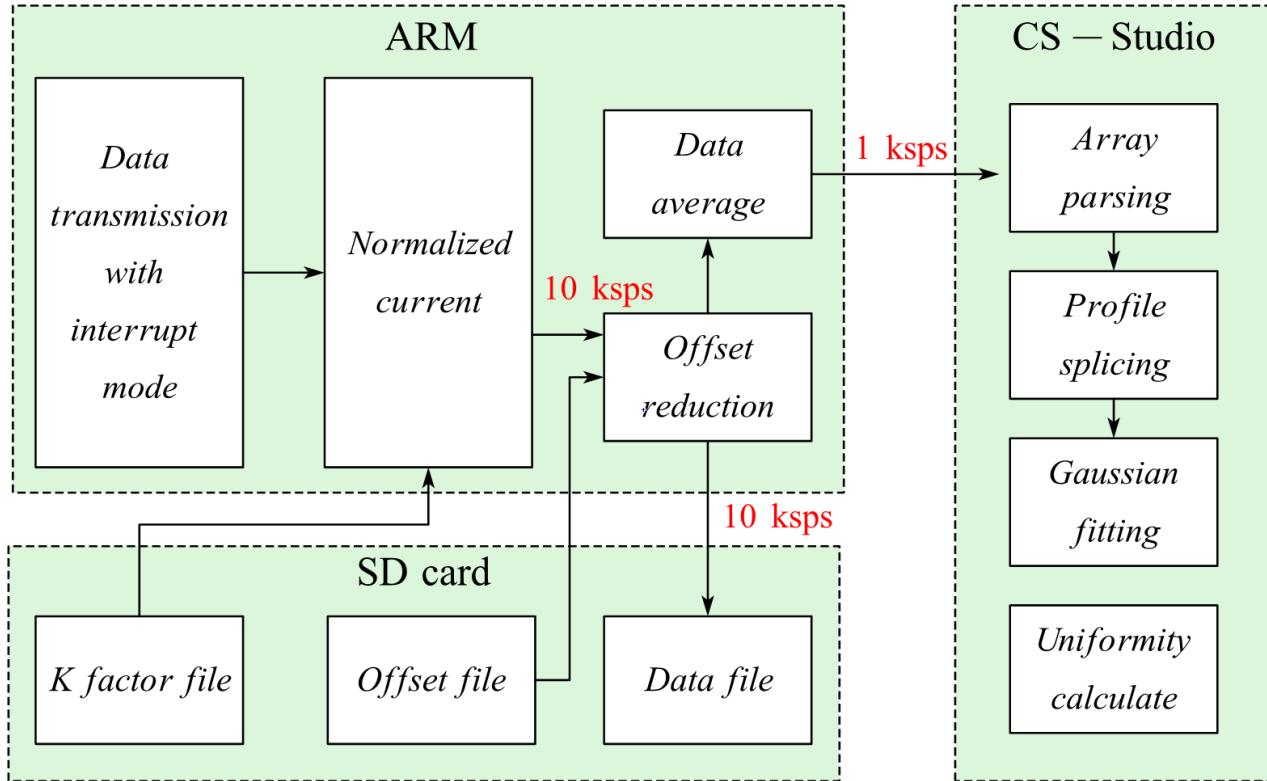


# Zynq FPGA Firmware Design



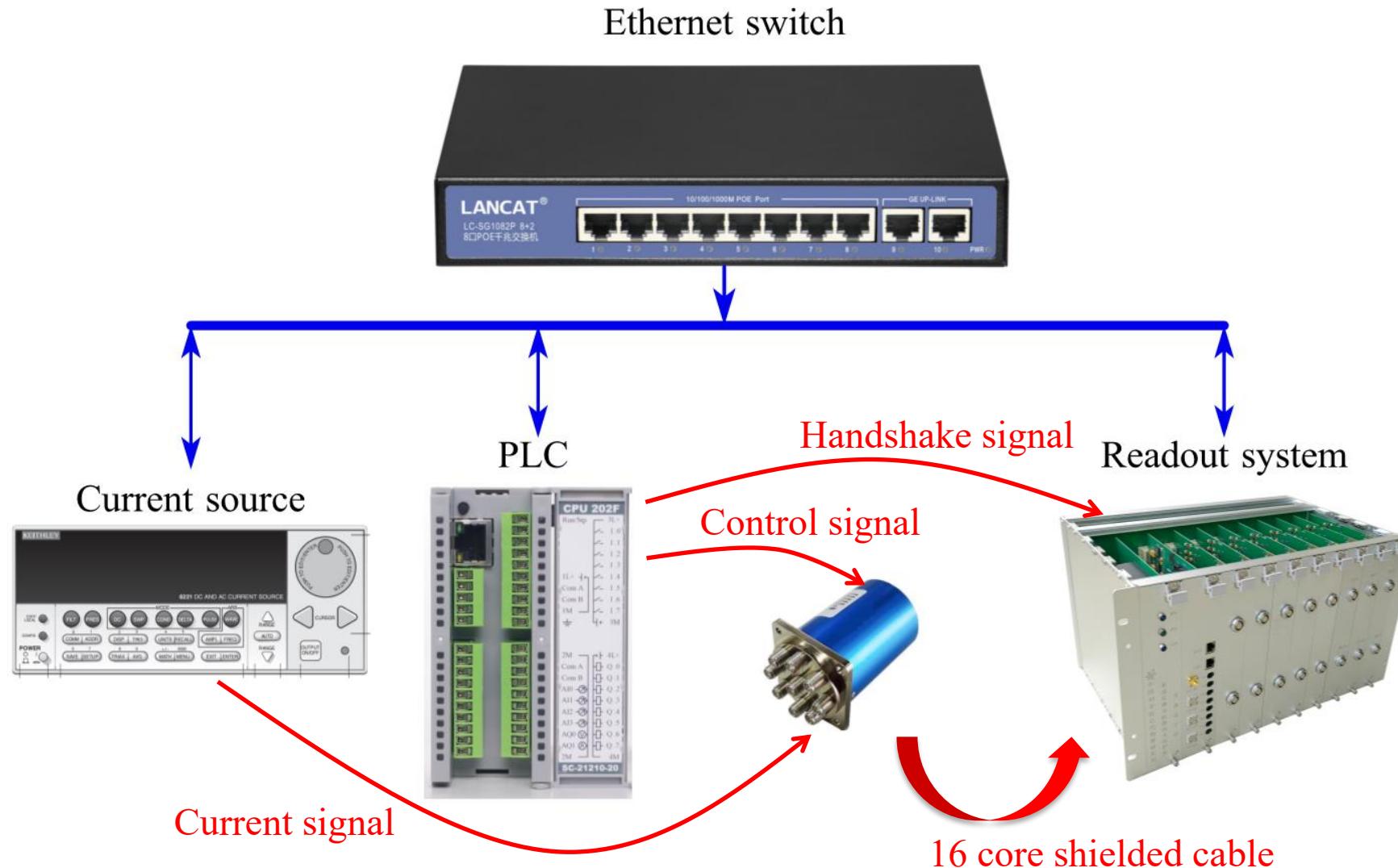
Schematic of the Zynq FPGA firmware and the PCB board diagram.

# ARM Embedded Design



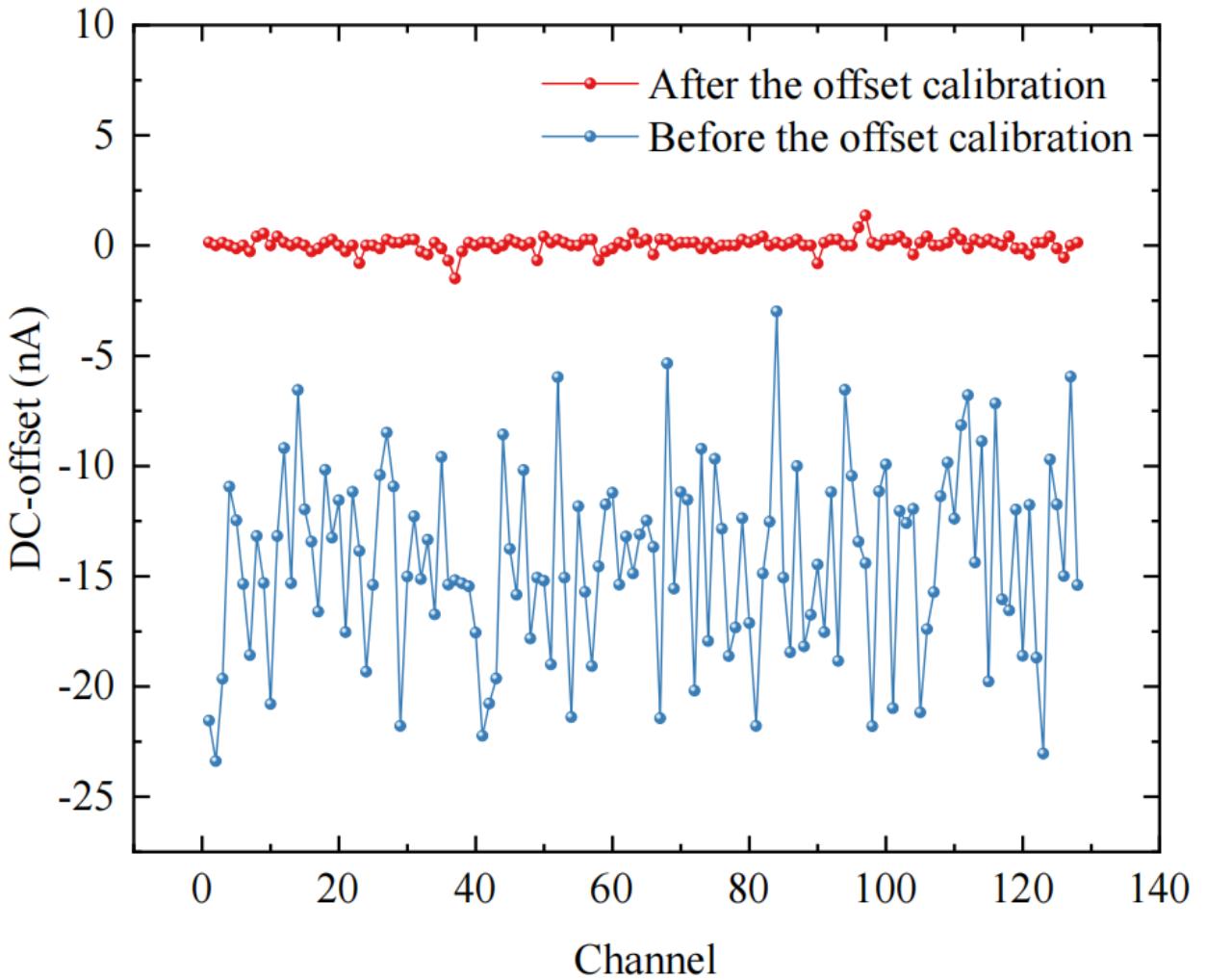
Schematic of the ARM embedded design and the graphical user interface.

# Off-line test platform



# Baseline Calibration Test

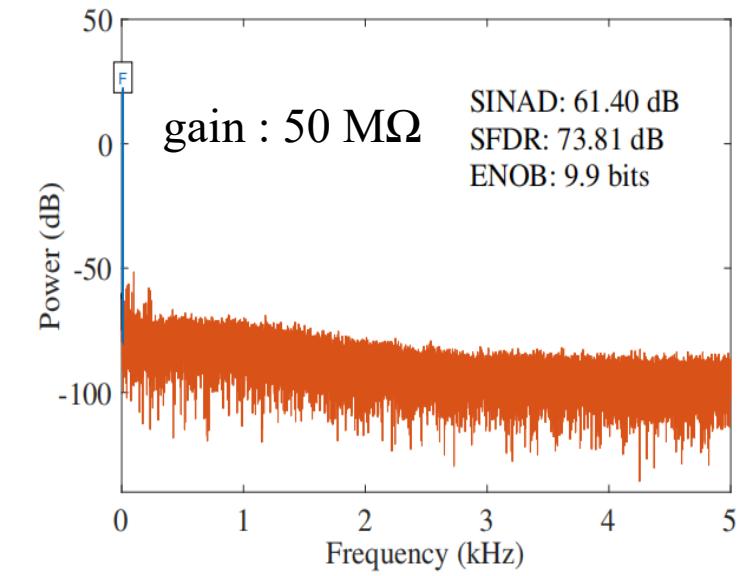
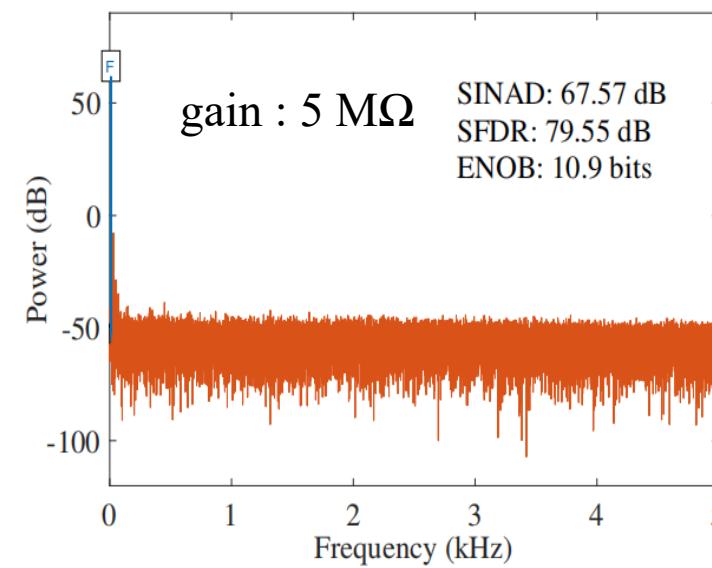
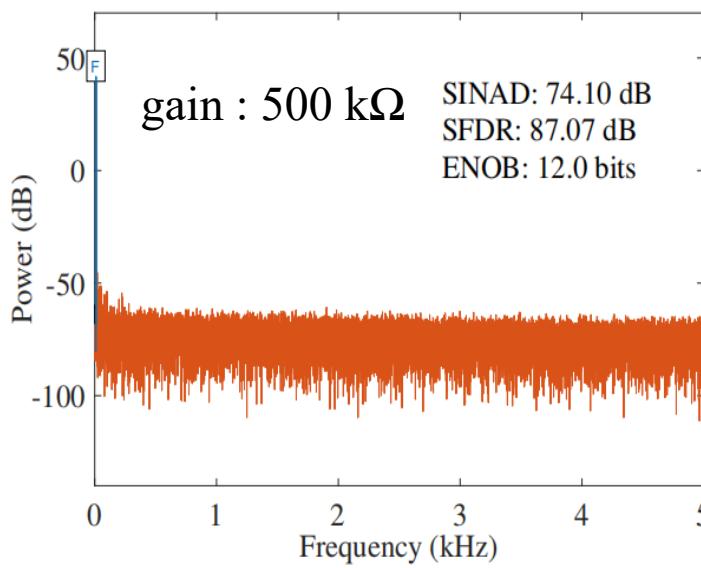
- **Mean offset :**  
-14.34 nA to 0.05 nA
- **FWHM:**  
10.01 nA to 0.75 nA.



The 128 channels' DC-offsets before and after the offset calibration.

# Effective Number of Bits Test

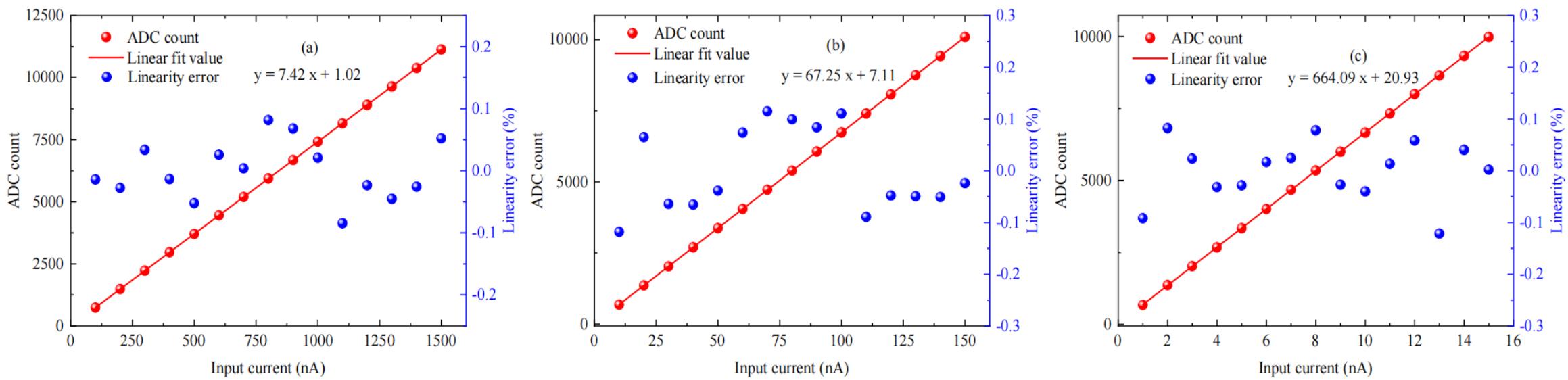
Gain	Bin width	SINAD	SFDR	ENOB
500 kΩ	0.1 Hz	74.10 dB	87.07 dB	12.0 bits
5 MΩ	0.1 Hz	65.57 dB	79.55 dB	10.9 bits
50 MΩ	0.1 Hz	61.40 dB	73.81 dB	9.9 bits



Noise spectral density of the readout electronics.

# Amplitude Linearity Test

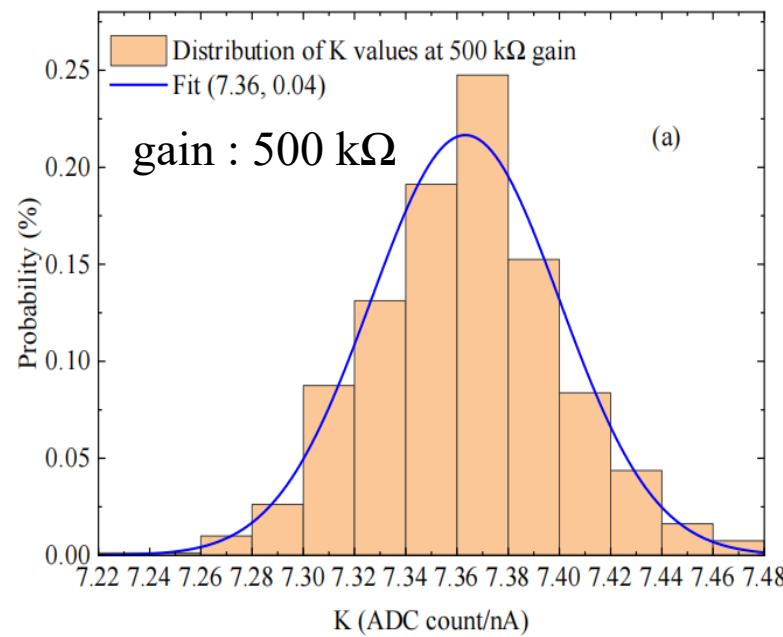
Gain	Min amplitude	Max amplitude	Step	Nonlinearity
500 kΩ	0.1 μA	1.5 μA	0.1 μA	< 0.09 %
5 MΩ	10 nA	150 nA	10 nA	< 0.11 %
50 MΩ	1 nA	15 nA	1 nA	< 0.12 %



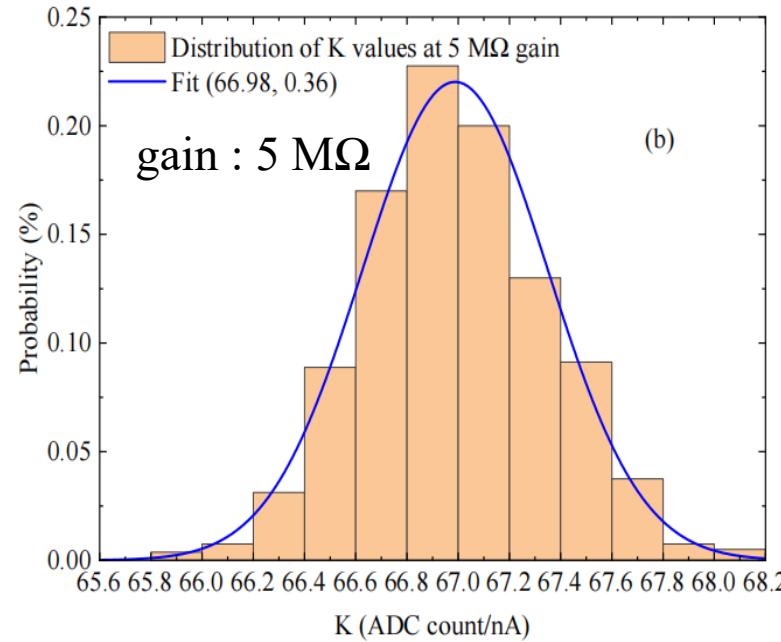
Output amplitude linearity of the readout electronics.

# Channel Consistency Test

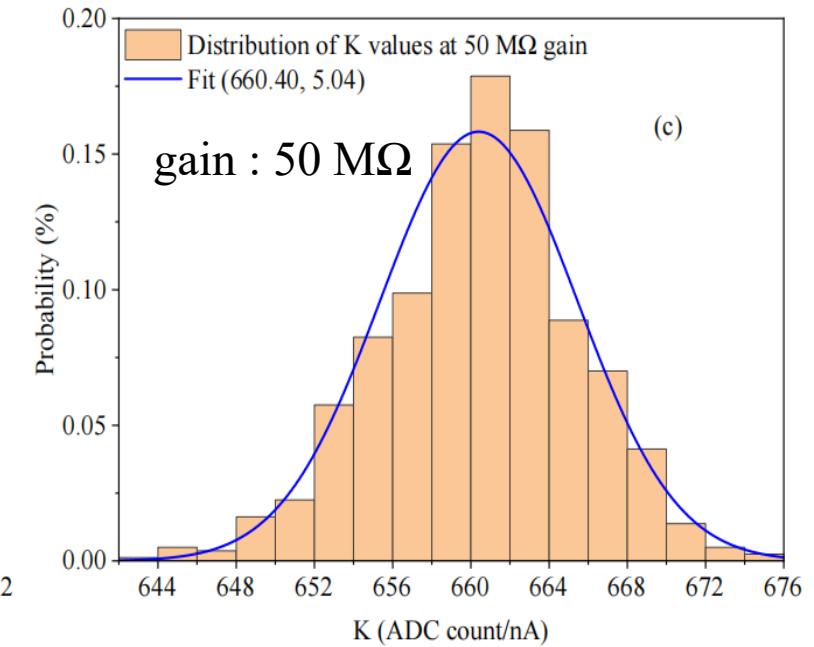
Mean : 7.36  
 $\sigma$  : 0.04



Mean : 66.98  
 $\sigma$  : 0.36



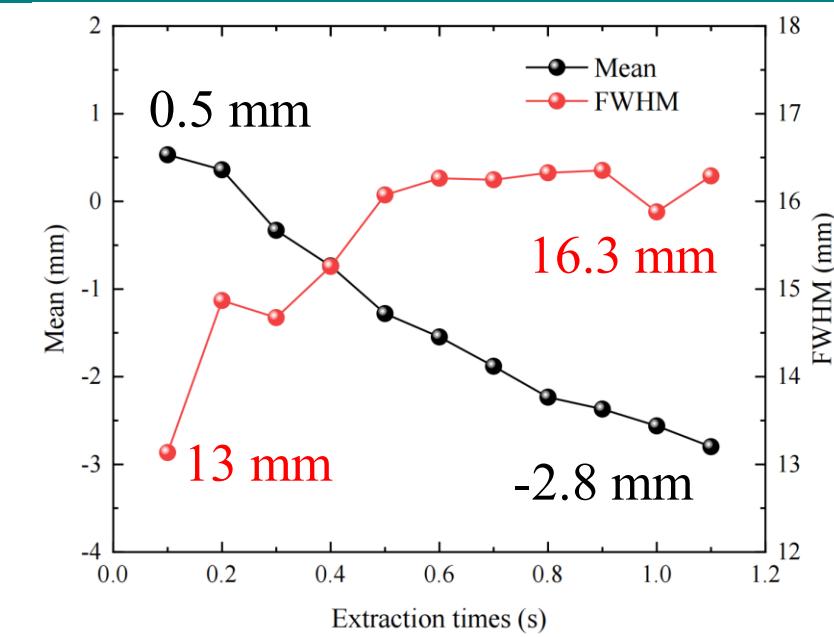
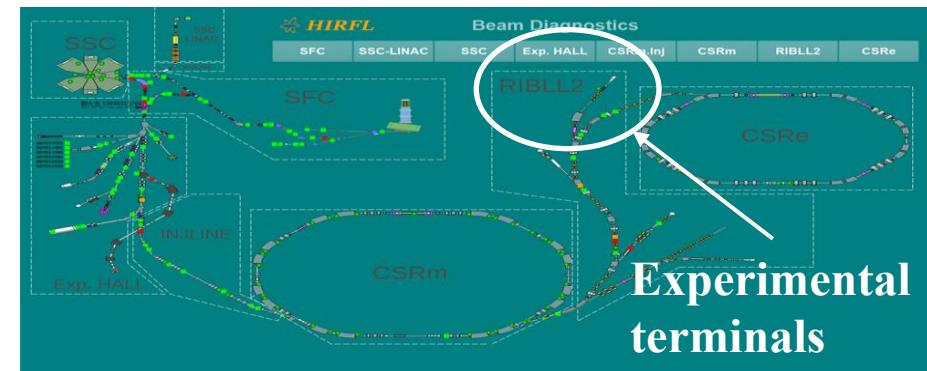
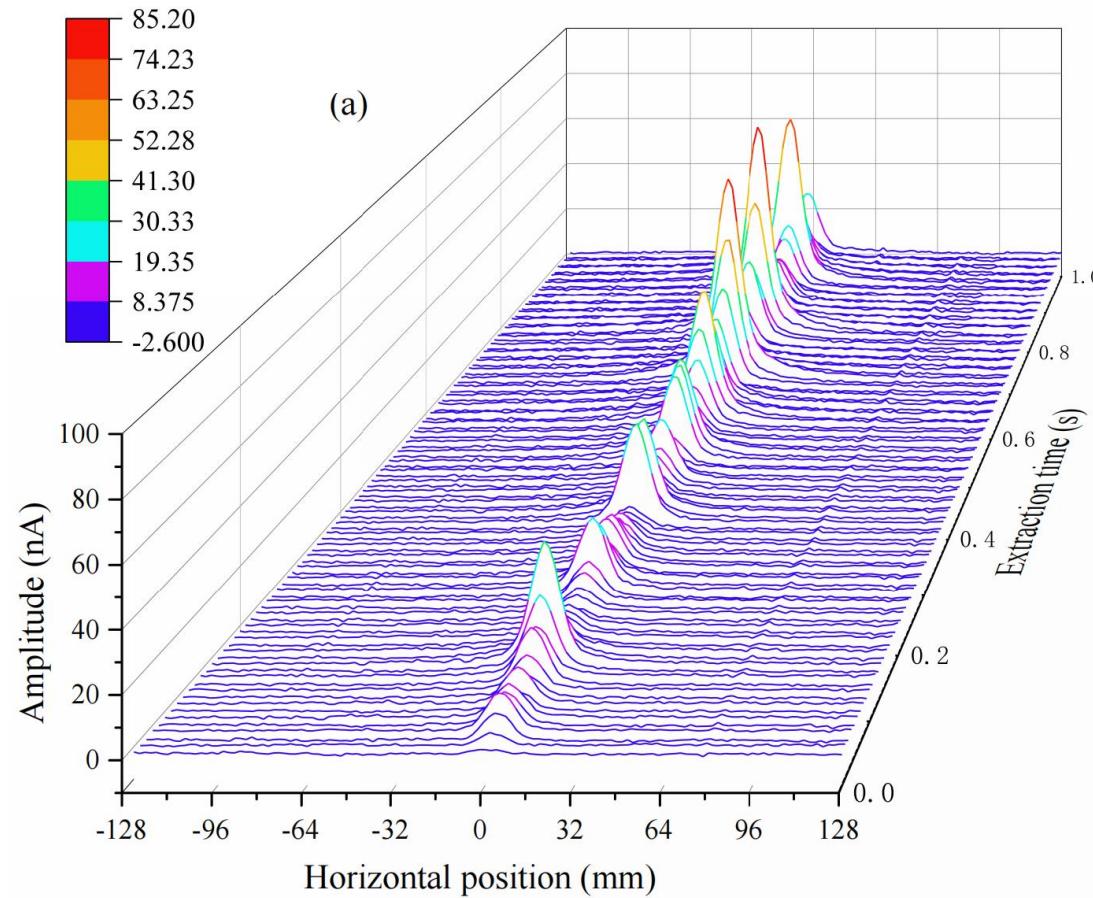
**It is Compensable!**



Statistical distribution of the K value in different gains.

# Beam Test with MSIC in HIRFL-CSR

Beam: O<sub>6+</sub>, 60 MeV/u



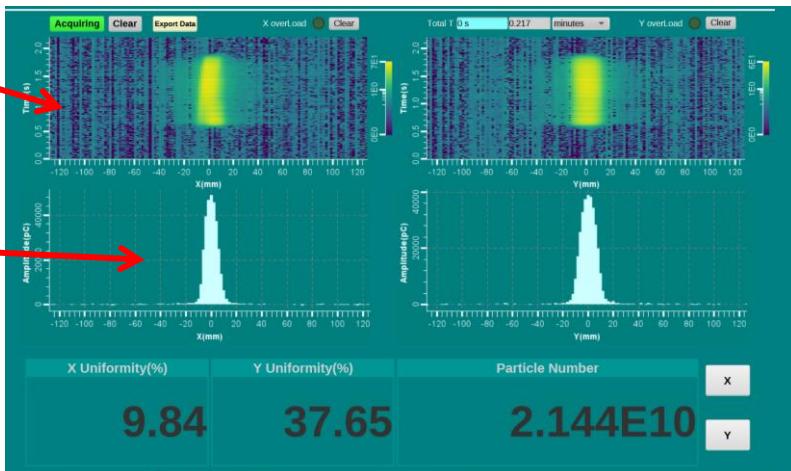
Beam profiles of the slow extraction in HIRFL-CSR.

# Beam Test in PREF - 60MeV proton beam

Unscanned beam

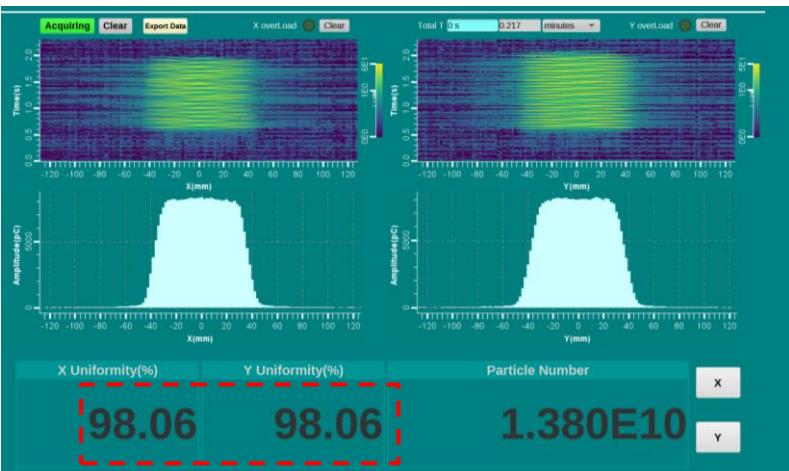
Waterfall

Profile



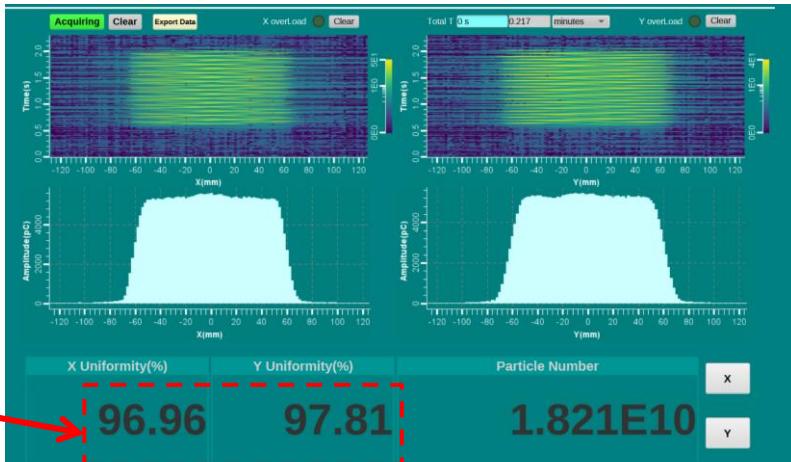
Scanning area: $50 * 50 \text{ mm}^2$

Beam current  
32.3 pA



Scanning area: $100 * 100 \text{ mm}^2$

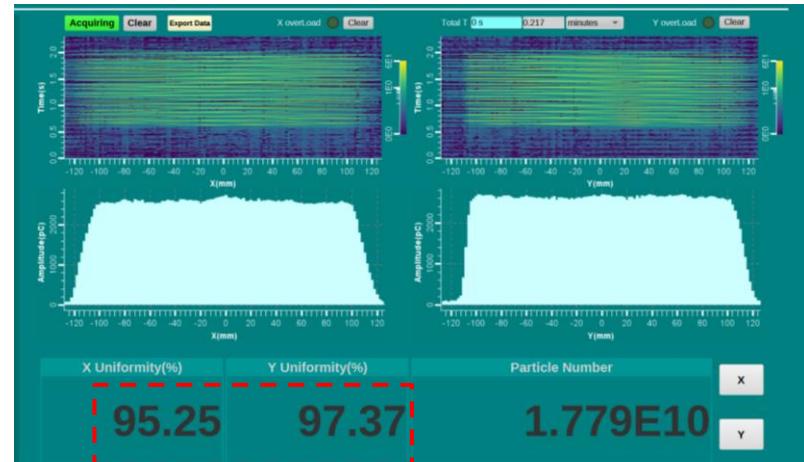
Beam current  
19.4 pA



Scanning area: $200 * 200 \text{ mm}^2$

Beam current  
9.3 pA

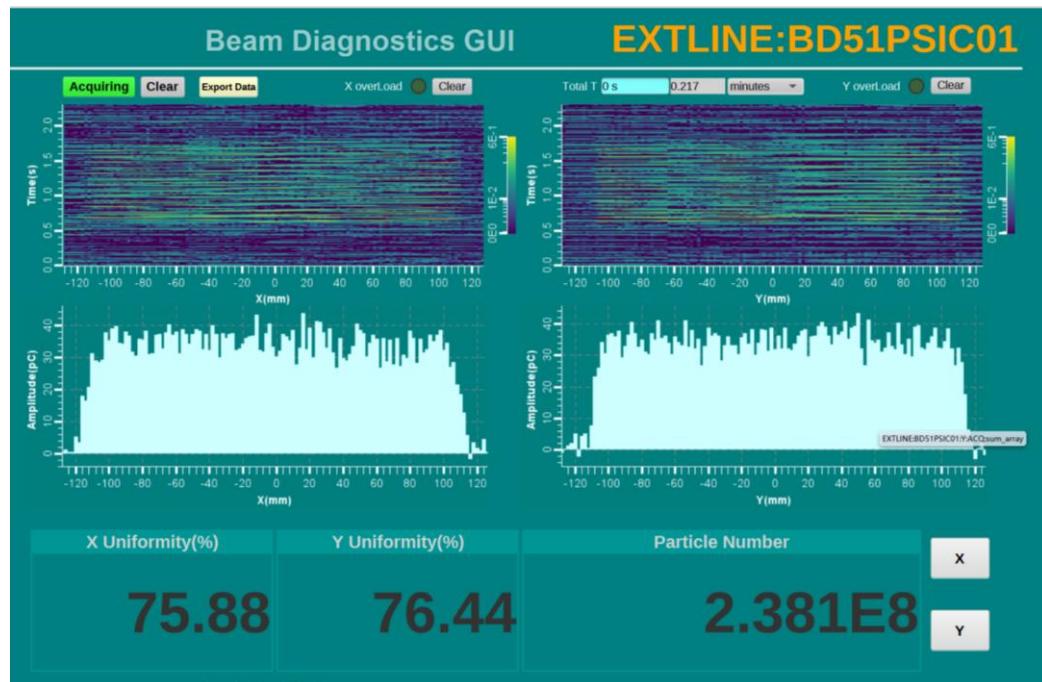
Uniformity



# Beam Test in PREF – weak beams

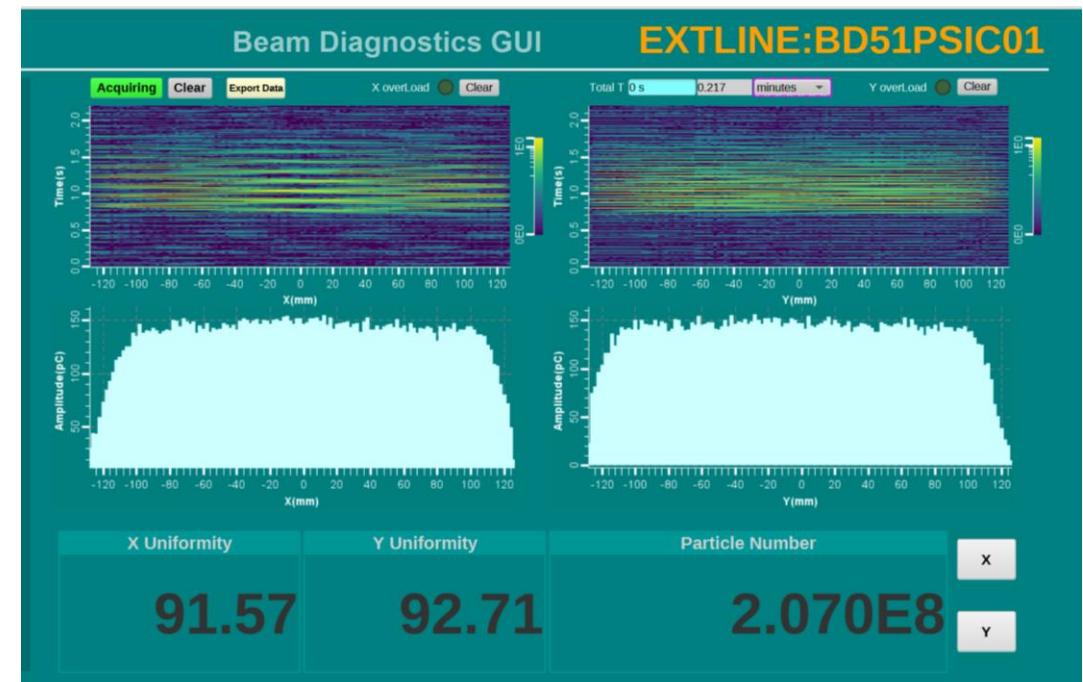
60MeV proton beam

Beam current : 0.14 pA



10MeV proton beam

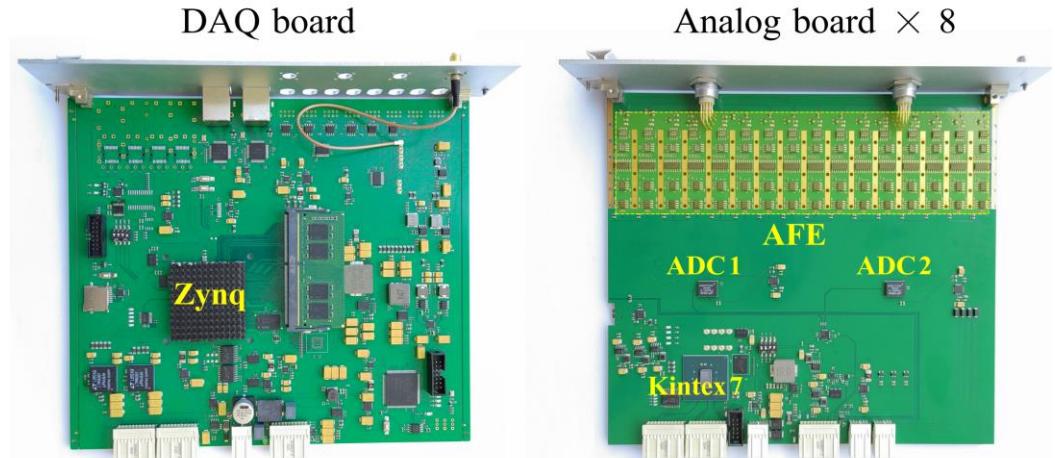
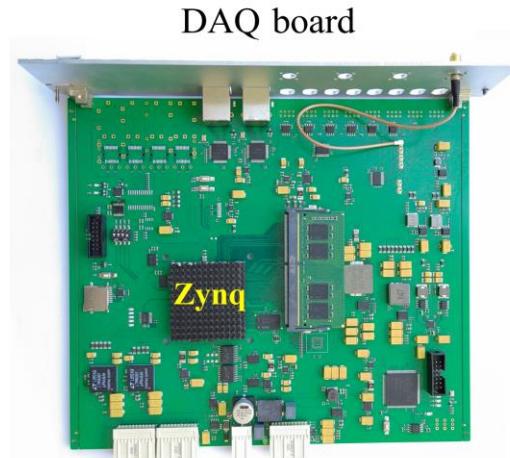
Beam current : 0.11 pA

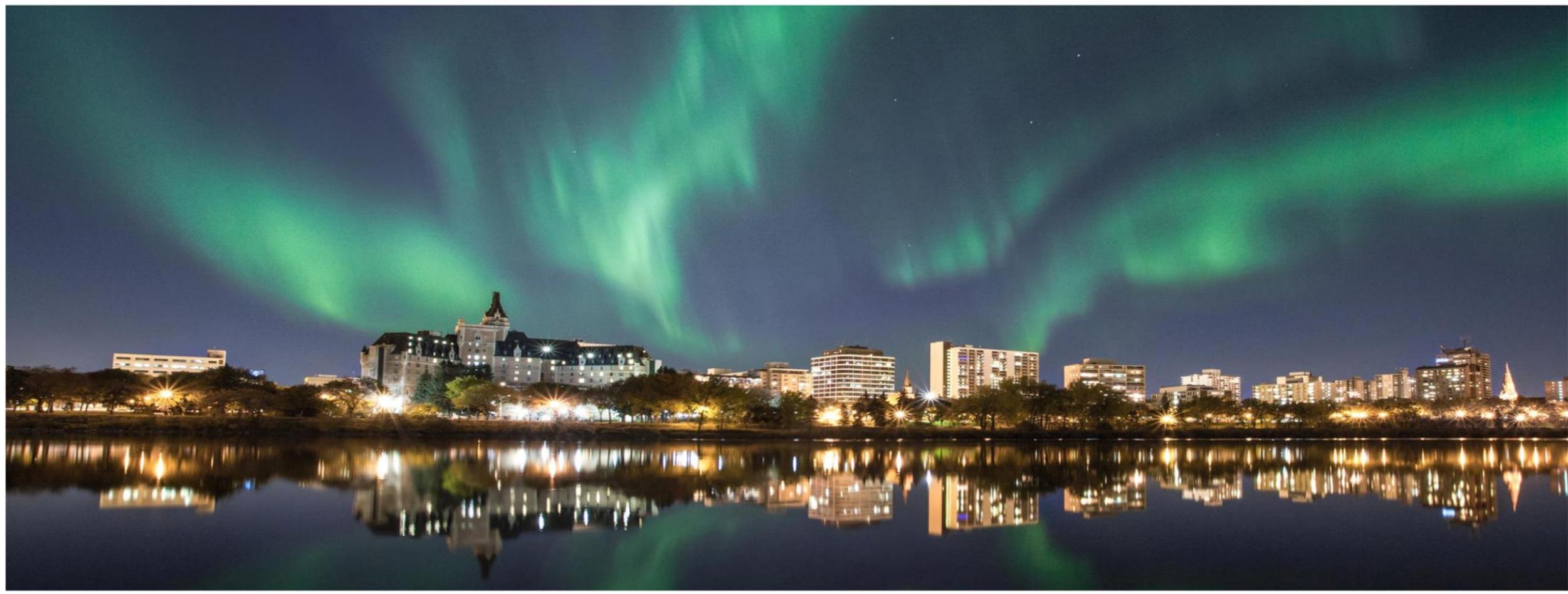


Beam profiles of the slow extraction in PREF.

# Conclusion

1. A **128-channel** readout system with **60 Msps**.
2. A new I-V converter with a high dynamic of **25 pA–1.8 μA**.
3. An adaptive decoding module to decode the **480 Mbps** serial data.
4. An automatic calibration device.
5. Extend to other **fast profile monitors**.





**Thank you for your attention!**