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STATUS OF THE RFSOC-BASED SIGNAL PROCESSING FOR MULTI-BUNCH AND FILLING-PATTERN FEEDBACKS IN THE SLS2.0*

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Abstract

Having effectively evaluated the RF System-On-Chip (RFSoC) as a suitable technology for the SLS2.0 Filling Pattern Feedback (FPFB) and Multi-bunch Feedback (MBFB) [1], our current focus lies in realizing and expanding the required real-time Digital Signal Processing (DSP) algorithms on an RFSoC evaluation board. This contribution outlines the present status of our feedback systems, including recent outcomes derived from testing prototypes both in the laboratory and with beam signals at the storage ring. [1] P. Baeta et al., "RF System-on-Chip for Multi-Bunch and Filling-Pattern Feedbacks," Proc. IBIC'22

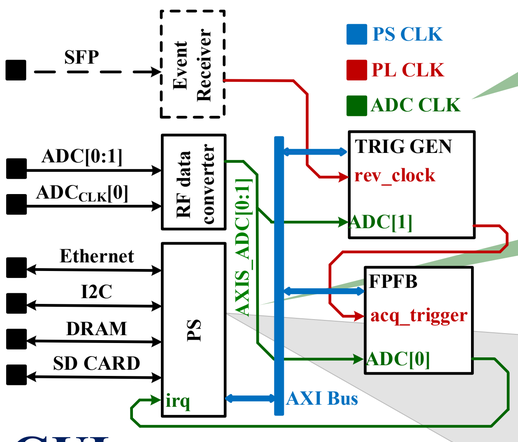
SLS 2.0 / Motivation

- Replacement of the SLS storage ring, providing up to 60-fold higher brightness for hard X-rays.
- Modernization of aging systems, including the Multi-bunch (MBFB) and Filling Pattern (FPFB) Feedback Systems.
- Xilinx RFSoC as platform to implement the MBFB and FPFB for the SLS 2.0.
- 1st SLS 2.0 beam is planned for 2025.

Filling Pattern Feedback (FPFB)

Measure the charge and the arrival time of each RF bucket. Control the injection time, adjusting the charge of each bunch given an user-defined pattern (filling pattern). Improves orbit stability (BPMs have filling pattern dependent error). Avoid HOMs (that are filling pattern dependent).

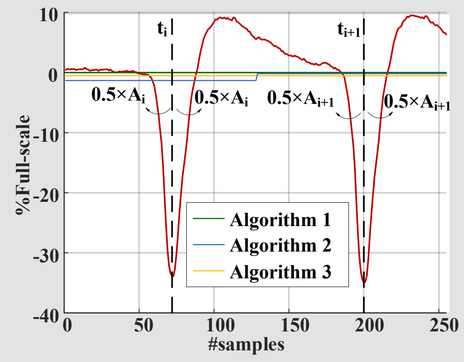
FIRMWARE



Filling Pattern ADCs run at slightly different ADC clock, to acquire a fractional number of samples per beam turn, Such that an interleaved sampling scheme increases the effective sampling rate of the ADCs from 4Gs/s to 64Gs/s.

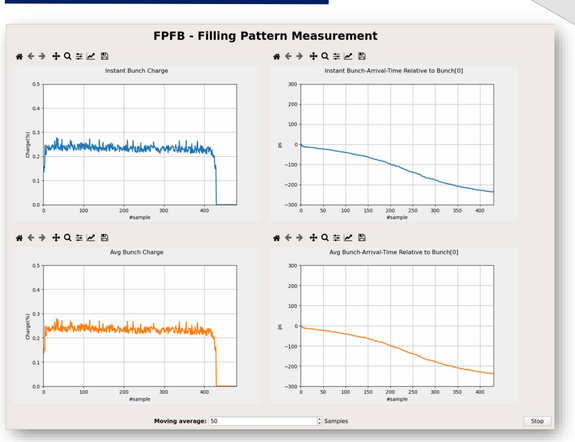
BPM sum signal (S) sampled by RFSoC ADCs and used for bunch charge & arrival time calculation.

Real-time Software

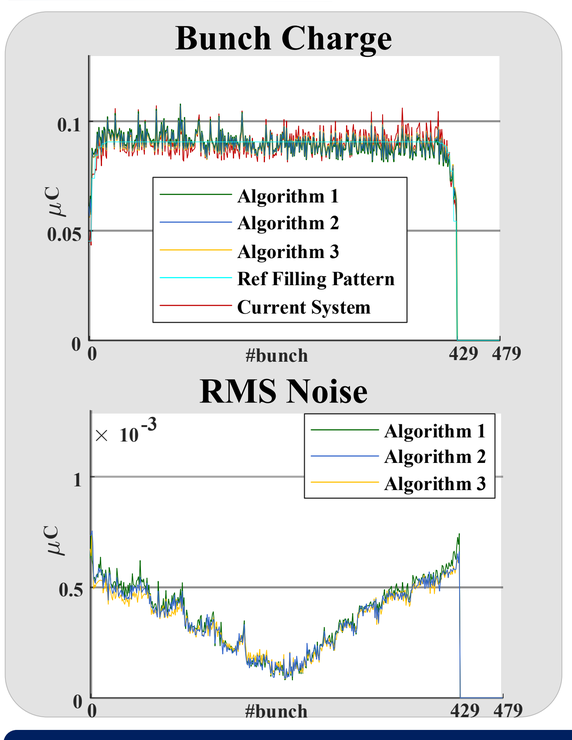


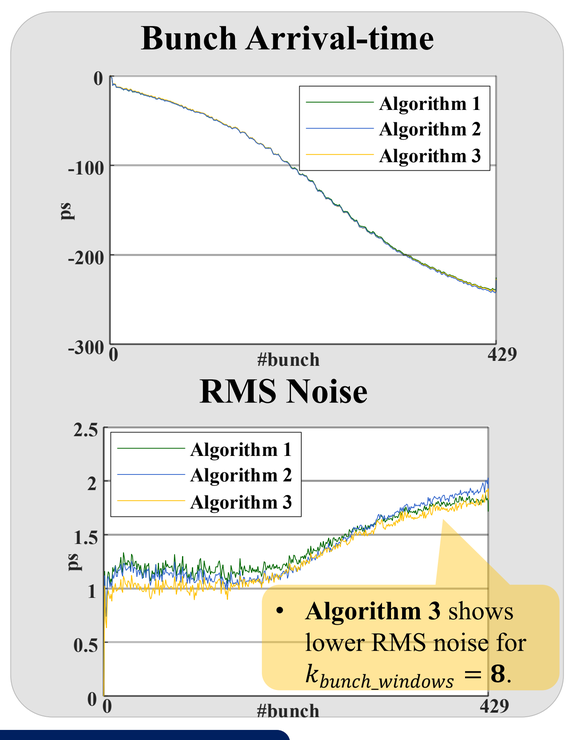
- Area A_i below dynamic baseline proportional to the bunch charge, and time t_i which splits A_i in half is an estimate for bunch arrival time.
- Algorithm 1:baseline is 0. Algorithm 2: baseline is the average of the sum signal, S, over a single bunch-window. Algorithm 3: baseline is the average of S over $k_{bunch\_windows}$ bunch-windows.

GUI



RESULTS



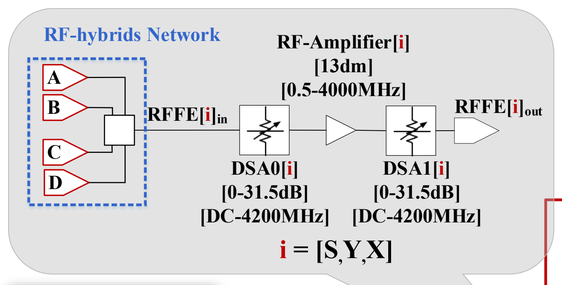


- **Algorithm 3** shows lower RMS noise for $k_{bunch\_windows} = 8$.

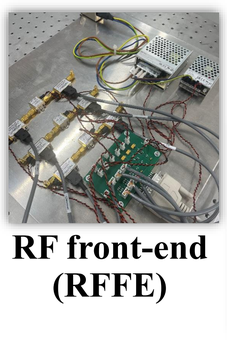
Outlook & Next Steps

- Finalize the transition towards direct (mixer-free) sampling of the BPM signals by adding adjustable delay lines to the RFFE, and interleaving multiple ADC channels; Implementing a digital solution for data acquisition that accounts for the phase slippage of the bunches on the bunch train, guaranteeing the correct position signal detection (bunch pulse detection).
- For the MBFB Longitudinal plane, we foresee an replacement of the analog upconverter (baseband to 1.5 GHz conversion) with a digital solution (interleaved DACs), for driving the kicker amplifiers.
- Add advanced diagnostics features to the MBFB, such as: excitation-damping measurements, tune measurement, automatic parameter tuning.
- Test closed-loop performance of the MBFB and FPFB systems at SLS and SLS 2.0.

Hardware

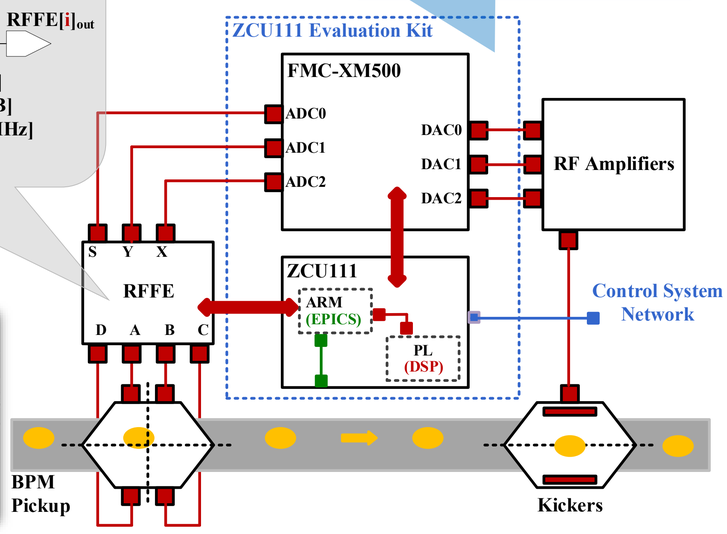


- 8 x 12-bit ADC @ 4Gs/s
- 8 x 14-bit DAC @ 6.5Gs/s



RF front-end (RFFE)

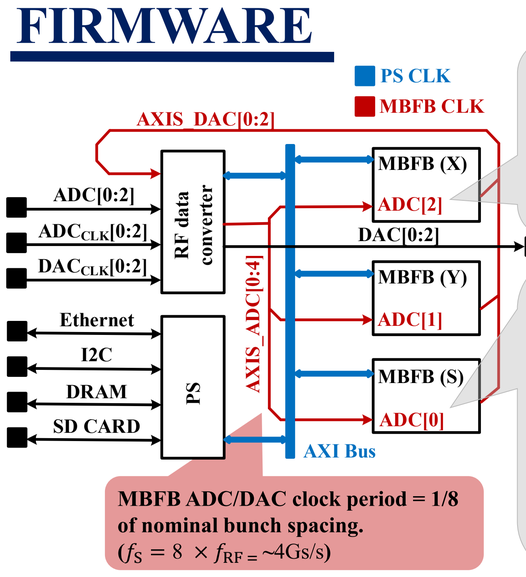
ZCU111



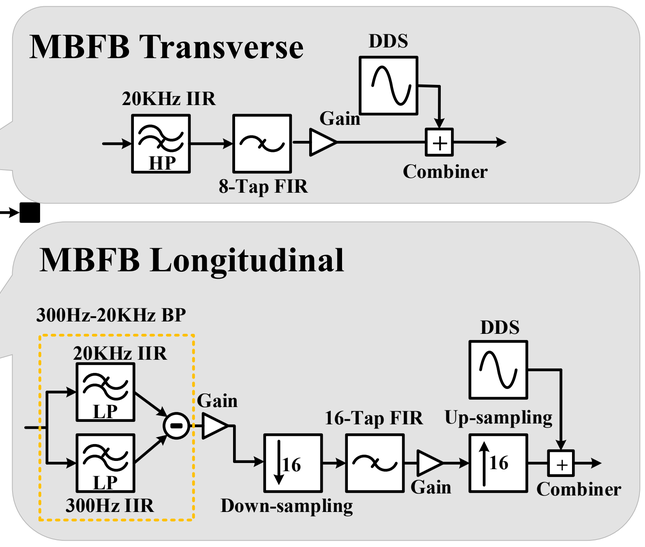
Multi-Bunch Feedback (MBFB)

Stabilize beam and avoid beam loss due to coupled-bunch instabilities (ion instabilities, resistive wall impedance, cavity HOM, etc.). Diagnostic tool: Identify source of beam instabilities; Excitation-damping measurement; Parasitic (X/Y/S) tune measurement.

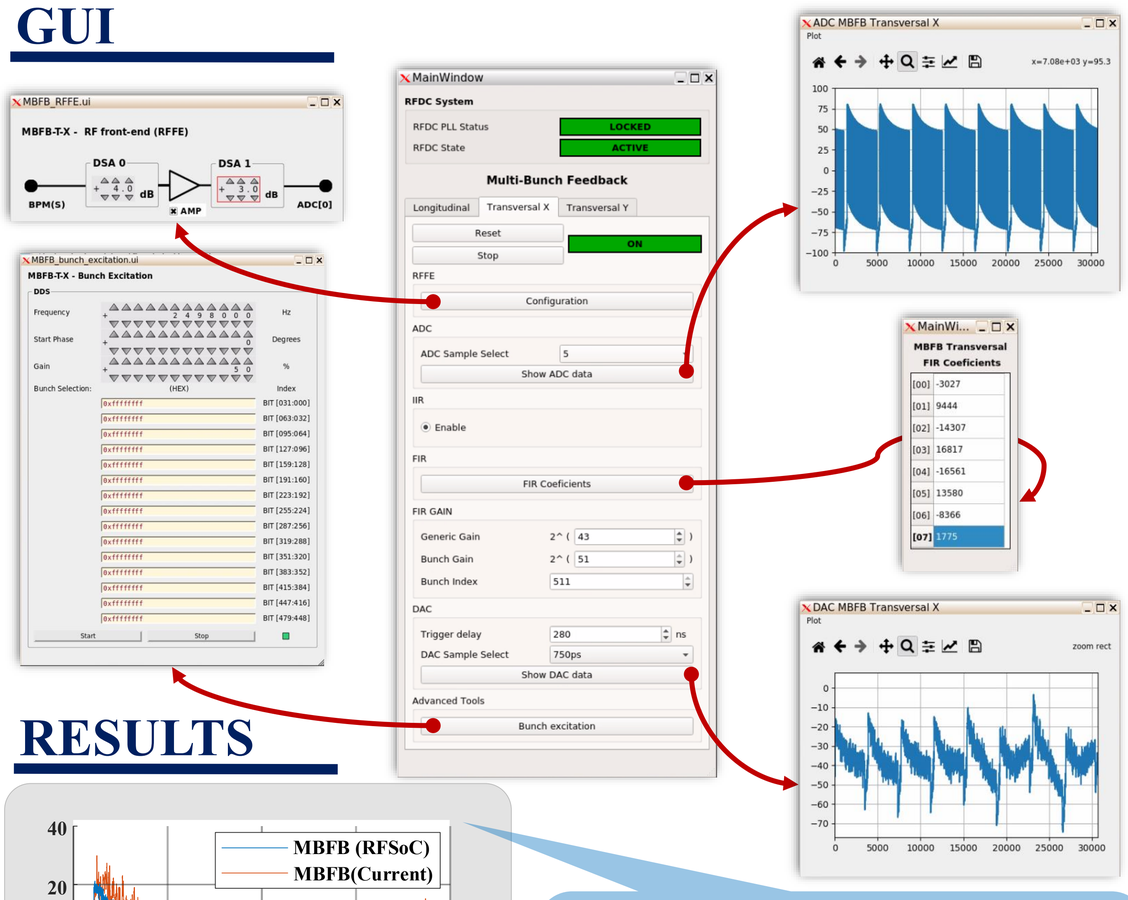
FIRMWARE



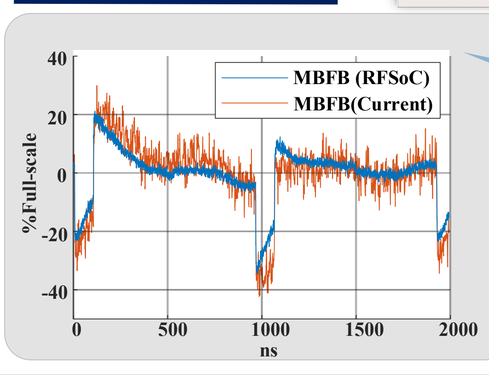
MBFB ADC/DAC clock period = 1/8 of nominal bunch spacing. ($f_S = 8 \times f_{RF} = \sim 4$Gs/s)



GUI



RESULTS



- Comparison of the open-loop response of the horizontal plane of the existing MBFB hardware versus the RFSoC-based prototype. The improved ADC and DAC resolution of the RFSoC significantly improved the noise of the DAC response.