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STATUS OF THE RFSoC-BASED SIGNAL PROCESSING FOR MULTI-BUNCH AND FILLING-PATTERN FEEDBACKS IN THE SLS2.0

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Abstract

Having effectively evaluated the RF System-On-Chip (RFSoC) as a suitable technology for the SLS2.0 Filling Pattern Feedback (FPFB) and Multi-bunch Feedback (MBFB), our current focus lies in realizing and expanding the required real-time Digital Signal Processing (DSP) algorithms on an RFSoC evaluation board. This contribution outlines the present status of our feedback systems, including recent outcomes derived from testing prototypes both in the laboratory and with beam signals at the storage ring.

INTRODUCTION

The Swiss Light Source (SLS), a 3rd generation synchrotron light source at Paul Scherrer Institute (PSI), will be upgraded by a cutting-edge storage ring magnet lattice with reverse bends. The new machine, the SLS2.0, will provide a much lower emittance and higher beam energy, ultimately increasing the hard X-ray brightness and making the SLS competitive with other newer facilities [1]. Moreover, upgrading the SLS includes modernizing aging systems, such as the multi-bunch feedback (MBFB) and the filling pattern feedback (FPFB). After we assessed the suitability of RF System-On-Chip (RFSoC) for implementing the MBFB and FPFB of SLS 2.0 [2], we proceeded with deploying the feedback systems on the ZCU111 evaluation board from Xilinx/AMD, which features an RFSoC [3]. In the hardware section of this paper, we present an overview of the set-up installed at the SLS for testing the new MBFB and FPFB designs, which includes an RF-front-end (RFFE) prototype and the RFSoC-based digital back-end. The subsequent Firmware and Software section covers a real-time implementation of bunch-charge and arrival-time measurement for the FPFB, along with DSP firmware upgrades in the MBFB design. Lastly, we report prototype results from testing RFSoC-based systems in the laboratory and at the SLS storage ring, utilizing RF beam position monitor (BPM) signals.

HARDWARE

Figures 1(a) and 1(b) depict a block diagram of the hardware set-up at the SLS storage ring for prototyping our RFSoC-based solution of the FPFB and MBFB systems. The signals from four capacitive electrodes of an SLS beam position monitor (BPM) are connected to an RF hybrid network, yielding the sum signal (S), proportional to the bunch charge, and the difference signals (X and Y), proportional to the bunch charge and the horizontal and vertical bunch position offsets. The RFFE module consists of digital step attenuators (DSAs) and RF amplifiers for conditioning the position signals S, X, and Y. Figure 1(a) presents the signal conditioning path for each of the three MBFB planes. The RFFE prototype has a bandwidth of approx. 1000 MHz, online user-controllable gain/attenuation adjustments, and on/off switching capabilities for each analog signal conditioning path. The previous MBFB at SLS1.0 used a commercial RFFE that down-converted BPM signals from 1.25-1.5 GHz to the baseband. The new RFFE represents a transition toward direct sampling of S, X, and Y signals. The digital back-end in Figure 1(b) comprises the ZCU111 evaluation board and two interface boards. The ZCU111 is the core of the feedback systems, performing the data acquisition and processing. The Xilinx/AMD FMC-XM500 card breaks out the nets of the RFSoC data converters of the ZCU111. The ADCs acquire the conditioned signals S, X, and Y from the RFFE. The ZCU111 can control the RFFE signal gain and power with a second adapter board. In the context of the MBFB, the DACs generate the correction signals, closing the feedback loop. The correction signals undergo amplification, including upconversion to 1.5 GHz in the longitudinal plane, before driving the MBFB kickers. As for the FPFB, embedded real-time software processes the sum signal (S), calculating bunch charge. This process concludes by providing injection control information across successive top-up cycles, as needed, to close the filling pattern feedback loop.

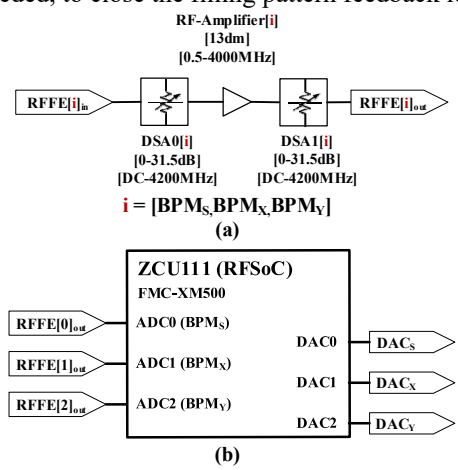

Figure 1: Block diagram of the FPFB and MBFB hardware set-up. (a) RF Front-end (RFFE) module for conditioning position signals from the SLS beam position monitor (BPM). (b) The Digital back-end module incorporates the ZCU111 evaluation board for data acquisition, processing, and communication with the SLS control system.

FIRMWARE AND SOFTWARE

Figures 2 and 3 illustrate the firmware block diagrams for the FPFB and MBFB systems implemented on the RFSoC platform. The Xilinx RF Data Converter is the core IP of the design. This IP configures the ADCs and DACs of the RFSoC and establishes the AXI stream data interface

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of each converter with the programmable logic (PL) [3]. The EPICS IOC, operating on one of the two ARM CPU of the RFSoC processing system (PS), handles the configuration and data transfer between the feedback and SLS control systems via an Ethernet interface. The PS and PL interfaces include AXI bus and PL to PS interrupts. The I2C bus controls the on-board PLLs, which define the clock frequency of the RFSoC converters. The reference clock of the design is received from the master generator for the SLS storage ring high-power RF systems (f_{RF} =~500 MHz). For the MBFB system, all data converters run in multi-tile synchronization (MTS) mode, guaranteeing temporal sample alignment among ADCs and DACs and reproducible latency from ADC to DAC after a power cycle. The PL clock and data converter clocks in the MBFB firmware design are synchronized to the external reference clock and, thus, to the electron beam revolution frequency. In the FPFB design, the ADCs and PL operate in different clock domains, realizing an interleaving scheme to increase the effective ADC sample rate.

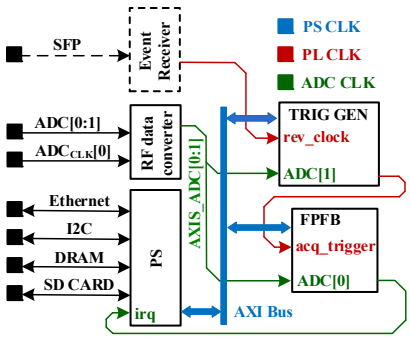

Figure 2: Firmware block diagram of the RFSoC-based FPFB system.

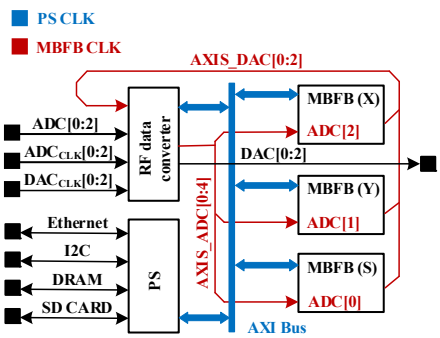

Figure 3: Firmware block diagram of the RFSoC-based MBFB.

Filling Pattern Feedback (FPFB) Systems

There are substantial changes in the firmware/software implementation compared to the design presented in Ref. [2]. The current FPFB firmware consists of a data-acquisition block that records the input data stream of the ADC0 running at a sampling frequency, f_S. The harmonic number of the SLS ring is 480, and the SLS machine reference clock, f_{RF}, is approximately 500 MHz. For $f_S = 8 \times f_{RF}$, the number of samples per bunch is 8, and per turn is $N = 8 \times 480$. To increase the effective sampling rate of the ADC0 by a factor of M, f_S is set such that a fractional number of samples per turn is acquired, and the data of M turns is interleaved.

$$f_s = \frac{f_{RF} \times 8 \times (M \times N - 1)}{(N \times M)} \quad (1)$$

In our prototype system, the interleave factor M is 16, resulting in an effective sampling rate of ~ 64 Gs/s.The ADC0 samples the sum signal, S, which contains the bunch charge and arrival-time information. The trigger generator IP controls the data acquisition, providing a periodic trigger, $acq\_trigger$, with a period of ~ 960 ns (480 bunches, or one beam turn) and synchronized with the machine revolution clock. The $acq\_trigger$ is the reference for bunch indexing. The data corresponding to bunch zero is the first eight samples after the rising edge of $acq\_trigger$, and bunch 479 is the last eight samples before the acquisition of a new turn. After acquiring the sum signal, S, over 16 turns, the ADC0 data stream is stored in a BRAM in PL, and the data-acquisition block generates an interrupt request, irq, to the Zynq UltraScale+ MPSoC Processing System (PS) [3]. The PS is connected to the memory block in the PL via the AXI bus and the Xilinx AXI BRAM controller IP. The real-time software for the FPFB, implemented in C, runs on the RPU0 CPU of the PS. The interrupt request, irq, starts the interrupt handler function. First, the raw data of the 16 turns is read from the BRAM and interleaved, resulting in one interleaved turn. The data of the interleaved turn is split into 480 bunch windows of 2 ns (or 128 samples).

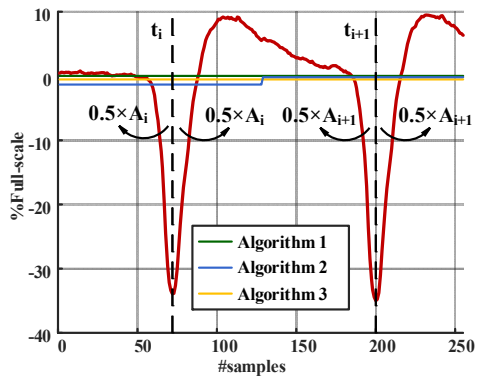

Figure 4: Sum signal, S, for two bunch windows of 2 ns, illustrating bunch pulses of the bunch train. The area A_i between the negative pulse (red curve) and the baseline (blue, yellow, and green curves) is used to estimate the charge of the bunch b_i. The Time t_i, which splits A_i in two equal parts, is an estimate for the arrival time of b_i.

Figure 4 shows the sum signal, S, for two bunch windows. For each bunch window, A_i, is the area between the negative pulse, the red curve, and the baseline. We considered three different algorithms for baseline calculation. The first algorithm, the green curve, defines the baseline as zero. In the second algorithm, the baseline is the average of the sum signal, S, over a single bunch window. In the third algorithm, the baseline is the average value of the sum signal, S, over the interval of $k_{bunch\_windows}$ bunch windows defined by the user, aiming to reduce the effects of

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baseline fluctuations on the ADC recordings. The charge of a bunch b_i , with index i , is the calculated area A_i times a common factor k_{charge} which translates area, A_i, into bunch charge in Coulombs. The bunch arrival time of b_i is the time t_i, which splits the area, A_i, equally by two. After calculating the bunch charge and arrival time, the RPU0 leaves the interrupt service routine, re-arming the data-acquisition block. The measurement is repeated at the next rising edge of the $acq\_trigger$. The filling pattern information and configuration parameters of the FPFB can be accessed via EPICS channels. The electron bunches are sorted by charge with the information the system provides, and a list with sorted bunch indices is ready for control the injections of the next top-up cycle. The execution time of the interrupt sub-routine within the real-time software, encompassing the bunch-charge and bunch arrival measurements, alongside the statistics of the measurements (moving average and root mean square error), averages approximately 93 milliseconds. This implementation successfully satisfies the requirements of the FPFB, given that top-up injections occur at intervals of 320 milliseconds.

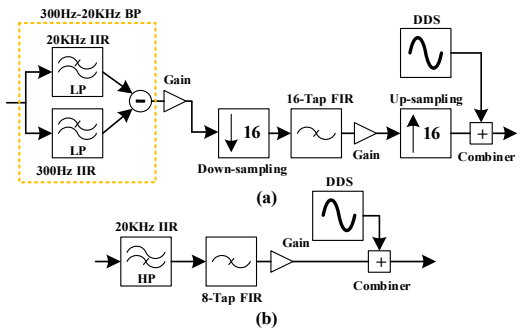

Figure 5: Block diagram of the MBFB firmware. (a) Longitudinal and (b) transverse planes.

Multi-bunch Feedback (MBFB) Systems

In alignment with the firmware design presented in Ref. [2], the interface between ADCs and PL in the latest MBFB firmware operates at f_{RF} (~500 MHz), streaming eight samples in parallel $f_s = 8 \times f_{\mathrm{RF}}$ (~4 Gs/s). In the subsequent processing stage, the input data stream is decimated by a factor of eight. The user selects, via EPICS channels, which of the eight samples, P_i, of the position signal is subjected to processing. Since the bunch window containing the bunch-pulse has 2 ns or eight samples, the P_i selection is such that the sample is close to the pulse peak, facilitating direct sampling. Figures 5(a) and 5(b) show the digital signal processing paths for the longitudinal and transverse planes of the MBFB, respectively. The digital filters (DF) process the selected position data P_i of each bunch i, generating the correction signals C_i. The coefficients and gain of the digital filters are reconfigurable via EPICS to inhibit coherent bunch oscillations. Furthermore, the latency of the DSP paths is adjustable in steps of 2 ns (bunch length), and in the output stage, the user can fine-tune with 250 ps resolution when applying the bunch correction signal C_i to precisely kick the bunch i. In addition to the basic MBFB features, the new firmware design features a multi-bunch excitation framework, which uses a DDS IP core to excite a single or set of bunches, presently with a fixed frequency. We foresee a bunch excitation mode featuring a frequency sweep or phase noise within a predefined frequency range for the next firmware upgrade. The excitation will allow the incorporation of advanced diagnostics tools, such as excitation-damping measurements, betatron and synchrotron tune measures, and automated tuning.

STATUS AND RESULTS

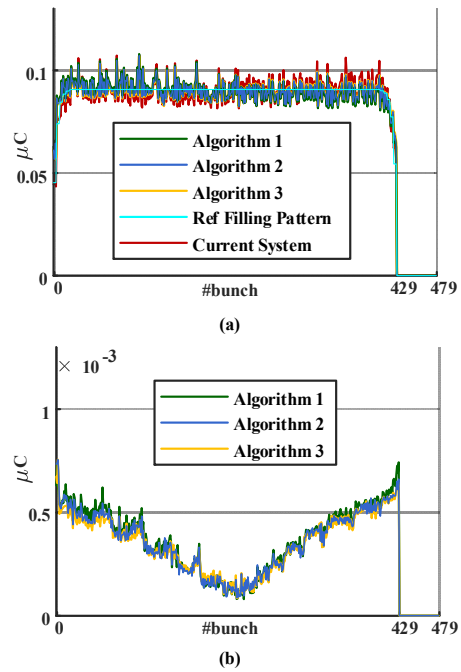

Figure 6: (a) Bunch charge measurement and (b) RMS noise of the measurements with different algorithms.

Filling Pattern Feedback (FPFB) Systems

Figure 6(a) shows the measurement results of the bunch charge obtained at the SLS storage ring using the current FPFB system and with the RFSoC-based system. Figure 6(b) compares the root mean square error (RMSE) of the different algorithms for bunch-charge measurement realized on the RFSoC-based FPFB. Algorithm 3 has slightly better performance. The baseline of Algorithm 3 is set as the average value of the sum signal, S, for eight bunch windows. Figure 7(a) shows the bunch arrival-time measurement results with the RFSoC-based system for the three baseline algorithms. Figure 7(b) compares the root mean square error (RMSE) in the bunch-arrival time measurement for each algorithm, where Algorithm 3 has the lowest RMSE. After successfully implementing the bunch-arrival time and bunch charge measurement in real-time software, the next step is to accelerate the algorithms in PL such that the MBFB can use the bunch-arrival time to correct longitudinal bunch oscillations.

Multi-bunch Feedback (MBFB) Systems

The present firmware version of the RFSoC-based MBFB has been designed to be functionally equivalent to the existing SLS MBFB based on 8-bit VMEbus ADC and DAC

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boards. The MBFB functionality was tested in the laboratory by comparing the open loop response of the VME-based MBFB hardware versus the RFSoC MBFB system for the same input signal and configuration parameters (digital filter coefficients and gains). Moreover, the digital delay control of the DSP processing path was adjusted such that the responses of both systems were aligned in time. Figure 8 shows the open-loop response of the horizontal plane for both systems. The higher ADC resolution of the prototype MBFB system results in lower noise in the correction signal C_i (DAC response). The MBFB prototype system and the RFFE prototype have been tested with beam signals at the SLS. Figure 9 compares the output signal from the existing commercial RFFE and the RFFE prototype for the storage ring filled with a single bunch. The results show that for a single bunch, the signal-to-noise ratio of the correction signal allows the replacement of the present analog downconverter RF front-end (RFFE) for direct sampling of the BPM signals. However, further improvements to the new RFFE and signal processing are foreseen. We plan to use delay lines and interleave multiple ADC channels to increase the effective sampling rate of the current ADC running at 4 Gs/s, facilitating the direct sampling (sample the pulse peak) in a more realistic filling pattern scenarios of the storage ring, where phase slippage of the bunches are present as shown in Figure 7(b).

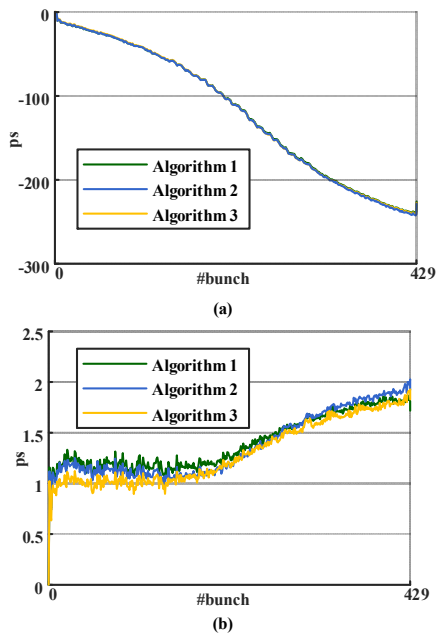

Figure 7: (a) Bunch arrival-time measurement and (b) RMS noise of the measurements with different algorithms.

CONCLUSION AND OUTLOOK

We have implemented the MBFB and FPFB real-time DSP algorithms on an RFSoC platform (ZCU111). The FPFB low-level software, utilized for bunch-charge and arrival-time measurements, meets the time constraints, as the execution time of the algorithms is shorter than the top-up cycles. Among the tested algorithms, Algorithm 3 exhibits a smaller RMS noise by reducing the effects of the baseline fluctuations in the ADC recordings of the sum signal. Next, we foresee the acceleration of the method in firmware such that the bunch-arrival time information can be used for the longitudinal MFFB. Regarding the MBFB, we have conducted a functional verification of the firmware by comparing the hardware response of the VME-based and RFSoC-based MBFB. Our next steps include testing the MBFB feedback closed-loop in SLS and SLS 2.0 and integrating advanced diagnostic tools such as excitation-damping measurements, tune measurements, and automatic parameter tuning. Finally, tests with the new RFFE motivate us to investigate a digital solution (ADC/DAC interleaving) for sampling the BPM signals and driving kicker amplifiers directly with simplified analog pre/post-conditioning, eliminating up/down conversion.

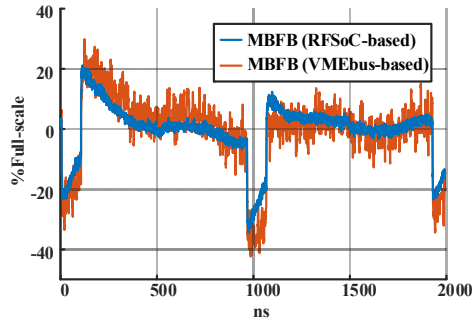

Figure 8: Comparison of the open-loop response (horizontal plane) between the RFSOC and the VMEbus-based MBFB system.

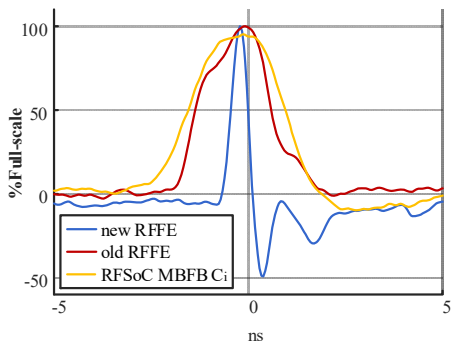

Figure 9: Comparison of the existing RFFE output signal (red) and the RFFE prototype (blue) for the storage ring filled with a single bunch. The yellow curve is the feedback response (horizontal plane) from the RFSoC MBFB.

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