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A HYBRID APPROACH TO UPGRADE HARDWARE FOR THE PROTON STORAGE RING FAST KICKER

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Abstract

The Los Alamos Neutron Science Center (LANSCE) Proton Storage Ring (PSR) needs precise timing to ensure successful extraction of the bunched protons. The current control system's hardware is obsolete and unmaintainable. The task was to replace the 1980's era CAMAC control and timing system for the PSR extraction kickers. This included a system which halts charging of the kickers after a duration without firing to prevent equipment damage. A hybrid approach was taken to integrate a Berkeley Nucleonics Corporation (BNC) pulse generator that was controlled by a soft input/output controller (IOC) and National Instrument (NI) compact Reconfigurable Input/Output (cRIO) IOC. This allowed for flexibility and modularity of the software and hardware development. This approach built the framework to streamline robust deployment of hybrid systems and develop a solution for upgrades of other LANSCE kickers.

INTRODUCTION

Proton Storage Ring

The LANSCE proton storage ring (PSR) [1], Fig. 1, is used to collect and bunch protons. The alignment and frequency of the protons are changed continuously to keep them inside the ring for multiple cycles which are then ejected to the Lujan Mark IV target [2] to produce neutrons which are used in several experiments.

Fast Kicker Purpose & Controls Upgrade

The storage fast kicker (SRFK) [3] system consists of a DC power supply, a Blumelein [4] that acts as a capacitor, and two plates (SRFK71 and SRFK81) as well as a control system that directs and monitors certain functionality. The fast kicker system is responsible for extracting the bunched protons from the PSR and sending them down the beam line towards the neutron producing target.

The control system that was upgraded used an obsolete, 1980's, CAMAC form factor. It is worth mentioning that it had no safety mechanisms in place for over charging the fast kicker Blumlein which is holding the charge that is being provided in a pulsed fashion by a DC power supply. The newly deployed and functionality advanced control system utilizes a hybrid approach by using two commercial of the shelf systems (a) BNC 577 pulse generator [5] for generating delayed pulses and (b) cRIO [6] for reading back the status of an RF switch and keeps track of charging pulses to the Blumlein. The hybrid approach also extends to the controls software implementing (a) soft IOC to control the BNC 577 and (b) NI cRIO based IOC that has a field programable gate architecture (FPGA) [7] backplane interacting with the modules for high-speed data acquisition.

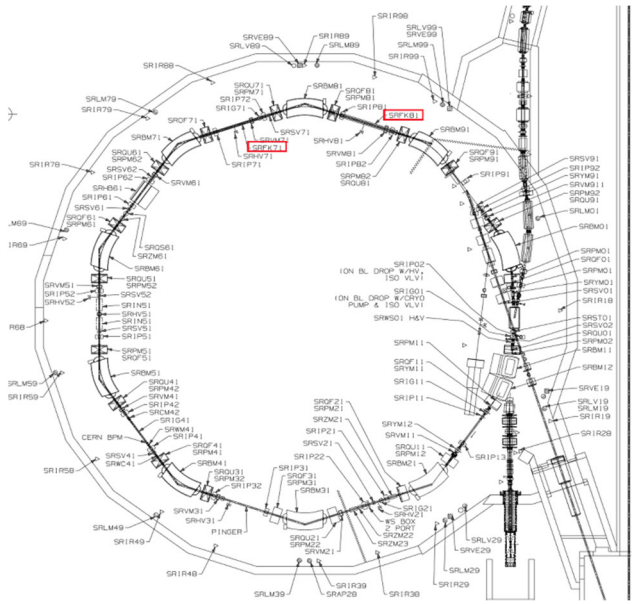

Figure 1: LANSCE Proton Storage Ring with magnet locations.

PSR TIMING STRUCTURE

LANSCE has a distributed Master Timer system [8] which provides timing gates to different systems across the accelerator facility. A subset of these gates is for the PSR operating at a nominal 20 Hz rep rate. The ones of interest for the kickers are Extraction Kicker Charge Gate (EKCG), Storage Ring Extraction Window (SREW), and Extraction Kicker Long Fire (EKLF).

The beam pulse structure is known as Long Bunch Enable Gate (LBEG). Within each LBEG pulse, there are ~2000 pulses mini pulses whose period is designed to be equal to the time for 800 MeV beam to circulate in the PSR at a rate of 2.8 MHz. The mini pulse is high/present for 270 ns and low/absent for 90 ns. This creates a gap in the beam which allows for the bunched protons to be extracted without interacting with incoming beam.

The EKLF gate is responsible for firing the kickers and extracting the beam. Two conditions must be met to extract, first the SREW much be high and second the EKLF pulse is synchronized with 2.8 MHz reference. These ensure the incoming and outgoing beams will not interact.

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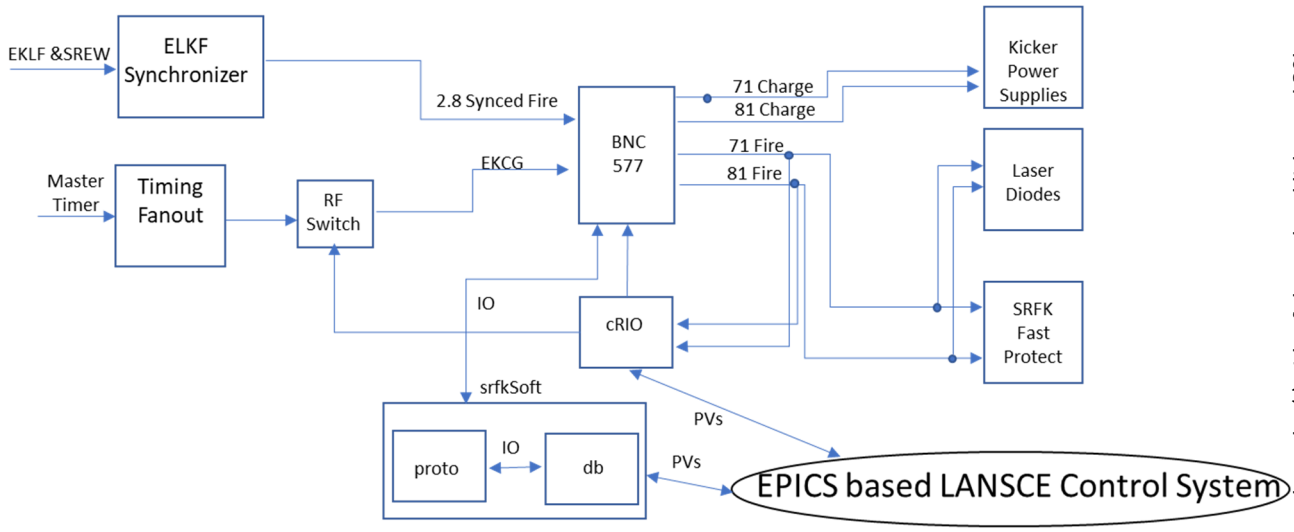

Figure 2: Software and hardware architecture for SRFK upgrade.

HARDWARE ARCHITECTURE

In the following we describe the hybrid hardware architecture in more detail. The complete hardware architecture is presented in Fig. 2, where it details the two major hardware controls the BNC 577 configuration shown in Table 1, and the NI cRIO which interact with the timing, power supply, synchronizer, switch, diodes, and fast protect system. The BNC pulse generator, Fig. 3, that the user can set pulse widths and delays for generating the pulses used to time the kicker. The delay and charging of the kickers are dependent on the length of the Blumlein cables which vary kicker to kicker. The LANSCE Master Timer system gates that the entering and exiting beam does not interact. When the BNC receives a timing gate, EKCG or ELKF, it triggers and delays an output pulse to the kickers. The Fast Protect system ensures that there is always a successful discharge of kickers which in turn eliminates radiation spill by shutting off the beam if it is not extracted from the PSR.

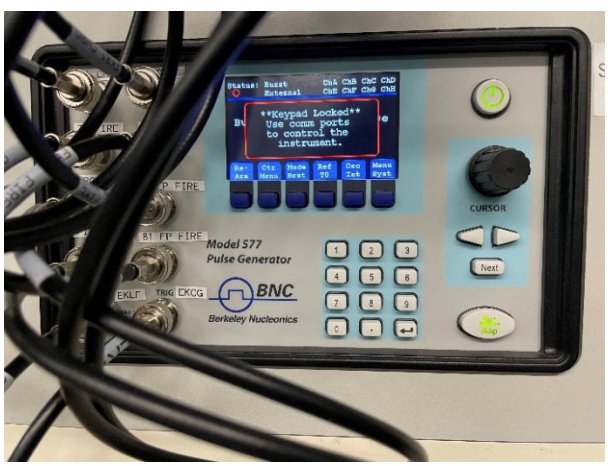

Figure 3: BNC pulse generator.

Figure 4: 8 card NI cRIO.

Table 1: BNC Specifications

Feature	Description
Channels	4 or 8 ind. channel outputs
Resolution	250 ps
Accuracy	1 ns + .0001 x setpoint
RMS Jitter	< 50 ps (channel to channel)
Voltage	5 V for TTL; 45 V for Adjustable
Pulse Width	10 ns – 1000 s
Memory	12 Storage Slots

Table 2: NI cRIO 9038 Specifications

Feature	Description
NI 9425	Binary Inputs
NI 9401	Counters
NI 9205	Analog Input with delays
NI 9262	Pulse Generation
NI 9485	Binary Outputs
NI 9485	Binary Outputs
NI 9485	Binary Outputs
NI 9264	Analog Outputs

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The 8 card NI cRIO, Fig. 2, handles readbacks and tracks counts with a delay using the NI 9401-counter card, NI 9205 analog input card that is triggered after a 7500 µs delay, NI 9485 binary command card, and NI 9264 analog command cards, all the NI cRIO module configurations are shown in Table 2. The delay is based on the charge gate and is needed to ensure that the readback voltage is sampled at the peak of the charge ramp. The counters ensure that the number of charge and fire pulses are the same. If there are more charge pulses than fire pulses, the NI 9485 is closed which flips an RF switch to prevent further charge timing pulses from reaching the BNC. This is how we ensure that the fast kickers are not over charged. The NI 9264 is used to change the setpoint voltage of the kickers.

SOFTWARE ARCHITECURE

The complete software architecture for the LANSCE control system (LCS) is presented in Fig. 2 interacting with the hardware. At LANSCE we use the Experimental Physics and Industrial Control System (EPICS) architecture [9]. EPICS is a set of open-source software tools, libraries, and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as particle accelerator, telescopes, and other large scientific experiments. It gives access to various levels of functionality for IOCs using process variables (PVs) which can have multiple user defined attributes that are available to other users who would like to access the system. Users can set/change values and are able to get readbacks using PVs which are ascribed to control a feature of a specific equipment. The PVs are housed inside the database located inside an IOC which allow the users of LCS to access the PVs across the site on consoles that are connected to LCS.

The BNC pulse generator has a serialized communication protocol using a MOXA [10] serial to ethernet adapter. The serial commands are interpreted by a stream-protocol file which associates the commands to the process variables (PV). The stream-protocol is designed to handle asynchronous data using EPICS. The input/output PVs configured in the stream-protocol is then associated with a database file that sets attributes to the PVs such as description, units, etc. Databases are important for EPICS to function because they are necessary to define PVs and can be generated either manually or programmatically through a template. In this project we handle calculation inside the database using calc and calcout record types. The PVs handle multiple types of input and output data, in this project we used analog output, analog input, binary output, and binary input.

The PVs for the BNC 577 were handled via stream-protocol and were housed in a virtual soft IOC called srfkSoft, Fig. 3. Soft IOCs are created as virtual instances of an IOC rather than a physical controller such as a NI cRIO. This can be housed in remote servers which allows the developers to access it remotely from all consoles on the LCS. Soft IOCs have been instrumental in reducing the number of physical sites to house hardware and provides a clear and robust approach to setting up disparate pieces of hardware using a single type of IOC flavor.

The NI cRIO software involves an object-oriented programming (OOP) FPGA code written in LabVIEW that generates a bit file. This bit file is used by a C++ device support code that assigns the data received from the device asynchronously to the EPICS PVs. We then use EPICS templates to define the attributes of the PVs in the database. The IOC in this case is the physical NI cRIO that is deployed on to the field. This approach differs from the soft IOC case because we require high speed data from the NI cRIO FPGA for controlling some of the devices that require faster responses. Hence, it is beneficial to have the IOC integrated with the cRIO system.

HYBRID APPROACH

The hybrid approach that was undertaken for this project focused on establishing versatility for system design by having two simple approaches to hardware and software architectures that were both integrated in the larger LCS framework. The ability to create PVs using soft IOCs on virtual machines for the BNC 577 pulse generator and physical IOCs using NI cRIO's FPGA backplane. This effort flows well with our long term LANSCE modernization [11] project that is focused on reducing the number of disparate control systems to a more unified approach. We used this homogenous approach principle to incorporate a soft IOC to handle the stream device input/output control PVs and use an existing deployed cRIO to handle the readbacks, counters, and set time delays for the pulses.

A hybrid approach by incorporating stream device protocol for BNC pulse generator accompanied by a soft IOC and an industrial input output (IIO) using cRIO with a self-contained IOC helped us easily upgrade the legacy CAMAC system that was used to control the SRFKs for over a decade. The flexibility this approach offers without introducing additional complexity to providing solutions will be useful moving forward with upgrading control systems at LANSCE and at other accelerator facilities that rely on the EPICS architecture.

CONCLUSION

The results have shown that the new hybrid system consisting of the BNC 577 pulse generator and cRIO is functionally equivalent to the CAMAC system it is replacing. Further we now have better control of the counters to time the kicker more accurately than in the past, which protects the equipment from being over charged. All these improvements will be beneficial as our organization is transitioning LANSCE away from its legacy hardware.

ACKNOWLEDGEMENTS

We would like to thank Scott Baily for creating the IIO LabVIEW template and helping with the 9205 card's time-delay as well as 9401 counter code troubleshooting which were instrumental in giving new capabilities to the storage ring fast kicker that it has never had previously.

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