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NOVEL CAVITY BPM ELECTRONICS FOR SHINE BASED ON RF DIRECT SAMPLING AND PROCESSING*

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Abstract

A RF direct sampling beam signal processor has been developed in SSRF. It mainly consists of four channels RF direct sampling ADCs and a SoC FPGA. The ADC is 9 GHz bandwidth and 2.6 GHz sampling rate. A prototype of RF module contains band pass filter, low noise amplifier and step attenuator has been designed for SHINE cavity BPM system. Then a novel cavity BPM electronic including the processor and the RF module has been built for SHINE. The performance of the electronic has been analyzed and evaluated in lab. The amplitude relative error is 2.0×10^{-4} which is better than the required 1×10^{-3} on cavity BPM system. The phase error is 14 fs, also better than the requirement of RF BAM system. The algorithm and implementation in FPGA have been introduced.

INTRODUCTION

Shanghai Hgh repetitioN rate XFEL and Extreme light facility (SHINE) is a 3 km long hard X-ray FEL facility built 30 m underground in Shanghai. The designed beam repetition rate is 1 MHz. The project was initiated at the end of 2018, and to be completed at 2027. The SHINE was built adjacent to the campus of Shanghai Synchrotron Radiation Facility (SSRF) and Shanghai Soft X-ray FEL(SXFEL). Three types of BPMs are used in different sections: stripline BPMs are used in injector and sections between cryomodules, cold button BPMs are installed inside the cryomodules of the super conducting LINAC, and cavity BPMs are used in beam distribution lines and FEL sections.

Two types of cavity BPMs are designed for SHINE. A Φ35mm cavity BPM is designed for the distribution lines, which center frequency is 3520.87 MHz, and the required resolution 1 μm at 100 pC, and the dynamic range is ±1 mm. While a Φ8 mm cavity BPM is designed for the FEL sections, which center frequency is 5254.2 MHz, and the required resolution 200 nm at 100 pC, and the dynamic range is ±100 μm. It means the relative resolution of the cavity BPM electronics should better than 0.1%.

The cavity BPM generates signals with different modes when electron beam passing through. The amplitude of TM_{010} mode signal is proportional to beam charge, and the TM_{110} mode signal is proportional to both beam charge and beam position. The signals are narrow bandwidth at high frequency with high Signal to Noise Ratio (SNR), normally at several GHz.

BPM electronics use independent RF front-end modules and digital signal processors. Different RF front-end modules will be designed to meet the signal characteristics requirements of different BPM types. A generic beam signal processor platform has been developed for beam diagnostic system. Three types of electronic structures can be used to process the high frequency cavity BPM signal. First is the heterodyne, it down converts the signal to intermediate frequency (always at tens of MHz) for digitizing. It is proven trusted and high performance, and widely used, like LCLS I, LCLS-II, SXFEL, *et al.* But it is complicate and large physical size. The long chain RF components, especially Local Oscillator (LO) synthesizer and mixing modules introduce extra noise, and fragile to environment temperature humidity. Second is direct sampling the high frequency signal with ADC. The hardware is the simplest, most flexible, it is practical at L, S, C band right now. Because of the limitation of ADC bandwidth and effective number of bits, no large-scale application now adays. Third is direct-convert the signal to base band, or we say zero intermediate frequency in two quadrature channels. This structure lowers the requirement to low-pass filters and ADCs, simplifies the digital signal processing. European-XFEL made excellent work with this structure. The challenges of this structure including I/Q balance, local oscillator leakage, the interference from low frequency noise, also need one more ADC.

In SXFEL, the cavity BPM signal is down converted from about 4680 MHz to 30 MHz, and then digitized and processed with a self-developed signal processor (DBPM) [1]. The DBPM in a one stand-alone processor with a FPGA carrier board, an ADCs board and an ARM board. The ADC board has four input channels, the maximum sampling rate is 125 MHz, resolution is 16 bits, and bandwidth is 650 MHz. The ADC running at 119 MHz external clock synchronizing to RF. A XILINX Virtex5 FPGA is used as the core component on the carrier board. Except for the DBPM, a RF front-end is install besides the pickup in tunnel, a LO synthesizer and a down-conversion module are installed in the cabinet of electronic hall with DBPM. Obviously, the install space is quite large and cost is high.

In SHINE, the cavity BPM electronic cabinets are near the pickups in tunnel. The RF module integrates RF front-end module, LO synthesizer, and down conversion module into a 1U chassis. The signal is down-converted to 54 MHz, then sampled and processed with a generic beam diagnostic processor. The processor is stand-alone 1U height, including a XILINX Soc FPGA carrier board, a high-speed

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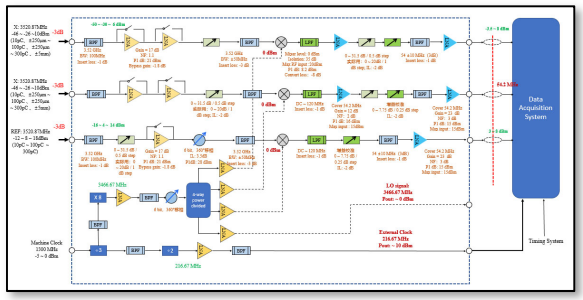
ADC board and White Rabbit timing board connected through two FMC interfaces. The ADC's maximum sampling rate is 1GHz, bandwidth is 2 GHz, and resolution is 14 bits [2-4].

Figure 1(a) is the block diagram of the cavity BPM electronic in SHINE, Fig. 1(b) is the picture of the beam signal processor.



(a)

(b)

Figure 1: Block diagram of Cavity BPM electronic (a) and picture of generic processor (b) for SHINE.

RF DIRECT SAMPLING ELECTRONICS

From the block diagram of the Fig. 1(a), we can see complicate RF chains. Mainly because of the heterodyne structure. RF Direct sampling Electronic (RFDE) shows obvious benefits compared to it. First, RFDE have no need of different LO synthesizers and down conversions for different types of cavity BPM in heterodyne structure, only need bandpass filter (BPF), low noise amplifier (LNA), and adjustable attenuator, which reduces the design difficulties and improve the maintenances efficiency. Second, less analog components improve the system sensitivity and stability. Third, smaller system size reduce power consumption and save budgets.

RFDE has long been pursued in accelerator. Since 2008, there have LLRF system, bunch feedback system, high speed digitizer, and BAM have used RF direct sampling electronics. We can summarize them into two categories. One is ADC boards sampling rate lower than 1 GHz, bandwidth smaller than 2.5 GHz. The other is XILINX RFSoC demo boards with multi number high speed ADCs and DACs. We tried the RFDE with an oscilloscope in 2017 [5]. No application in cavity BPM online signal processing yet.

The digital signal processing system mainly includes two parts: sampling and digital signal processing. Currently, varieties of ADCs with sampling rate to several GHz and bandwidths to about 10 GHz appeared. Then the CBPM signal in L/S/C band can be digitized directly. The ADCs based on JESD204B serial interface standard supports 12.5 Gbps data transmit speed between ADCs and FPGA, which makes real-time data transmission and processing in FPGA possible. Nowadays, powerful FPGA contains hard ARM cores, rich peripheral interfaces and massive logic resources have been widely used, which can realise real-time complex signal processing algorithms.

RFDE FOR SHINE CAVITY BPM

We developed a RFDE processor for SHINE. The processor is specified in Table 1. The processor is designed as a 1U height standalone, consists of a FPGA carrier board and an ADC daughter board connected through FMC connector. Another FMC connector is reserved for a White Rabbit timing board.

Table 1: RFDE Processor Specifications

Parameter	Value
Channels	4
Bandwidth	9 GHz
ADC bits	14
Max ADC rate	2.6 GHz
FPGA	Xilinx ZCU15EG
Clock	External
Trigger	Ext./Self/Period
SFP	2 UDP, 2Aurora
Interlock	Lemo
PL DDR4	2 GB
GPIO	12
Software	Arm-Linux/EPICS

Figure 2 shows the pictures of the processor. The ADC board is designed in large size for better performance.

Figure 2: Picture of RFDE processor.

We build a protype of RF module to evaluate the possibility of RFDE. Each channel includes a band pass filter, a low noise amplifier, and a 10 dB step attenuator. The block diagram and the picture are show in Fig. 3. The connections between components are removable for easy testing.

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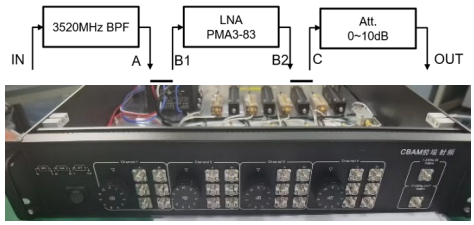


Figure 3: RFDE RF module.

With the developed processor and the RF module, a RFDE for cavity BPM system is built. The overall function is depicted in Fig. 4. Compared to the heterodyne structure in Fig. 1, RFDE system is much simpler.

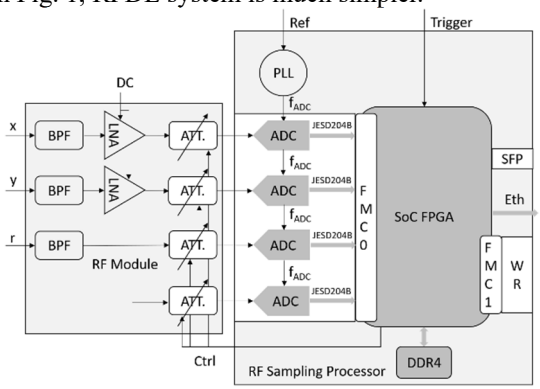


Figure 4: Overview of RFDE for SHINE cavity BPM.

SYSTEM PERFORMANCE ANALYZING

One of the main concerns with RFDE is whether it can meet the requirement of cavity BPM system. Noise figure (NF) is always used to evaluate the performance of an electronic. It's a measure of the noise added by the device (degradation of the SNR from input to output). The definition F and NF are listed below:

$$F = \frac{S_i/N_i}{S_o/N_o} \quad (1)$$

$$NF = 10 * log_{10}(F) \quad (2)$$

Where $S_{i/o}$ and $N_{i/o}$ are the signal and noise of the input and output respectively.

The NF of the cascaded devices chain can be calculated with NF and the gain (G) of each device. The NF and G parameter can be found in the datasheet of LNA. For passive devices, such as mixer, filter, and attenuator, the NF is not listed. The NF can be approximated with insert loss. There is no NF parameter listed in ADC datasheet, the calculation is a bit complicate. Equation (3) is the definition of NF_{ADC}.

$$NF_{ADC} = 10 \cdot \log\left(1000 \cdot \frac{(V_{PP})^2}{8 \cdot Z_{IN}}\right) + 174dBm - SNR_{ADC} - 10 \cdot \log\left(\frac{F_S}{2}\right) \quad (3)$$

Where F_S is the sampling frequency. The NF_{ADC} of RFDE processor and SHINE generic processor is 30.1 dB and 25.4 dB respectively.

Except for the NF of the hardware, extra digital signal processing gain can be obtained from filtering out the 1.6 MHz cavity BPM signal from the Nyquist zone. The formula is:

$$Processing\ Gain = 10 \cdot \log\left(\frac{F_S}{2B}\right) \quad (4)$$

Where B is the bandwidth of the cavity BPM signal. The processing gain of RFDE processor and SHINE generic processor is 24.3 dB and 29 dB respectively.

After getting above information, the SNR of RFDE and SHINE heterodyne structure is 85 dB and 87.2 dB respectively when the SNR of cavity BPM signal is 72 dB, the relative error of them is 7×10^{-5} and 5×10^{-5} respectively. They show similar performance and both far better than the requirements.

RFDE PERFORMANCE EVALUATION

Processor B using 16 bits ADCs and Xilinx FPGA XCZU9EG. LMK04832 is used to provide low jitter clock for ADC and the system. Figure 4 is the PCB of the processor. The ADC board is wider than the FMC standard. Lab test conditions were the same as the processor A test, but the sampling clock was multiplied to 833 MHz.

A lab test platform in Fig. 5 was built to evaluate the RFDE performance. A vector signal source generates a decay RF signal to simulate the cavity BPM signal and a 1.3 GHz signal divided as clock source. An external trigger from trigger divider is input.

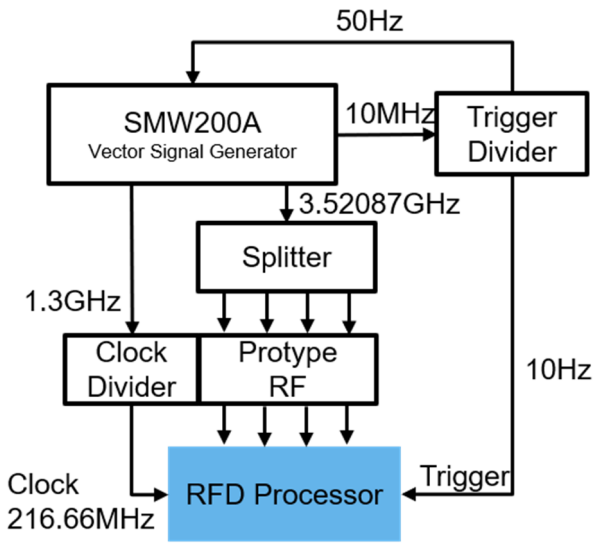
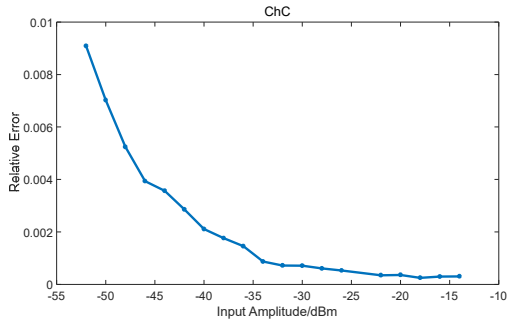


Figure 5: Block diagram of lab test platform.

The channel input signal amplitude changed from -52 dBm to -14 dBm. Figure 6 is test results. The best relative error of one channel is 2.6×10^{-4}, which contains signal source jitter. The best relative error between two channels is 2.0×10^{-4}, this is better than the required 1.0×10^{-3}.



(a)

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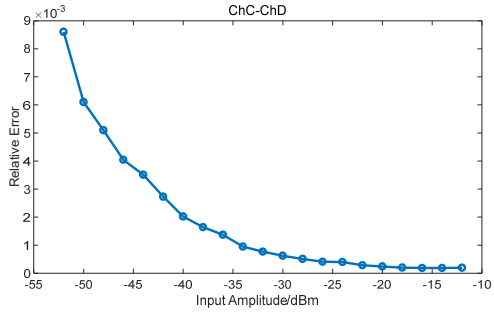


(b)

Figure 6: The relative amplitude error of one channel (a) and the value between two channels (b).

There are RF cavity BAMs in LINAC of SHINE designed the same frequency with Φ35 mm CBPM. Figure 7 is the relative phase error between two channels. The best phase RMS jitter is 14 fs, which is better than the required 25 fs resolution.

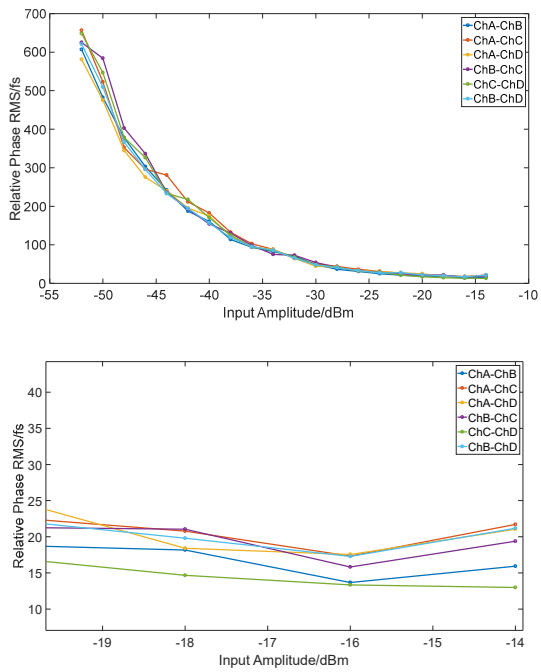
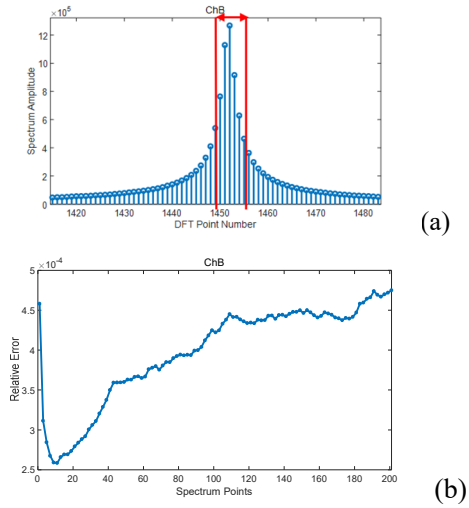


Figure 7: The relative phase error between two channels.

We investigated three cavity BPM signal processing algorithms to evaluate the performance and implementation. First is the fix point Goertzel-DFT algorithm. Figure 8(a) shows the calculated DFT points. The number of used points around peak influence the calculated relative error. Figure 8(b) shows the relative error of peak point is 4.5×10^{-4}, 3 points is 3.1×10^{-4}, 5 points is 2.8×10^{-4}, the best value is 2.6×10^{-4}. Second is Digital Down Conversion (DDC) algorithm. Third is Hilbert algorithm. All three algorithms can get the best result of relative error at 2.6×10^{-4}. We choose to implement Goertzel-DFT in FPGA, because the calculation point is fixed and 3 points DFT calculation is good enough.



(a)

(b)

Figure 8: Goertzel-DFT algorithm (a) and the relative error change with DFT points (b).

We implemented 3 points DFT algorithm in FPGA. About 35% CLB and 7.5% DSP were costed.

CONCLUSION

A RFDE has been built for SHINE cavity BPM signal processing, including a prototype RF module and a RF direct sampling processor. The RF module contains only BPF, LNA and step attenuator, which is much simpler compared to the heterodyne structure. The processor supports sampling 9 GHz signal at 2.6 GHz, and calculate 1 MHz rate beam position in real-time. The system performance is 2.0×10^{-4}, which is better than the requirement of SHINE.

Compared to the electronics 10 years ago, same budget today can afford much higher performance electronics. The cost saved from RF module can support the RF direct sampling ADCs. It's time to consider large-scale application of RFDE in beam diagnostics.

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