ISBN: 978-3-95450-236-3 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2023-MOP023

THE CONCEPTUAL DESIGN STUDY FOR NEW BPM SIGNAL PROCESSING SYSTEM OF J-PARC MAIN RING (MR)*

K. Satou†, T. Toyama, S. Yamada, J-PARC/KEK, Tokai, Japan

Abstract

The beam position monitor signal processing system, which is a 19-year-old system, has been suffering from gain fluctuation due to contact resistance of the mechanical gain selector and communication disruption caused by an unstable contact of a card edge connector. It also has difficult repairments because some onboard parts have already reached the end of a product-life cycle, and some units have been in an unusable situation. currently, we are on the beam power upgrade campaign to 1.3 MW by increasing the beam bunch current and shortening the main ring operation cycle, and precise beam tunings would require massive waveform data processing and transfer to a storage system than the present system. For this, we have been developing a system based on the 10 GbE optical link. The ADC board, which is under development, performs direct sampling using the third harmonics of accelerating radio frequency. The digital IQ demodulation technique is used to extract the baseband oscillation from the raw data. The obtained raw waveform and closed orbit data are stored in the data storage system. In the presentation, we will report on the progress of development aimed at operation in 2025 and the conceptual design of the new system.

INTRODUCTION

In the J-PARC main ring (MR), 186 beam position monitors (BPMs) have been used to measure beam orbit and beam optic parameters [1, 2]. Its signal processor, BPM circuit (BPMC), designed 19 years ago, has two modes of position measurement:

1) Closed orbit distortion (COD) mode,
2) bunch-by-bunch (BxB) mode.

The first mode is a narrowband measurement that performs a fast Fourier transform on the waveforms digitized with 80 MHz to extract the second harmonic component of the accelerating radio frequency (RF) to obtain the COD. Meanwhile, the second mode is a broadband measurement for measuring bunch waveforms to measure the beam center of each bunch. The position measurement error is approximately 30 and 300 μm for the COD and the BxB modes, respectively [3].

At some BPMC, communication disruption was caused by an unstable contact of a card edge connector. However, this BPMC is too old that some circuit parts have already been discontinued. This makes maintenance work difficult and some BPMCs unusable. If this situation progresses, there is a risk that sooner or later stable MR operation will be hindered.

The BPMC shows the beam position shift due to the change in the contact resistance of a relay. To optimize the input signal level, it has a 20 dB fixed attenuator placed just before the input terminal and a variable attenuator in the BPMC. Depending on the beam condition, the attenuation factor is selected by switching a relay element on the circuit, and its switching frequency is approximately several times per year. The contact surfaces are then exposed to atmospheric gas for a long time because the relay is not strictly shielded. The inspection of the relay surface confirmed that the silicon-based compound was layered. This results in surface contamination and consequently resistance changes. A 0.5 Ω change in contact resistance results in an error of 1.3 mm. Moreover, an error of several millimeters– may occur because of individual differences in relays. This resistance can be reduced by applying a voltage [4]. However, there are large individual differences in this effect, and no clear systematicity has been confirmed so far, therefore, calibration is difficult. To examine the impact of this effect, some consistency check methods between the BPM sensors are now proposed [4, 5].

Moreover, beam tuning above 1 MW is supposed to require high-precision measurement of optics parameters [3]. Thus, it is necessary to process a large amount of highly accurate position data. Improvement of the system is also necessary.

NEW BPM SIGNAL PROCESSOR

We are developing a new signal processor as part of the MR beam power upgrade campaign to 1.3 MW. In the new system, we aim to reduce the position error to 1/3 or less in both modes. To achieve this, we will use the following items:

1. Reduction of the reflection coefficient of the attenuator input terminal,
2. reduction of signal distortion and gain temperature coefficient in the attenuator and ADC,
3. improvement of the vertical resolution of the ADC,
4. improved digital signal processing section.

Figure 1 shows a block diagram of the new system installed in four different buildings. It uses the existing BPM sensors and its signal cables, which are 100-300 m depending on the sensor location. An attenuator unit, ADC card, network interface controller unit (NIC unit), and data storage system have been developed.

The attenuator unit is powered by a nuclear instrumentation module (NIM) standard bin power supply and the ADC card is housed in the same NIM case. The digitized waveform data are delivered over a 10 GbE optical private network and forwarded through the NIC unit to the data storage system. This network uses the user datagram protocol (UDP).

* Work supported by Accelerator and Beamline Research and Technology Development for High-Power Neutrino Beams in the U.S.-Japan Science and Technology Cooperation Program in High Energy Physics.
† email address: kenichirou.satou@j-parc.jp

Content from this work may be used under the terms of the CC-BY-4.0 licence (© 2023). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

ISBN: 978-3-95450-236-3 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2023-MOP023

The configuration of the attenuator units and the ADC cards will be made through the experimental physics and industrial control system (EPICS), which is a distributed control system on the accelerator control network. The COD and alarm data will also be sent to the control network through the NIC unit. The development of the attenuator unit has already been completed, and we are currently developing the ADC card, NIC unit, and data storage system.

The development of each component will be completed by the end of this fiscal year, and part of the system will be built and tested in the next fiscal year, and mass production will be completed. We plan to start operating the new BPM system by FY2025. This paper provides an overview of the new system and the functions and outlines of each component.

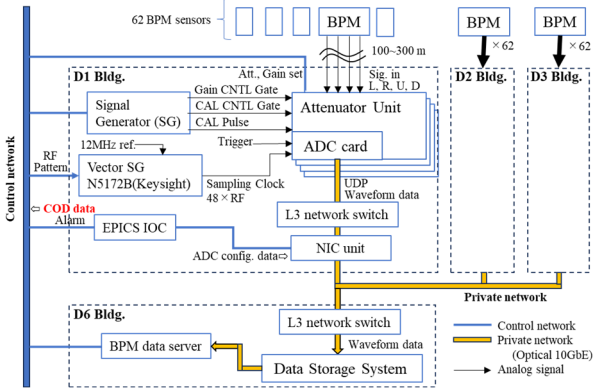

Figure 1: Block diagram of the new BPM system.

COMPONENT DESIGN

In MR, 3 GeV protons are accelerated to 30 GeV in about 1 second. The accelerating frequency of the RF accelerating devices changes from 1.672 to 1.720 MHz, with a harmonic number of 9.

The BPM sensor is a diagonal cut type, and the four signals R, L, U, and D from the right, left, top, and bottom electrodes are transmitted to the BPM signal processing unit via 5D-FB coaxial cables. The sensor capacitance and 50 Ω input impedance form a high-pass filter with a cutoff frequency of approximately 16 MHz, resulting in an output pulse shape of the derivative of the charge bunch as shown in Fig. 2.

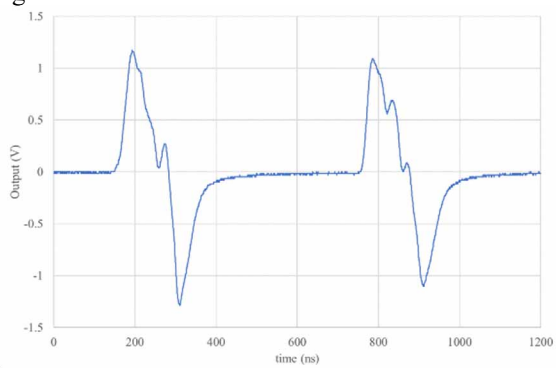

Figure 2: Beam pulse shape of 3 GeV beam.

Attenuator Unit

The new attenuator device has already been developed and is in mass production [6]. Figure 3 shows a block diagram of the new attenuator device.

As the beam bunch shape becomes sharper with acceleration, the signal reaches a maximum voltage of 200 V peak to peak (Vpp) when the beam energy of 30 GeV is reached. To match the input level of an ADC of 2 Vpp, the input signal is attenuated through an RF2033 power divider (−12 dB), a switchable attenuator (−10 dB or 0 dB), a variable gain (G = 1 or 1/2), and an RF transformer (1/2).

The new attenuator uses a reed relay, HFS-1C-05W (manufactured by OKITA Works Co., Ltd.), enclosed in a glass tube filled with nitrogen. It is expected that the contact resistance will be stable for a long time because it is not affected by dust or atmospheric gas because of its sealing. From the Ref. [7], it can be seen that if the reed relay was used within 2E6 times, the contact resistance would be approximately 10 mΩ. This impedance change induces beam position variation of approximately 4 μm. It was implemented using a special socket so that it can be replaced in case the relay exceeds its usage limit or is damaged.

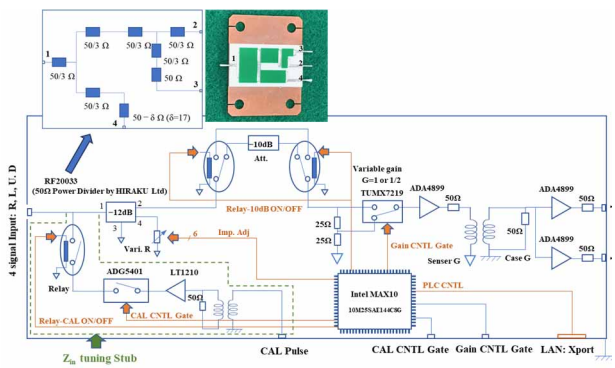

Figure 3: Block diagram of the new attenuator unit.

In the BxB measurements, impedance matching between the signal cable and the attenuator device is important. To achieve fine matching, a circuit to adjust the input impedance was implemented. For adjustment, the power divider RF2033 produced by HIRAKU Ltd. is used (Fig. 3). If a 17 Ω resistor is connected to terminal 4, the input impedance (Z_{in}) and attenuation (Att) seen from the input becomes 50 Ω and 1/4 (−12 dB), respectively.

When 17−δ Ω is connected to this terminal, the impedance seen from the input is given by

$$Z_{in} = 50 - \frac{\delta}{4} - \frac{3}{800}\delta^2. \quad (1)$$

Therefore, Z_{in} can be finely adjusted by the δ with a variable resistor. At the same time, the δ modulates the attenuation to be

$$Att = \frac{3}{8}\frac{400 - 3\delta}{600 - 3\delta}. \quad (2)$$

A high intensity beam can produce up to 200 Vpp at the input terminal of the attenuator unit, so the signal must be attenuated to match the input level of the ADC circuit.

By driving the Z_{in} with any test signal, the gain balance of each channel, cable attenuation, and matching between

Content from this work may be used under the terms of the CC-BY-4.0 licence (© 2023). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

ISBN: 978-3-95450-236-3 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2023-MOP023

Content from this work may be used under the terms of the CC-BY-4.0 licence (© 2023). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

the cable and Z_{in} can be measured. As shown in Fig. 1, the Z_{in} tuning stab circuit is connected by turning on Relay-CAL. Then, the Z_{in} can be excited with a waveform input from CAL_SIG. The relay is used here because the voltage at Z_{in} is expected to be at a maximum of 200 Vpp for the designed beam power operations.

A burst wave of 5 MHz, its frequency in the main signal band to be processed at the ADC card, is used as a test signal. The wave height of the input wave (first wave) determines the total gain of the attenuator unit and ADC card. The first wave is reflected by the BPM sensor's capacitance (130 pF), and the returned wave is observed as the second wave. The cable attenuation can be estimated from the signal ratio of the second wave to the first wave considering the reflection at the BPM sensor. Before the second wave arrives, it turns off the MOSFET switch ADG5401 by the CAL CNTL GATE to disconnect the impedance of the drive amp from Z_{in}. If the Z_{in} does not match the cable impedance, a part of the second wave will be reflected to the BPM sensor and then observed as the third wave. The reflection coefficient at Z_{in} can be calculated from the third wave, where the third wave height depends on the reflection at Z_{in}, cable attenuation, and reflection at the BPM sensor. Here, at a frequency of approximately 5 MHz, the electrical length is approximately 40 m. Thus, the reflection inside the N-type connector used can be ignored.

Figure 4 shows the test results using a 200 m 3D-FB cable with a Z_{in} of 50 Ω. From the wave heights of the first and second waves, the cable attenuation was estimated to be 32 dB/km at 5 MHz. The actual BPM cable is NH-5D-FB, and its cable attenuation is approximately 1/5. From the third wave, the reflection efficiency at Z_{in} was estimated to be 1.02. In the actual operation, matching is achieved by adjusting Z_{in} so that the wave height of the third wave becomes the minimum value.

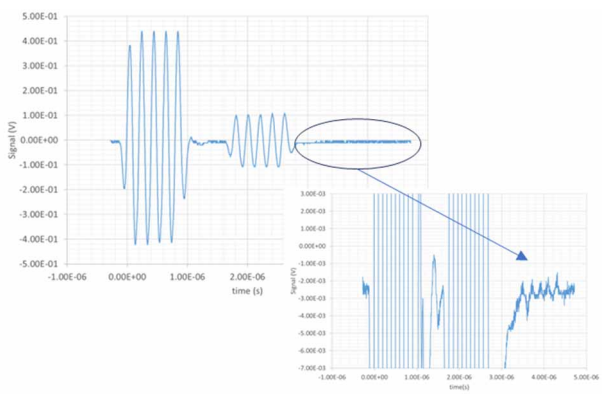

Figure 4: Calibration test signal input at the Z_{in} and multi-reflected waves. The third wave shows impedance mismatching at the input terminal.

In the actual operation, the Relay-CAL is turned off. Therefore, it is necessary that Z_{in} does not change due to the relay operation. The upper part of Fig. 5 shows the difference in S11 with and without the Z_{in} tuning stub circuit. Here, Z_{in} was set to 50 Ω (δ=17). The voltage standing wave ratio (VSWR) at the input terminal was measured in the range of 1 to 10 MHz. In the range of 1 to 5 MHz, they are almost the same within the error. However, in the range of 5 to 10 MHz, the compensation circuit is slightly over-compensated, and a difference of approximately VSWR = 0.002 appears. Currently, the VSWR is within 1.005 in the range of 1 to 10 MHz. The lower part of Fig. 5 shows the Smith chart of Z_{in} at 5 MHz where Z_{in} was shifted by changing δ. As shown in the figure, the impedance moves in the range of 50 ± 1 Ω along the line $\mathrm{Im}(Z_{in}) = 0$. The impedance step is 0.037 Ω, which allows impedance matching down to VSWR < 1.001.

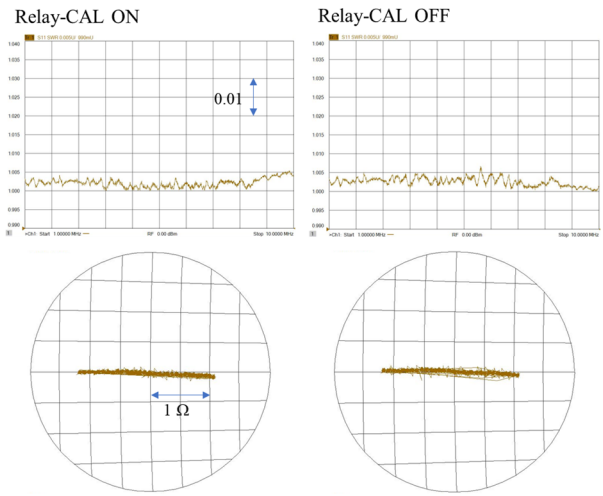

Figure 5: Measurement of impedance matching at the input terminal with and without the Z_{in} tuning stub circuit. The upper part shows VSWR when $Z_{in} = 50\ \Omega$. The lower part shows the footprint in the Smith chart when changing the input impedance.

ADC Card

Figure 6 shows a block diagram of the ADC card under development. The ADC card uses two 16-bit ADCs, LTC2194 from Analog Devices, which perform direct sampling using a 48-multiplied RF clock of approximately 82 MHz. The sampling clock is directly generated using a vector signal generator (SG) N5172B from Keysight based on the RF pattern IQ data and input to the ADC card.

The raw waveform data from the LTC2194 is transmitted and processed using an Arria 10 FPGA from Intel. The timing of each waveform data from a different BPM sensor is synchronized with a delay circuit in the FPGA. To decrease beam signal fluctuations and random noises at each measurement, we average over 1 to N cycles (1 to N MR beam shots) at 1.3 to 5 s MR trigger intervals. For the waveforms processed, filtering with narrowband BPF and IQ demodulation with the third harmonics of the RF is performed to extract a betatron oscillation. Then the I and Q data are processed with LPF, and the amplitude R and a phase θ are calculated. The R data are further processed using LPF, then a sum Σ and a difference δ between the R (U) and L (D) are calculated to obtain horizontal and vertical COD waveform data of approximately 2kSps. When the COD exceeds its preset threshold value, an alarm signal is generated to dump the beams.

ISBN: 978-3-95450-236-3 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2023-MOP023

Part of the raw waveform data, all waveform data of R, θ, δ, Σ, and the alarm status are stored in DDR4 memory and transferred to the NIC unit by using UDP via a 10 GbE SFP+ optical port.

The processing functions, COD alarm threshold level, and raw data to be saved and transferred are dynamically set by reading the configuration register in the FPGA. The configuration register can be edited through the USB port or from the NIC unit via the SFP+ port.

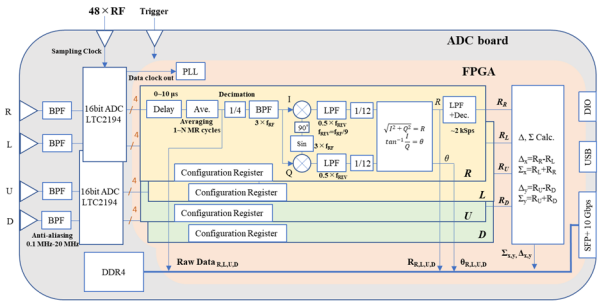

Figure 6: Block diagram of the ADC card.

Network Interface Controller Unit

The NIC unit under development is responsible for communicating with the ADC card though the private optical network, acquiring a set of waveform data from different ADC cards, and sending it to the data storage system. Furthermore, it communicates with an EPICS IOC (Input output controller) via a dedicated API (Application Interface) and delivers the COD data and alarm status onto the control network. The user can write the set value to the configuration register of the ADC card via EPICS records and then read the set value back to the EPICS records.

Data Storage System

The data storage system under development stores a large amount of waveform data sent via UDP from the NIC unit. This system has 16 SATA 16 TB HDD storage and builds RAID5 or 6 with a dedicated hardware RAID card.

In UDP communication, the order in which the data flames transferred from the NIC unit are received is different, and there is no protection against flame data loss. It has the advantage of having less overhead during transfer and can be processed at high speed. The input communication card of the data storage system rearranges the data flames based on the time information in the header information of each flame data and organizes them into a file at each MR cycle. When a flame loss occurs, the user is notified, but no retransmission request is made.

A large amount of waveform data is written in this file, however, the user usually needs only a part of the data, such as the beam oscillation data immediately after beam injection and beam motions when the machine status is changed. It is inefficient to read all data in the file and search for analysis points. Therefore, we consider adopting the HDF5 format as a file system that can extract and read some of the data stored.

CONCLUSION

We are developing a next-generation BPM data processing system to replace the outdated BPMC system, a 19-year-old system since its design. In the new system components, an attenuator unit has been developed and is in mass production. We are currently fine tuning the circuit.

We are now conducting a design study for the ADC card, NIC unit, and data storage system. We plan to complete these developments by JFY2023. Additionally, we plan to build a part of the full system with limited modules in JFY2024, and launch a new system in JFY2025. However, the availability of the FPGA chip, Arria10 270, used in the ADC card is now poor, and there are no prospects for full mass production. Although it appears to be improved in the future, it is necessary to closely examine the FPGA production status.

REFERENCES

[1] K. Satou *et al.*, "Beam Diagnostic System of the Main Ring Synchrotron of J-PARC", in *Proc. HB'08*, Nashville, TN, USA, Aug. 2008, paper WGF11, pp. 472-474.

[2] T. Toyama *et al.*, "Performance and Upgrade of BPMs at the J-PARC MR", in *Proc. IBIC2012*, Tsukuba, Japan, Oct. 2012, paper MOPA26, pp. 107-111.

[3] S. Igarashi *et al.*, "Accelerator design for 1.3-MW beam power operation of the J-PARC Main Ring", *Prog. Theor. Exp. Phys.* vol. 2021, p. 033G01, 2021. doi.org/10.1093/ptep/ptab011

[4] T. Toyama *et al.*, "Recovery and check of the switching relay in the BPMs in the J-PARC MR", presented at the IPAC'23, Venice, Italy, May 2023, paper THPL104, to be published.

[5] T. Asami *et al.*, "High accuracy optics measurement in JPARC MR for 1.3 MW upgrade plan", in *Proceedings of the 19th Annual Meeting of Particle Accelerator Society of Japan*, August 29 – September 1, 2023, Funabashi, Japan.

[6] K. Satou *et al.*, "Development of Signal Attenuator with Low Reflection and Low Distortion for New BPM Signal Acquisition System of J-PARC MR", in *Proceedings of the 19th Annual Meeting of Particle Accelerator Society of Japan*, October 18-21, 2022, Online (Kyushu University), in Japanese.

[7] "OKITA RELAYS CATALOG", OKITA Works Co., Ltd.

Content from this work may be used under the terms of the CC-BY-4.0 licence (© 2023). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI