# SOLEIL NEW PLATFORM FOR FAST ORBIT FEEDBACK

R. Bronès<sup>†</sup>, A. Bence, J. Bisou, N. Hubert, D. Pédeau, G. Pichon Synchrotron SOLEIL, Gif-sur-Yvette, France

### Abstract

SOLEIL is upgrading its Fast Orbit Feedback platform to withstand coming obsolescence of electronic BPM and future evolutions of the machine. This new platform has to be compatible with current boundary devices such as BPM electronics or corrector power supplies, but it also shall evolve to interface future versions of these systems. A MTCA based platform was designed and installed. It is integrated in the control system by mean of a OPCUA server, and care has been taken to seamlessly toggle the closing of the feedback loop on the former or new FOFB platform. This paper will present the first tests and results conducted to commission this new system.

# **CONTEXT AND SPECIFICATIONS**

SOLEIL is working on upgrading its accelerators to the fourth generation of synchrotron. SOLEIL II will bring outstanding performances, with a new beam lattice, renewed systems and cutting-edge technics. As presented in [1], the renewal of BPM electronics will be conducted prior to the long shutdown and machine upgrade. The current Fast Orbit FeedBack (FOFB) system, which is strongly embedded in these electronics, is to be ported on a new platform.

The evolution of the FOFB spreads on several years and must follow the numerous modifications and improvements that will bring SOLEIL II. The roadmap for this system can be summarized in Table 1, while evolutions of key points are underlined in Table 2.

Table 1	: FOFB	Roadmap
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	Evolution	Impact	
2024	FOFB running on new platform	Same performances	
2025	Added features	Faster lattice identification.	
2026	New BPM electronics	Loop latency reduced, data rate increased, correction bandwidth increased	
2028	SOLEIL II, new PSC	Loop latency reduction, dimension reduction, SOLEIL II performances	
2028 +	New correction algorithm	Increased performances	

### Table 2: FOFB Performances Evolution

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	Actual FOFB	Future FOFB
# BPM	122	180~200
# Corrector	50 H & V	44~60 H & V
Data rate	10 kHz	100 kHz
Correction BW	200 Hz	1 kHz
Loop Latency	350 µs	100 µs
Stability	10 % of beam size 20 μm H ; 0.8 μm V	2-3% of beam size 50 nm H & V

<sup>†</sup> romain.brones@synchrotron-soleil.fr

A versatile platform was elaborated and is presented in [1]. We will detail last additions and comment on the installations.

# Hardware Platform

The basis of the platform is a MTCA chassis, equipped with a SOC-FPGA board that host a SFP-FMC. The overall system is composed of five of these chassis, connected in a star topology. For denomination: a Central Node connected to four Cell Nodes. Communication between these nodes is a simple custom packet protocol, encapsulated in Ethernet frames and transported over optical fibers at 10 Gbps. This network was installed in the first months of 2023. Three full duplex fiber pairs are layed between Central and Cell Nodes, with one used and two as spare links.

The Cell Nodes are installed near BPM electronics in four different cells. For now they are connected as data spy to the running communication ring transporting the position data. After the upgrade of the BPM electronics, each Cell Node will be connected directly to a subset of them. Position data are grabbed, before being packeted and forwarded to the Central Node.

Correction packets are received back and transmitted to Power Supply Controller (PSC). A 1.25 Mbps RS422 UART link connects a Cell Node to each PSC. This limits the link length to 80 m and great care has been taken to position the Cell Nodes, each one serving PSCs in its own  $\widehat{R}$  cell cabinet and to three neighbour cells. Current PSC can  $\widehat{R}$ position the Cell Nodes, each one serving PSCs in its own only receive command from one driver. We selected and installed very simple RJ45-CAT6 cables, each one transporting 4 differential pairs. To ease commutation from actual drivers (BPM electronics) to Cell Nodes, electromechanical relays were temporarily installed to toggle the differential lines from one driver to the other. Each relay can toggle 2 differential pairs. All relays are powered from a central location, activated by a single switch lever. Switched off relays connect the PSC to the BPM electronics. For the new platform tests, we simply have to toggle the lever to switch on all relays and connect PSC to the Cell Nodes. This feature was well received and shortened greatly the set-up times for dedicated machine shifts. Ultimately, relays will be removed.

To provide the RS422 UART commands to each PSC, Cell Nodes are equipped with a custom made RTM board named CACTUS. These very simple boards receive LVCMOS single-ended signals from the AMC FPGA and translate it to RS422 pairs, transported to RJ45 outlets, allowing us to put eight outlets on the RTM, hence providing signals to eight groups of four PSCs. Except from the MTCA management, no other functionality is embedded on the CACTUS. These board will be decommissioned with the PSC and replaced with a new interface compatible with SOLEIL II new PSC.

# FPGA Firmware

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Fast or interface-specific functionalities are supported by the FPGA matrix present on the AMC. From the position data grabbing to the correction command sending, the data passes through FPGA logic blocs: Ethernet core, BPM communication decoder, correction computation, UART for PSC, etc. The overall firmware project is built with the help of FWK, the framework provided by DESY MSK. This framework allows to separate functionalities in deployable blocs, organized and versioned to prepare two slightly different systems: Central and Cell Nodes firmware. Further features of this framework are an easier integration with software control and process script to rebuild. This will keep the firmware project clean and allow further evolutions.

The Cell Nodes grab the position data exchanged on the BPM dedicated network. Every 100  $\mu$ s (10 kHz), 122 positions packets are exchanged, composed of (1) the BPM identification, (2) X and Y position data and (3) a frame number incremented at each iteration. Each Cell Node selects around <sup>1</sup>/<sub>4</sub> of these packets and forwards these to the Central Node. On the way back 100 correction packets are received from the Central Node, composed of (1) the PSC identifier, (2) the correction data and (3) the same frame number used to compute this correction. Each Cell nodes selects in the stream the correction data for the PSC it is connected to and forward it with the proper format on the correct output interface.

The latency from the position packet departure to Central Node to the corrector packet reception has been measured on field with a maximum value of  $4.5 \ \mu s$ .

The Central Node receives and aggregates all the positions data from the Cell Nodes. The correction processing scheme is kept identical to the previous implementation [2]: (1) Remove reference orbit to get the position error at each BPM, (2) space change from BPM position errors to PSC correction errors using the inverted obtained from singular response matrix. value decomposition and corrected with Tikhonov Regularization and (3) filter corrections signals with a 8 Hz low-pass filter given in Eq. (1), before broadcasting corrections to the Cell Nodes. Note that with the closedloop, perturbations will be attenuated by the inverse of this correction filter.

$$H(z) = \frac{64}{4096 - 4075 z^{-1}}$$
(1)

Data can be captured before and after the correction processing chain. On user demand, a few tens of seconds of data can be captured and pushed in a dedicated DDR memory for the on-board software. A sine waveform generator is also added on the data path. It can add a sine waveform, with programmable frequency, phase, amplitude and offset to the correction signal. These features are heavily used for the systems tests and commissioning. The global data processing scheme in the Central Node is pictured in Fig. 1.



Figure 1: Overview of data processing inside the Central Node.

# On-board Software

The FPGA-SOC provides a CPU which is running a Linux distribution built by Yocto. Regular operation can performed: SSH connection, NFS be mount, configuration scripting, logging, etc. To access the FPGA bloc functions programmed, we use a ChimeraTK generic server, which access FPGA register using Linux UIO and run an OPCUA server to provide access to remote control. The available FPGA registers are automatically understood by the software with a MAP files generated alongside the firmware. This feature allows name access to registers, from the OPCUA server. Identically, it is possible to access from python scripts and prompt with a ChimeraTK DeviceAccess python bindings. This features proved to be very helpful to conduct tests.

## Integration in the Control System

SOLEIL II control system will still be Tango. Control of the new platform must initially be compliant with current Matlab Script and GUI, with features and access tools gradually added. Base access to the on board functionalities will use a Tango Server / OPCUA client which will bring registers up to the Tango Level. Expert users or applications will be built over this server.

#### **NEW IDENTIFICATION FEATURES**

With the on-board sine generation and the local data capture, it is now possible to conduct easily identification of the system.

### Transfer Function Identification

This identification aims at measuring the frequency response, or Transfer Function (TF) from the PSC command to the BPM Fast Acquisition (FA, 10 kHz) data output. This identification is performed open-loop, the correction algorithm is disabled and outputs zeros and a sine waveform is generated for a single PSC. Data is captured for several frequencies in the band of interest, capture length is stretched to be able to record at least 100 periods of the sine.

Data capture and sine generator are synchronized on the same clock reference. The sine generator is composed of a 16 bits Numerically Controlled Oscillator with a programmable phase increment  $\Phi i$ . Equation (2) shows  $v_{sin}$  the normalized frequency to the data-rate which will be used for frequency analysis, preventing scalloping losses. Equation (3) shows how for each capture, we compute the complex Discrete Time Fourier Transform (DTFT) of all the BPM position at  $v_{sin}$  before dividing it by the PSC DTFT. With this, we have the TF gain and phase of the selected PSC to every BPM, at each frequency point captured.

$$\mathbf{f}_{sin} = \mathbf{f}_{datarate} \Phi_i / 2^{16} \rightarrow \mathbf{v}_{sin} = \Phi_i / 2^{16}$$
(2)

$$TF_{m,n}(v_{sin}) = \frac{DTFT[bpm_n](v_{sin})}{DTFT[psc_m](v_{sin})}$$
(3)

Each BPM has a different TF gain, depending on the Orbit Response Matrix (ORM). As we are interested in the overall shape of the TF, we first select the ten most significant TF and further normalize each one by its value at a given frequency (210 Hz) before aggregating the data by mean. The result is displayed on the Bode plot in Fig. 2. It shows an expected drop at 1.5 kHz coming from the notch filter, and a constant delay of 354  $\mu$ s and 332  $\mu$ s for X and Y planes respectively. We suspect that this difference comes from the vacuum chamber geometry at the corrector magnets location, resulting in a different latency from Eddy currents.



Figure 2: Bode plot of the measured TF. Blue and orange are one horizontal and one vertical PSC respectively.

#### Orbit Response Matrix Identification

This identification aims at measuring the ORM of the fast corrector magnets to BPM. Usually, this is performed by taking each of the PSC and apply a constant current step. ORM coefficients are deduced from the position difference induced on each BPM. Another approach, presented in [3] is to apply sine waveforms and perform a frequency analysis. This brings the possibility of frequency multiplexing to quicken the measure.

We tried this latter approach with our new platform. PSC in both planes were randomly selected by group of ten. One sine waveform is allocated and generated simultaneously by each PSC, from 223 Hz to 423 Hz, with 20 Hz gaps. For each group, 1.5 seconds of position data is captured. The measure has been repeated 4 times, with different groups and frequency distributions, allowing us several identifications for further corrections. For each capture, the DTFT at the ten sine frequencies are computed. We used a Blackman window on the data to reduce frequency leaking from one sine to the other, but in the future a better selected frequency gap will be used to minimize the leaking.

Two corrections are applied to the DTFT result before obtaining the ORM coefficients: (1) the phase is corrected by the identified constant delay, different to each plane, leading to real values. And (2) the module is corrected by estimating the TF shape on the measurement frequency band, for each PSC. Indeed, the results showed a  $\pm 2$  % module variation over the 200 Hz, different for each PSC. Once these corrections done, we observe the repeatability over the four repetitions in Fig. 3. We hope to improve this by performing a better identification of the TF shape for each PSC.



Figure 3: ORM measured coefficients. Each point is a PSC to BPM coefficient, its location gives the mean and peak to peak values from the 4 measure repetition. The error distribution is given for convenience.

# MACHINE TEST RESULTS

A few machine shifts have been dedicated to test the new platform correction. After some struggles with the corrector algorithm gain, we succeeded in closing the loop and achieving similar orbit stability compared to the previous system. We measured performances by assessing the integrated position PSD, and measuring the FOFB efficiency.

## Position PSD

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Figure 4 shows the power spectral density and its integration over the frequency band, for the mean orbit over all BPMs, obtained from the FA data. These signals are measured with a 5 mA beam stored, only one plane is shown for clarity. We can see that same performances are reached with the new platform. Sharp eyes can observe a slightly increase of the resonance crossover frequency. This comes from a small latency reduction obtained with our new platform. Indeed, the computation on the Libera starts after a waiting time of 60 µs after the loop iteration start, whereas the new platform starts the correction as soon as all position are received, which is around 30 µs after the loop iteration start.

The FOFB running on the new platform has been kept on while the beam was accumulated up to 450 mA without any issues.



Figure 4: Position PSD and integrated PSD, for x plane. Green is FOFB off, blue and red is FOFB running on new and old platform respectively. Measured with a 450 mA stored beam.

## FOFB Efficiency

This measure uses the on-board sine generator to add a sine wave on one selected PSC. The position orbit is then captured with and without the FOFB running. As for the TF identification, we compute the DTFT of the mean position over all BPM at the PSC sine wave frequency, only the module is kept. We consider efficiency as the ratio of the mean orbit oscillation with and without the

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FOFB running. By repeating this measure at several PSC frequencies, we have the efficiency over the band of interest, as plotted in Fig. 5. It shows an attenuation factor of 5 at 100 Hz and a resonance crossover frequency at 400 Hz. Comparison to previous system efficiency is not possible as that one is outdated. The new platform allows a very quick way to make this measurement, whereas the previous method required disabling a PSC in the correction algorithm and driving it with an analog external generator, which would takes too many time.



Figure 5: FOFB efficiency for several PSC.

## **FUTURE STEPS**

Integration to the Control System is still to be deployed and tested. This will allow SOFB and FOFB interaction which is mandatory for nominal operation. With this last addition, the new platform will be selected for operation, with the possibility to fall back to the previous system for the first few weeks.

#### CONCLUSION

The new FOFB platform based on MTCA was installed at SOLEIL and has reached the actual performances. This new platform unlocks new identification features that will be used to improve daily operations, diagnostic and correction scheme.

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