PAUL SCHERRER INSTITUT

PSI

SLS2 BPM & Feedback Team :: Paul Scherrer Institut

P.Baeta†, B. Keil, G. Marinkovic

RFSoC for Multi-bunch Feedback (MBFB) and Filling Pattern Feedback (FPFB)

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Introduction: SLS Upgrade – The SLS 2.0

Swiss Light Source (SLS) Upgrade, the SLS 2.0 project

- Replacement of the SLS storage ring, providing up to 60-fold higher brightness for hard X-rays.
- Modernization of aging systems, including the Multi-bunch (MBFB) and Filling Pattern (FPFB) Feedback Systems
- Evaluation of the Xilinx RFSoC as platform to implement the MBFB and FPFB for the SLS 2.0.
- 1st SLS 2.0 beam is planned for 2025 [1] .

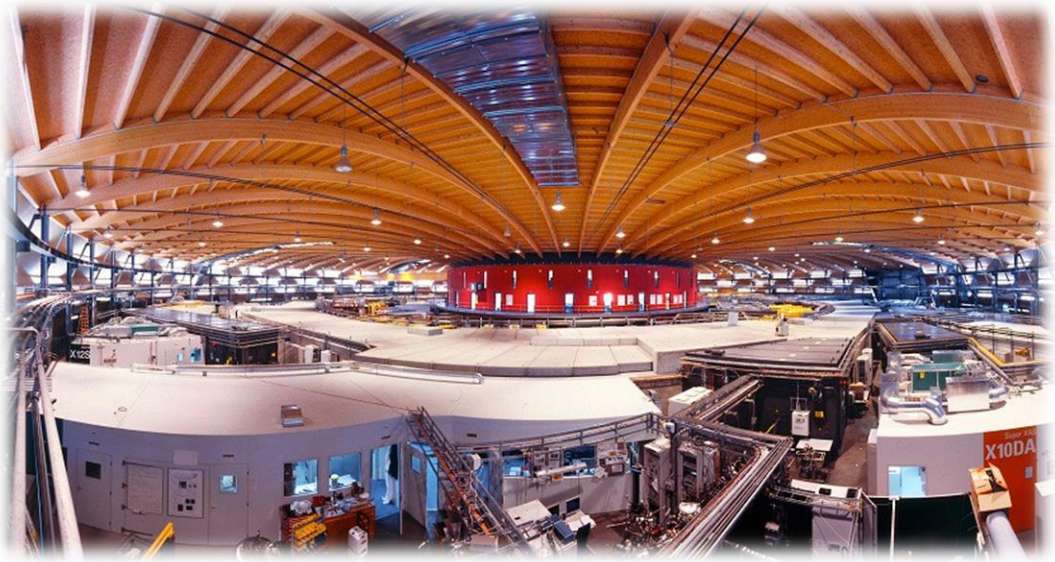


Figure 1 - Interior view of the Swiss Light Source (SLS) In user operation since 2001.

Introduction: Multi-bunch Feedback (MBFB) and Filling Pattern Feedback (FPFB)

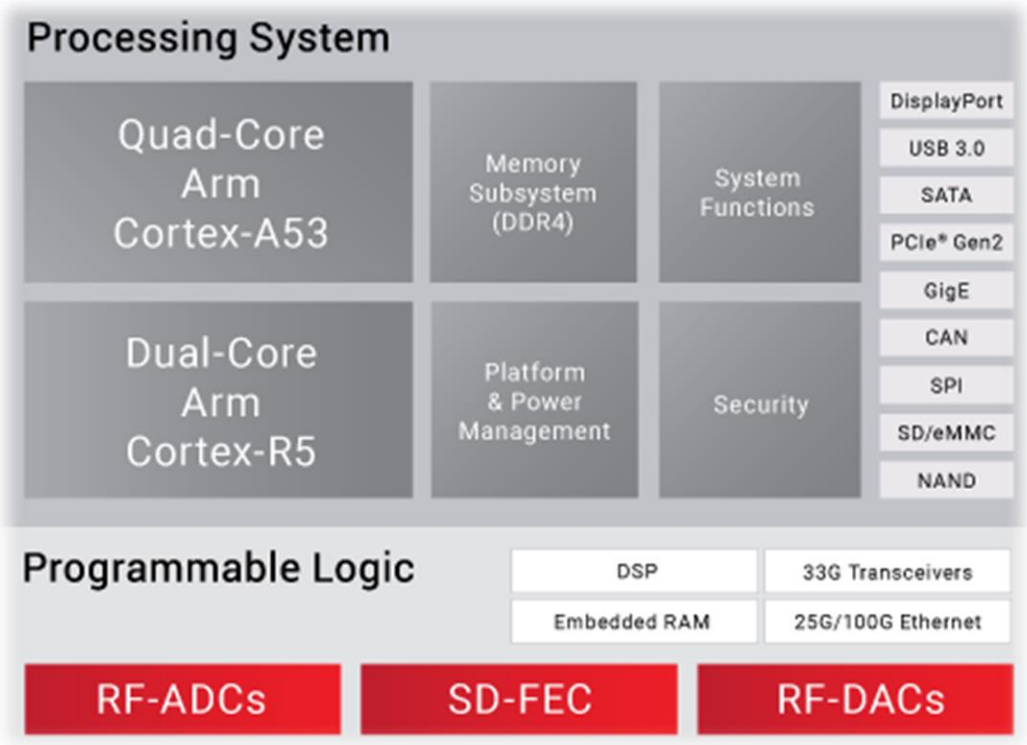
Multi-bunch Feedback (MBFB):

- Stabilize beam and avoid beam loss due to coupled-bunch instabilities (ion instabilities, resistive wall impedance, cavity HOM, etc.)
- Diagnostic tool:
  - Find source of beam instabilities
  - Excitation-damping measurement
  - Parasitic (X/Y/S) tune measurement

Filling Pattern Feedback (FPFB):

- Measure the charge of each RF bucket
- Control the injection time, adjusting the charge of each bunch given an user-defined pattern (filling pattern).
  - Improves orbit stability (BPMs have filling pattern dependent error)
  - Avoid HOMs (that are filling pattern dependent)

Hardware: RF System-on-Chip (RFSoC)



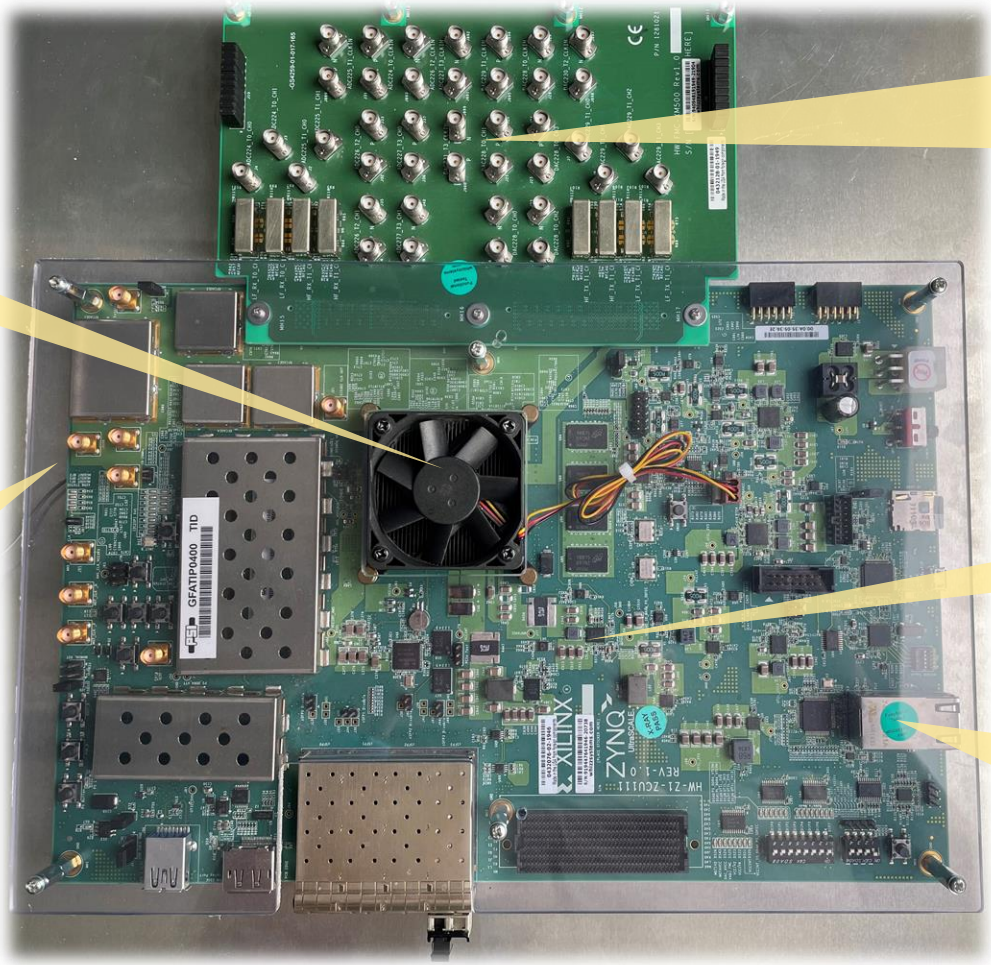
Zynq® UltraScale+™ RFSoC [2]

- **Integrates:**
  - Multiple CPUs
  - Resourceful FPGA Fabric
  - GHz-range ADCs and DACs
  - Various data storage and communication interfaces
- **Low ADC to DAC Latency**
  - ADCs (up to 4.0 Gs/s): ~46-101 ns
  - DACs (up to 6.5 Gs/s): ~24-116 ns
  - Total Latency: ~70-217 ns
  - Stable and reproducible (i.e. after a power cycle).
- **Stable temporal sample alignment among ADCs and DACs**
  - Multi-tile synchronization (MTS) mode.

ZCU111 RFSoC Evaluation Kit

Zynq® UltraScale+™ RFSoC

Add-on card breaks down the RFSoC ADCs/DACs inputs/outputs to SMA connectors



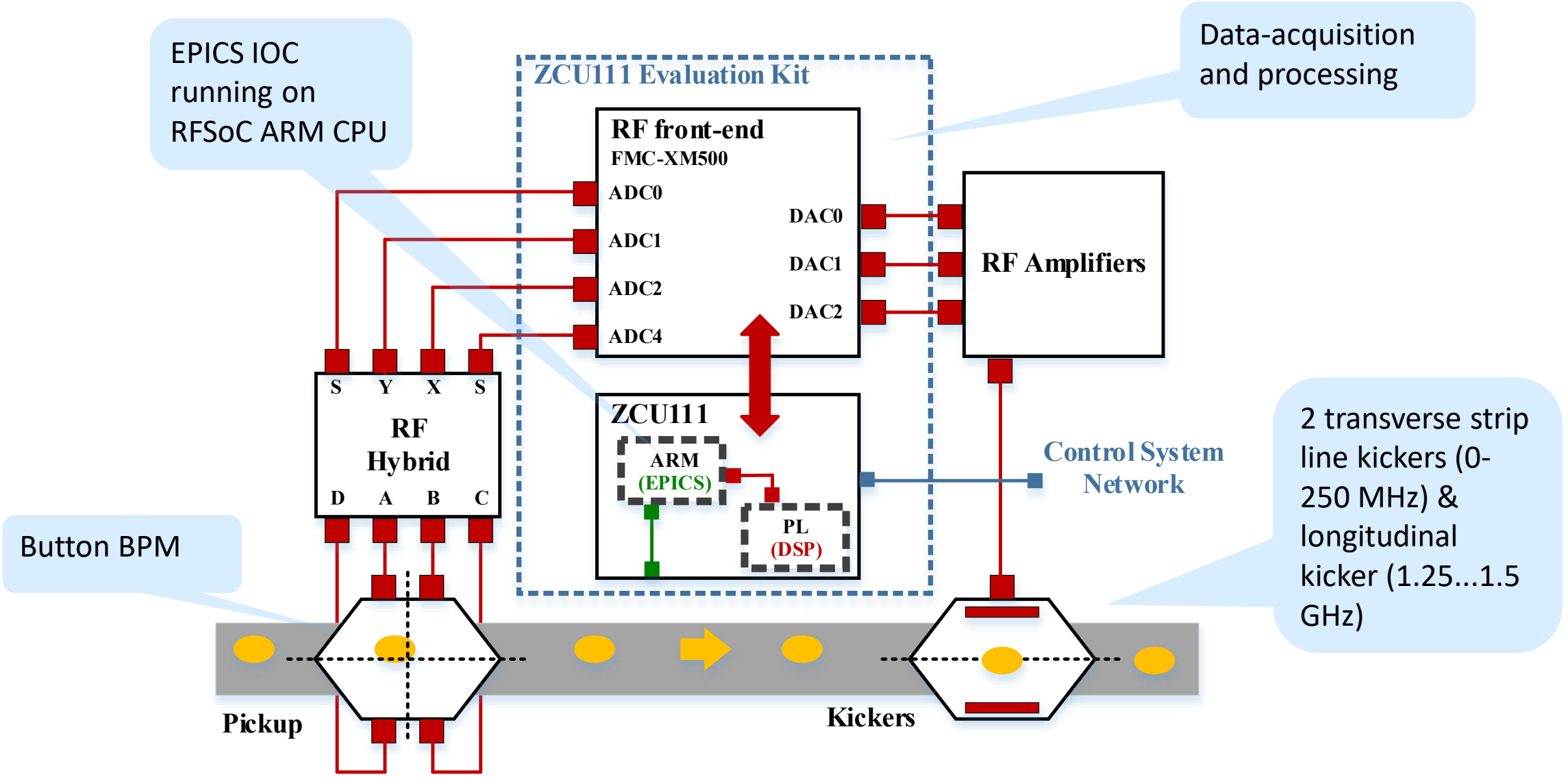
Approx. 10 thousand USD

Machine reference clock input (f_{RF} = ~500 MHz) synchronizes data converters and programmable logic (PL)

Ethernet for communication with control system network

Xilinx ZCU111 Evaluation Kit

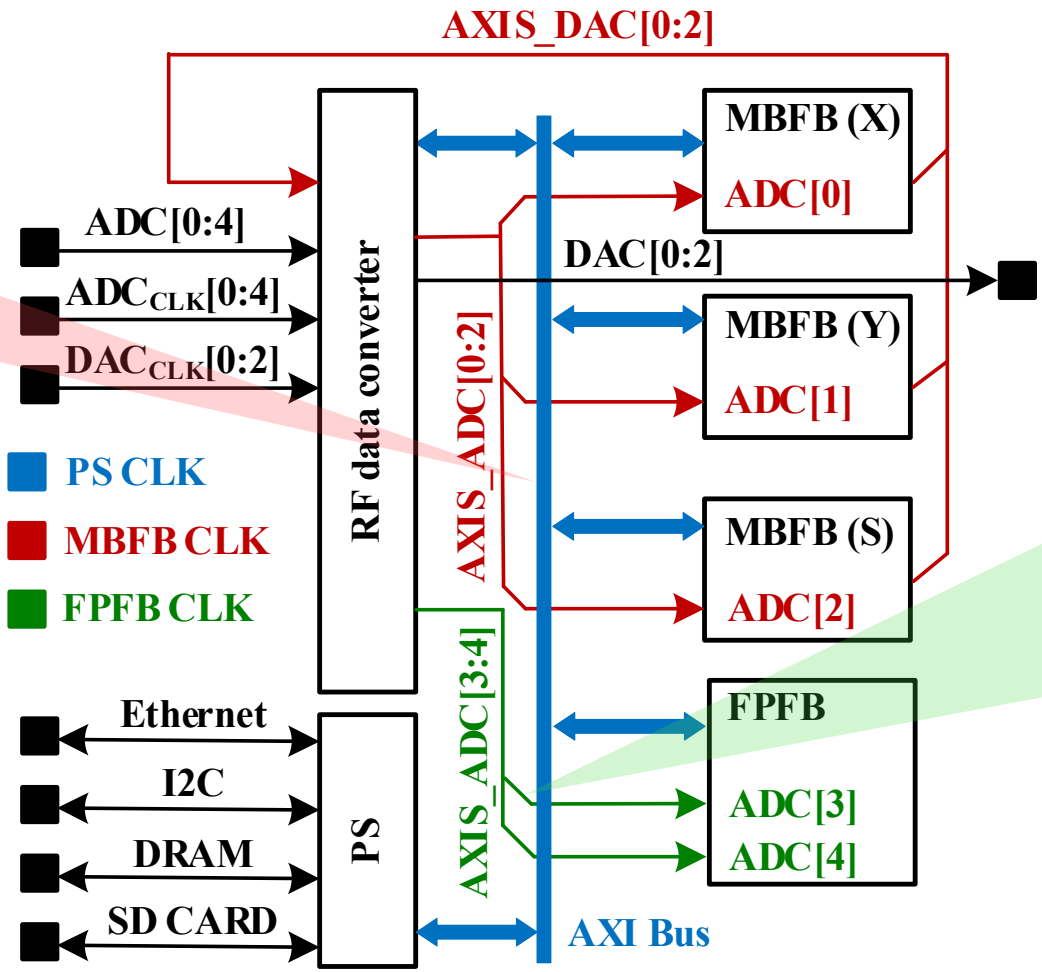
Hardware: MBFB/FPFB Test Setup at SLS



RFSoC hardware setup for testing the MBFB and FPFB at SLS.

Firmware: Overview

MBFB ADC/DAC clock period = 1/8 of nominal bunch spacing.
($f_S = 8 \times f_{RF} =$ ~4Gs/s)



Filling Pattern ADCs run at slightly different ADC clock, to acquire a fractional number of samples per beam turn. Such that an interleaved sampling scheme increases the effective sampling rate of the ADCs.

Unique firmware realizes the MBFB and the data acquisition for the filling pattern measurement.

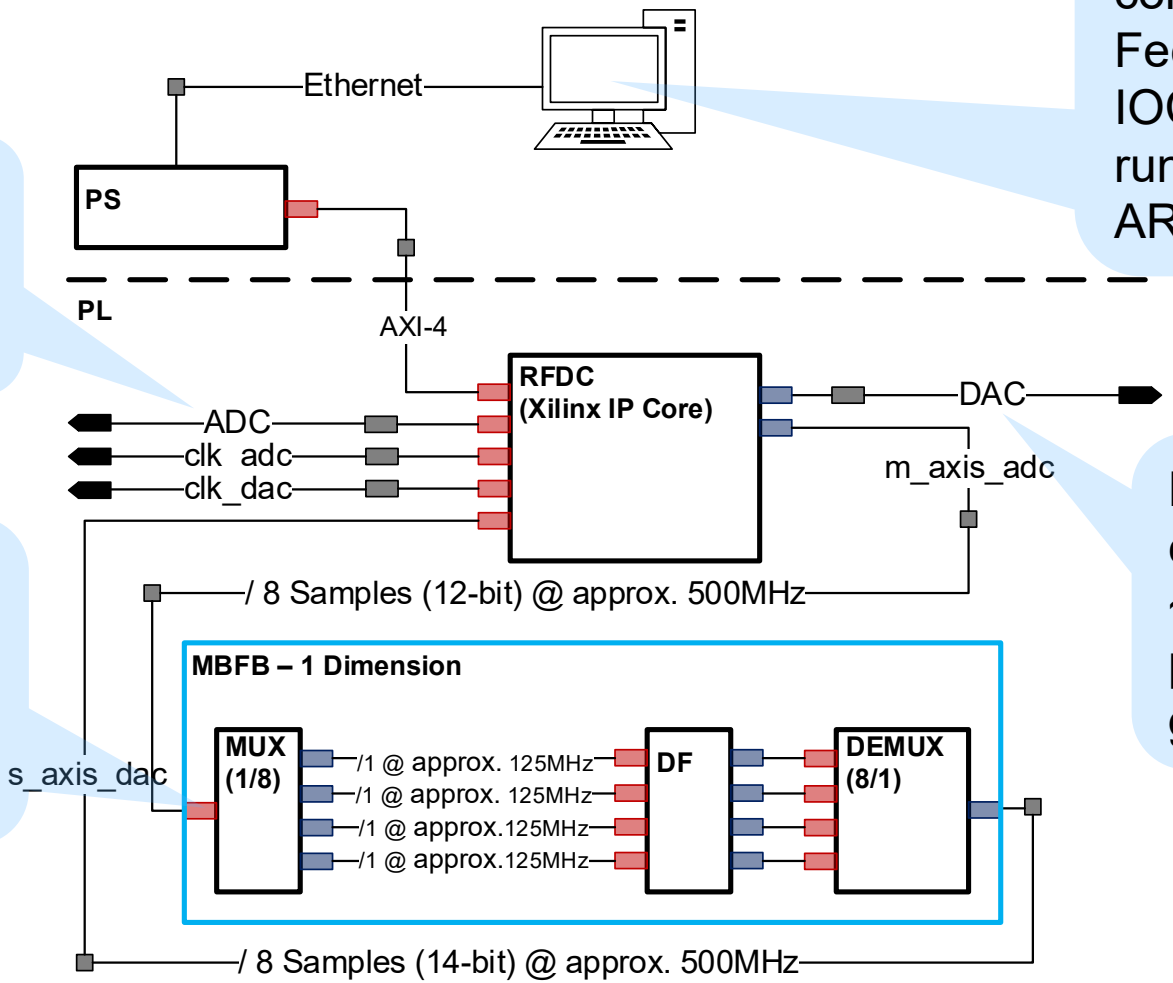
Firmware: Multi-bunch Feedback (MBFB)

User interface configures the MBFB Feedback via EPICS IOC channels running on RFSoC ARM CPU.

ADC sample the position signals at ~4Gs/s, 8 samples per bunch.

DSP path processes one out of eight samples and has data throughput of 500Ms/s

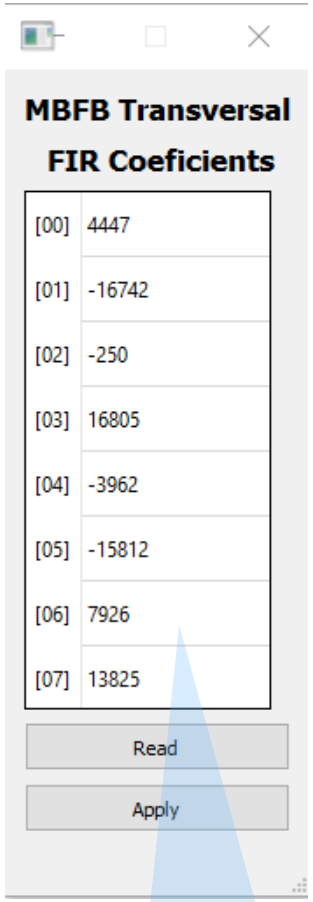
DAC generates the correction signals at ~4Gs/s, 8 samples per bunch, thus time granularity of 250ps



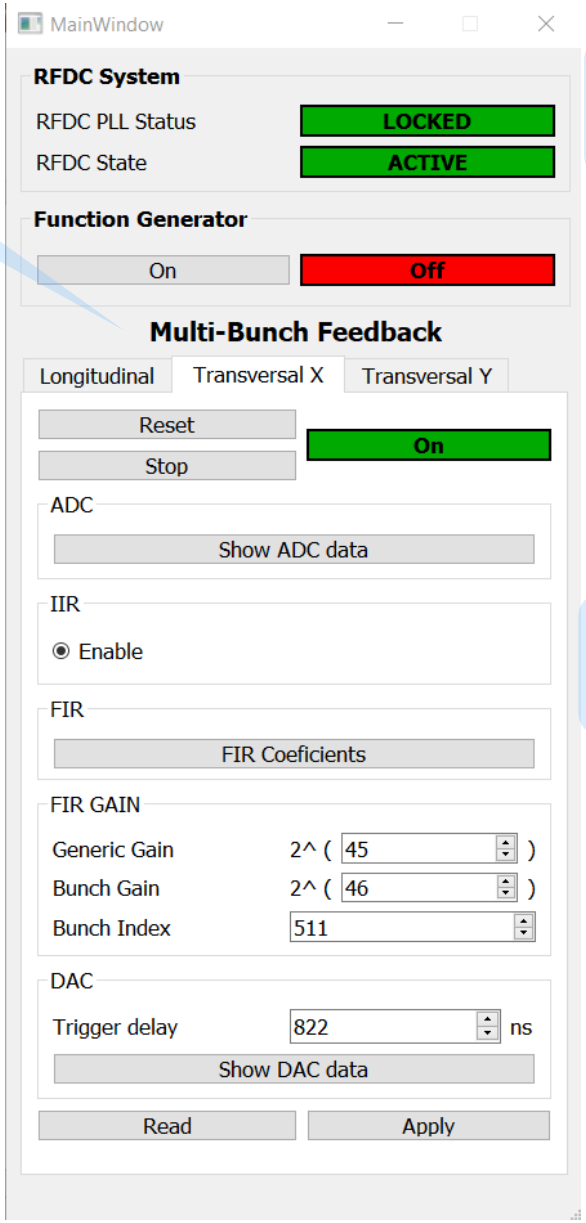
High-level block diagram of 1 dimension of the MBFB.

Software: MBFB – New Python GUI

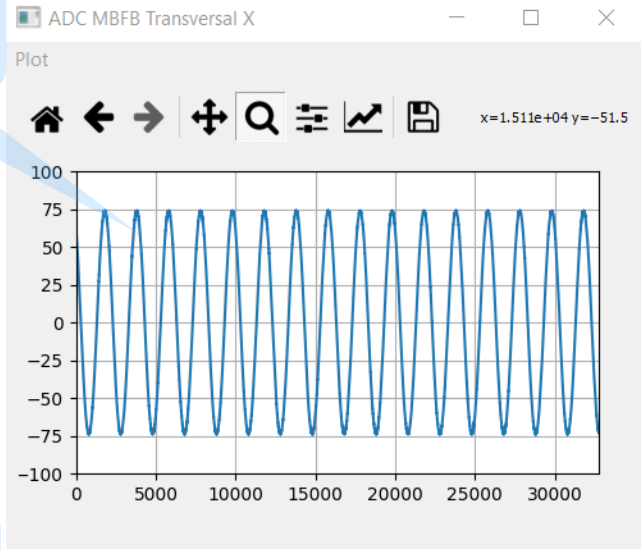
Main GUI



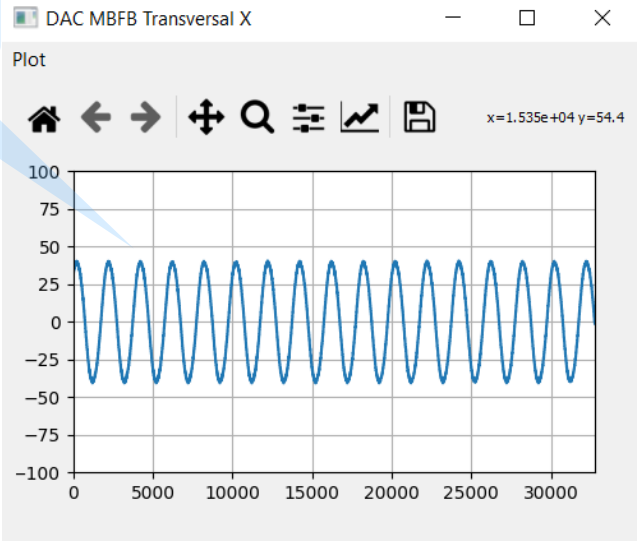
FIR Coefficients GUI



ADC data monitor

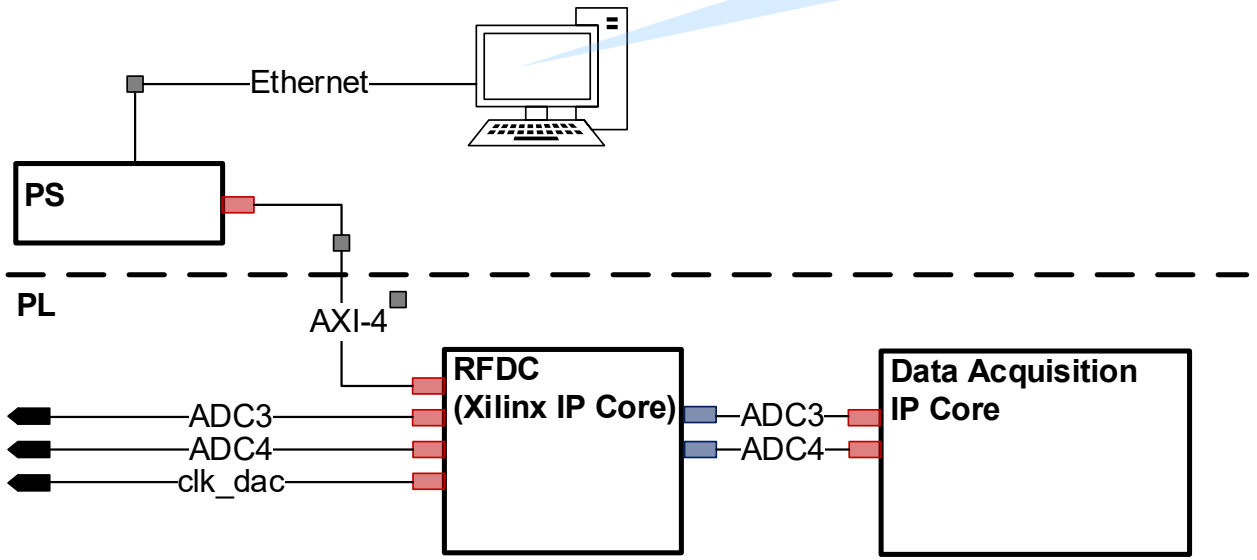


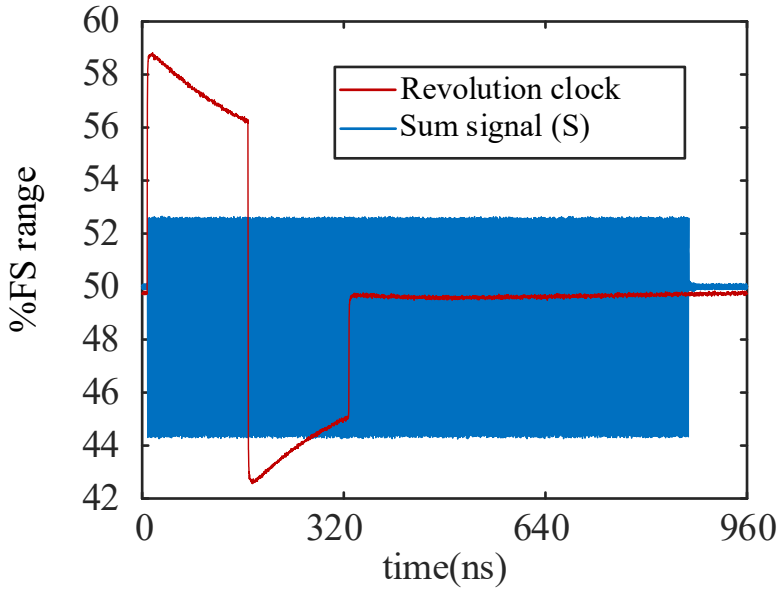
DAC data monitor



Firmware: Bunch Charge & Arrival Time Measurement

Software running in a PC read the acquired data via EPICS IOC channels, and processes the data offline





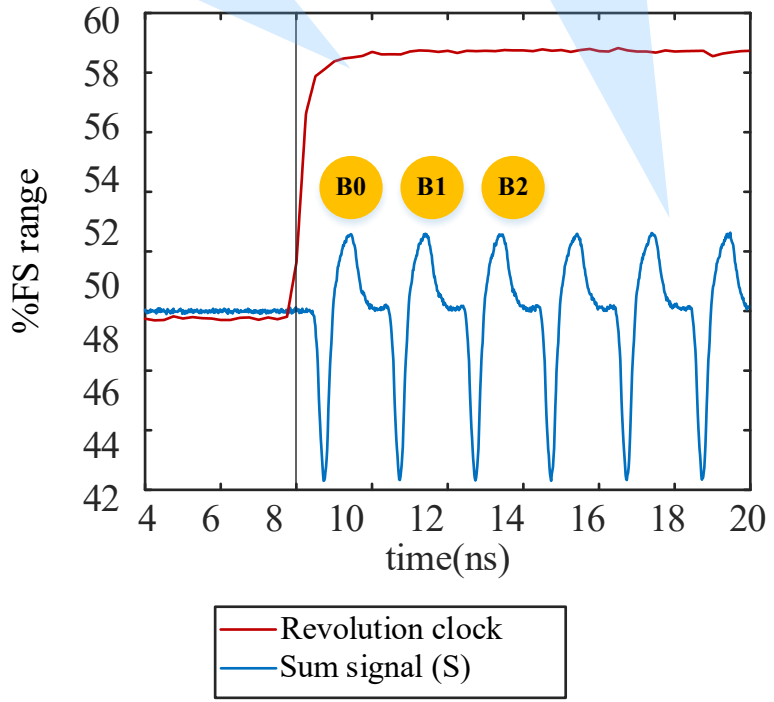
High-level diagram of data-acquisition firmware for the FPFB.

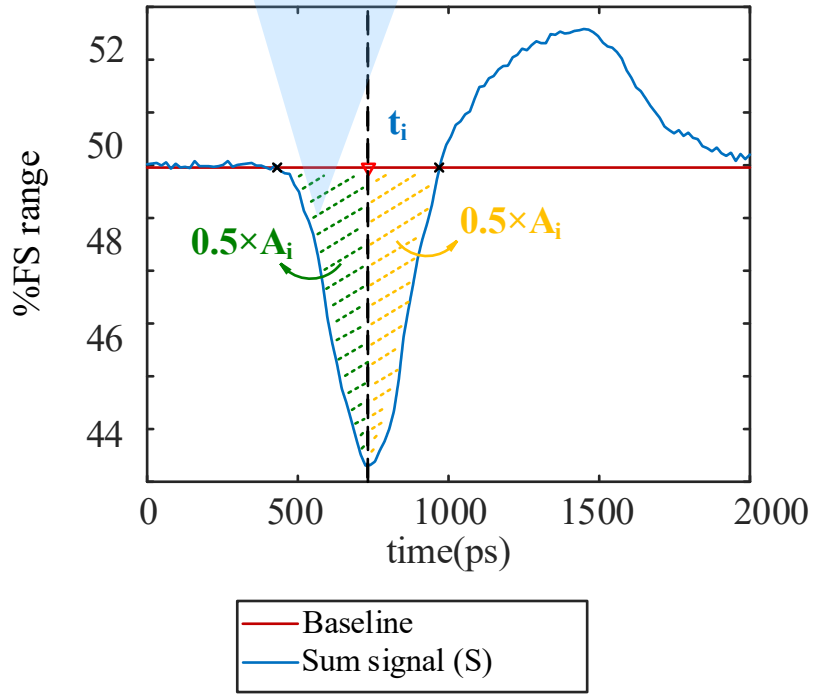
Software: Bunch Charge & Arrival Time Measurement

BPM sum signal (S) sampled by RFSoC ADCs and used for bunch charge & arrival time calculation

Revolution Clock used for bunch indexing

Area A_i below dynamic baseline $\propto$ bunch charge, and time t_i which splits A_i in half is an estimate for bunch arrival time

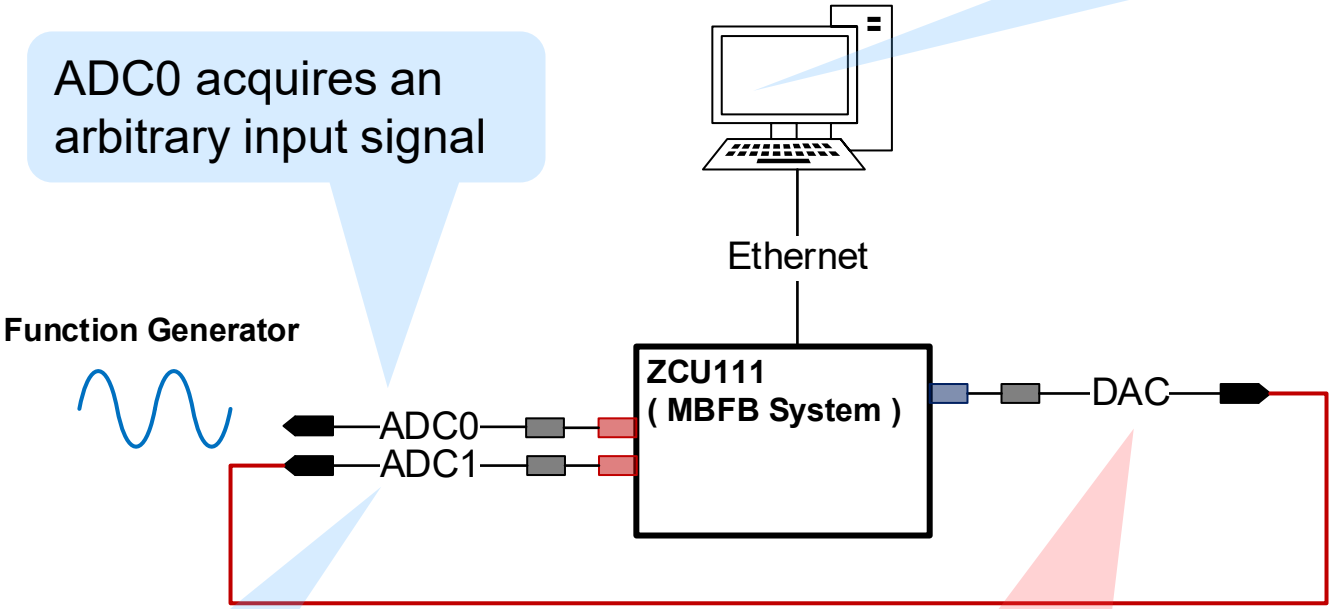


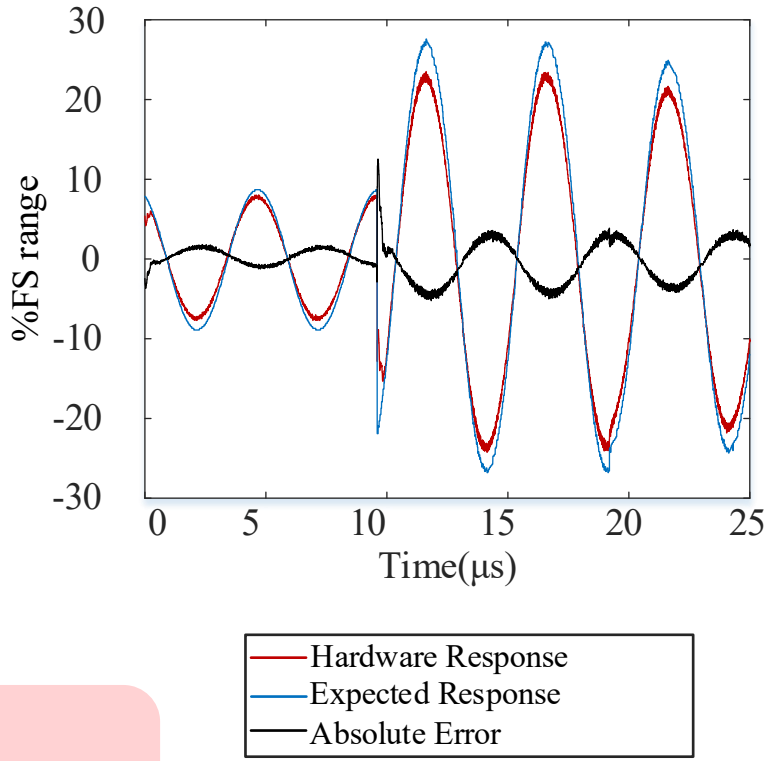


Results: MBFB Firmware - Functional Verification

Python model calculates the expected response for the ADC0 data and compares with the HW response

ADC0 acquires an arbitrary input signal





Hardware-in-loop (HIL) – Functional verification.

ADC1 acquires HW response of the MBFB

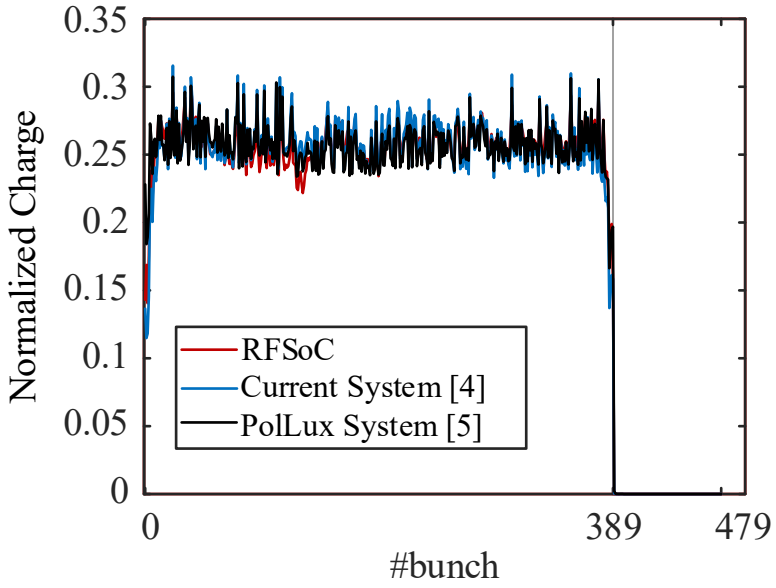
Analog loop-back path introduces attenuation of the DAC correction signal

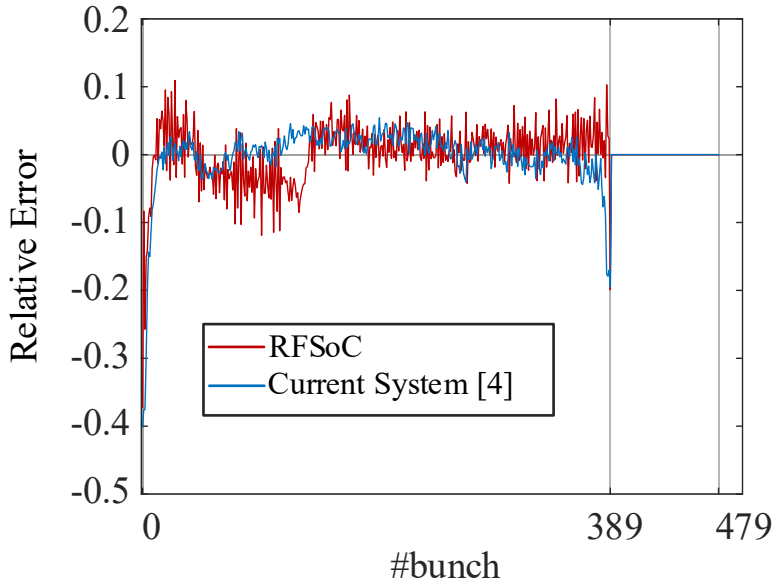
Result– Bunch Charge Measurement

PolLux system as reference (higher linearity, and negligible offset)

Bunch charge measurement with different methods:

- **System 1**: **PolLux system** - based on X-ray Photon counting system at PolLux beamline in SLS
- **System 2**: **RFSoC system** based on RF BPM sum signal
- **System 3**: **Current FPFB system** at SLS - based on visible photons and Avalanche Photodiode



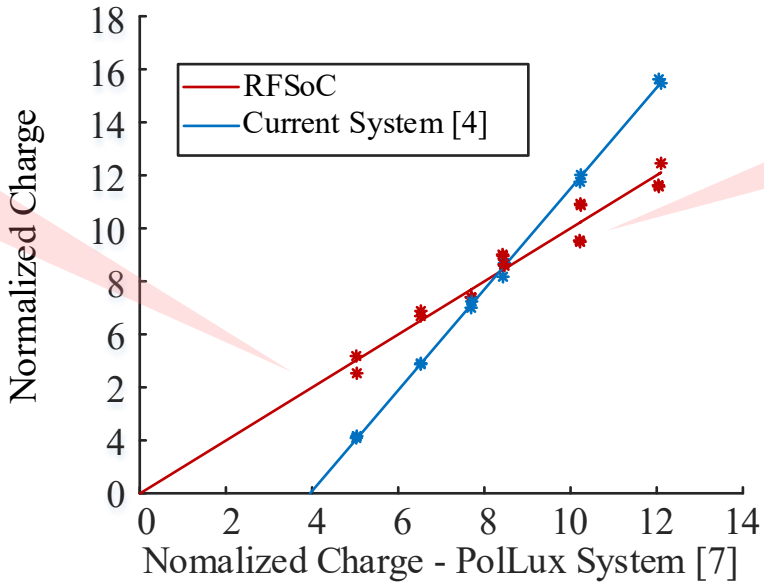


Result: Bunch Charge Measurement - Linearity

Linearity Test

- Charge of single bunch increased in steps to check linearity

RFSoC has good linearity & smaller offset than current SLS FP measurement.



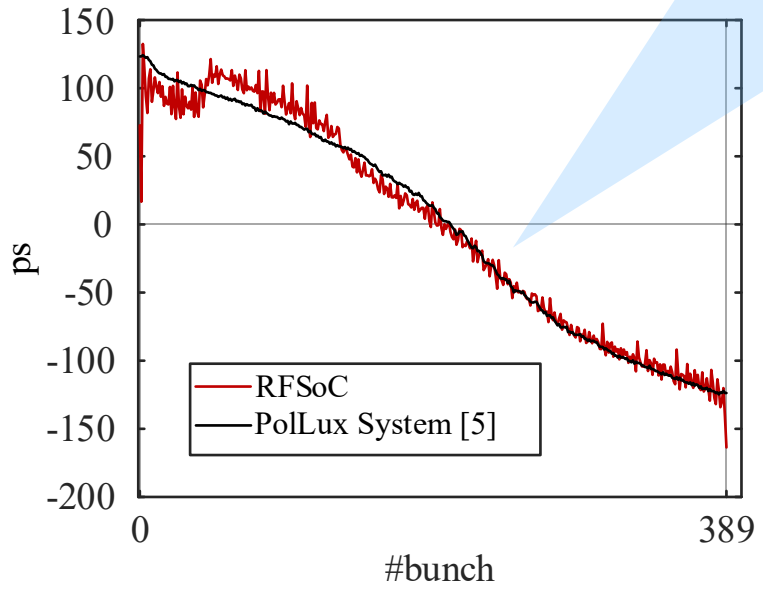
RFSoC noise can be improved by longer averaging (now only 128µs, vs. seconds for old FPFB & Pollux)

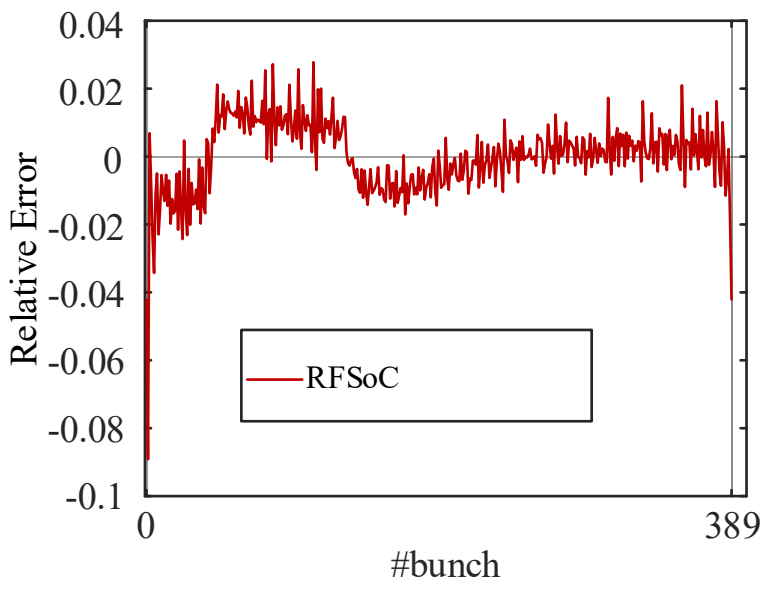
Result: Bunch Arrival Time Measurement

Bunch arrival time measurement with different methods:

- **System 1**: **PolLux System** - based on X-ray photon counting system at PolLux beamline in SLS
- **System 2**: **RFSoC System** based on RF BPM sum signal

Slope caused by gap in SLS bunch train (430 bunches filled, 50 empty) -> cavity beam loading





Conclusion and Outlook

Multi-bunch Feedback (MBFB):

- 3-D MBFB implemented on the RFSoC
  - RFSoC suitable for MBFB
- Next Steps:
  - Test the RFSoC MBFB system at SLS
  - Define & develop final hardware/firmware

Filling Pattern (FPFB):

- Filling pattern measurement implemented on RFSoC with raw BPM sum signal.
  - RFSoC is promising candidate for the SLS 2.0 filling pattern measurement via BPMs as alternative or principal solution.
- Next Steps:
  - Reduce systematic errors (i.e. impact of long cable reflections)
  - Reduce noise (longer averaging of the bunch charge)
  - Close FPFB loop.

Thank you!

References

- [1] A. Streun, “SLS 2.0, the Upgrade of the Swiss Light Source”, in *Proc. IPAC'22*, Bangkok, Thailand, Jun. 2022, pp. 925-928. doi:10.18429/JACoW-IPAC2022-TUPOST032
- [2] Xilinx, https://www.xilinx.com/products/boards-and-kits/zcu111.html
- [3] M. Dehler, G. Marinkovic, P. Pollet, and T. Schilcher, “State of the SLS Multi-bunch Feedback”, in *Proc. APAC'07*, In-dore, India, Jan.-Feb. 2007, paper TUPMA014, pp. 118-120.
- [4] B. Kalantari, T. Korhonen, and V. Schlott, “Bunch Pattern Control in Top-up Mode at the SLS”, in *Proc. EPAC'04*, Lucerne, Switzerland, Jul. 2004, paper THPLT186, p. 2885.
- [5] S. Finizio, S. Mayr, and J. Raabe, “Time-of-arrival detection fir tuine-resolved scanning transmission X-ray microscopy imaging”, *J. Synchrotron Radiat.*, vol. 27, pp. 1320-1325, 2020. doi:10.1107/S1600577520007262