# DUAL CHANNEL FMC HIGH-VOLTAGE SUPPLY

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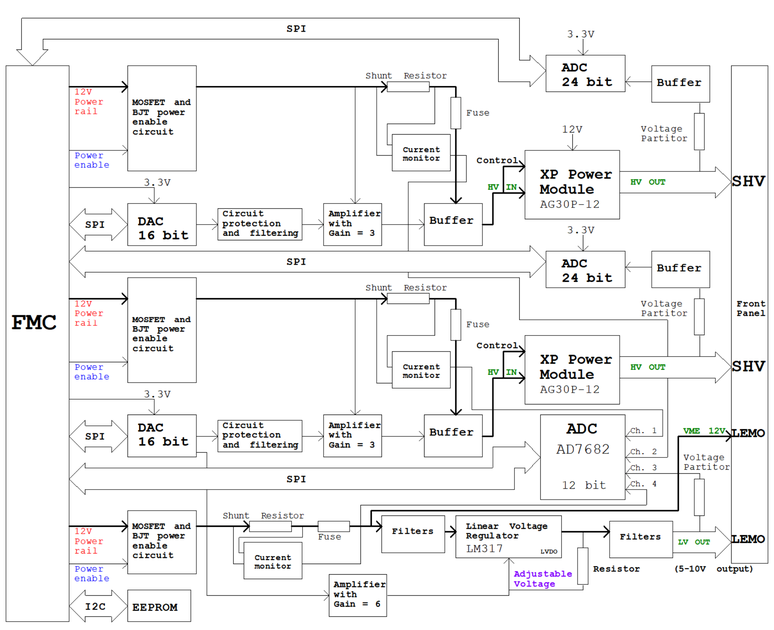
***Abstract:*** The Beam Loss Monitoring (BLM) detectors and electronics are installed in the CERN accelerators to provide measurements of the beam loss and to protect from excessive losses. The majority of the BLM detector types require voltage biasing up to 2000 VDC with a possibility to generate patterns to verify the connection chain from the detectors to the front-ends.

Currently, the power supply solution consists of Components Off-The-Shelf (COTS) large format power supplies with additional custom electronics and various interconnections to provide monitoring and remote control. For this reason, a market search has been done to identify a high reliability module suitable for dedicated BLM installations composed of a few detectors. The outcome of this market survey has justified the need to design a low-cost custom board, compatible with the CERN infrastructure and different detector types, as well as easily customizable to cover various installation architectures and needed voltage ranges.

The main characteristics of the developed board are: autonomy and full remote control; common hardware for different applications with a change of the DC\DC converter and a few components; smaller size than what is currently used as High-Voltage (HV) power supplies; multiple different high voltage or low voltage outputs for specific applications with the default design consisting of two positive high voltage outputs and one low voltage output; µV voltage sensing and mA current sensing capabilities; protection against overvoltage.

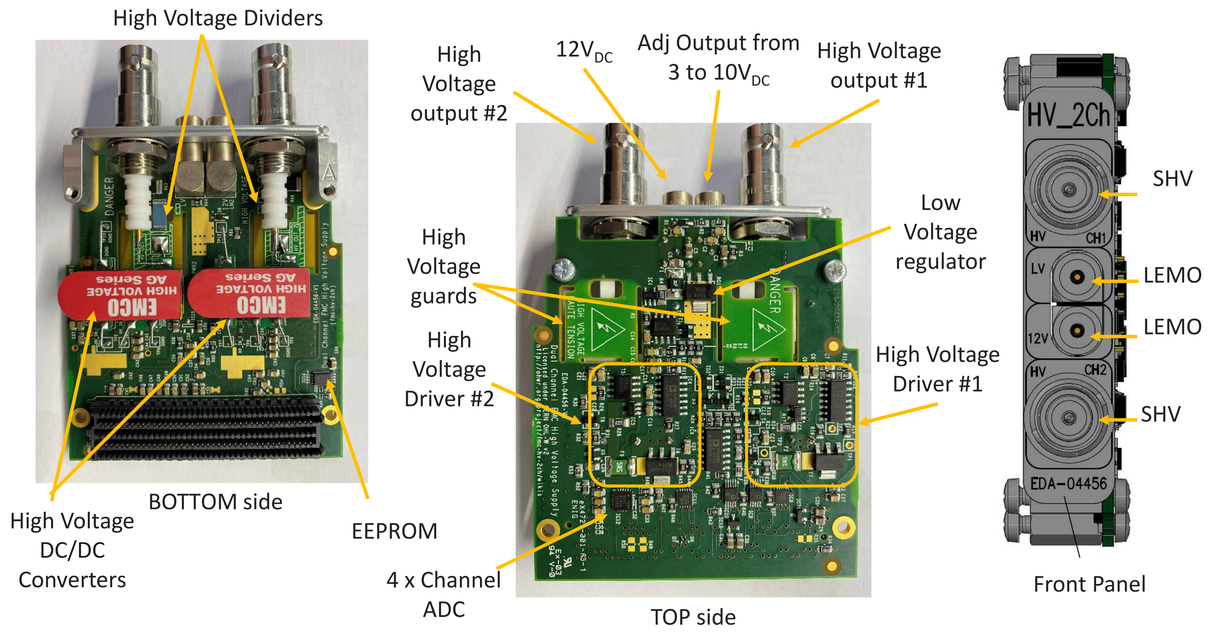
## Board architecture

An XP Power AG Series DC/DC converter is the core component in the developed design. The AG Series is a broad line of ultra-miniature DC to HV DC converters that sets an industry standard in high-voltage miniaturization.
From the FMC connector, the mezzanine receives the +12 VDC power rail for the HV DC/DC converters and the +3.3 VDC power rails to the digital circuitry. A power enable digital signal is used to control, using Pulse Width Modulation (PWM), the +12 VDC rail making it possible to adjust the main HV DC/DC accordingly, with the XP Power AG series that works at 12 VDC or at 5 VDC, while the voltage regulator is fine-tuned by a DAC and additional dedicated circuitry.




The high-voltage output is monitored by a high-resolution ADC through a 1:1000 high-voltage divider. An auxiliary ADC measures the primary side of the HV DC/DC converter to indirectly monitor the power consumption at the output, and at the same time to allow a supervision algorithm to control power dissipation.

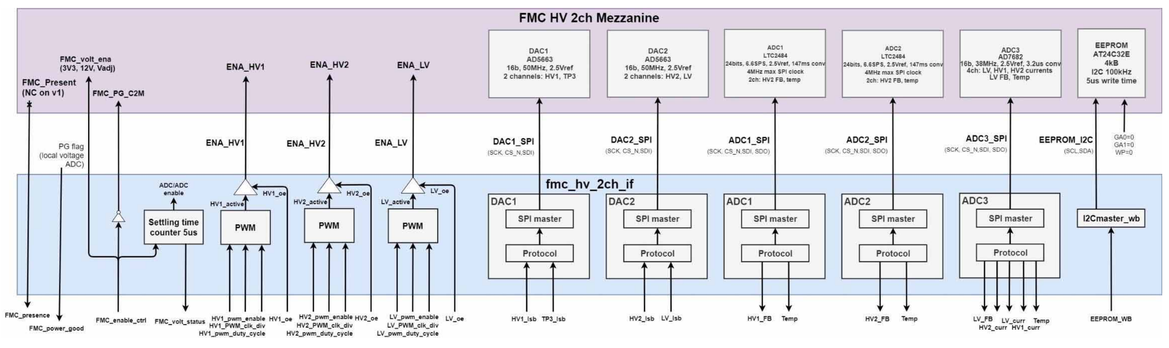
## Board Layout




The PCB design required particular attention due to the presence of high-voltage, which is a potential source of safety issues, electrical discharges, and current leakage. For these reasons, dedicated high-voltage guards have been created on the PCB by applying the following rules:

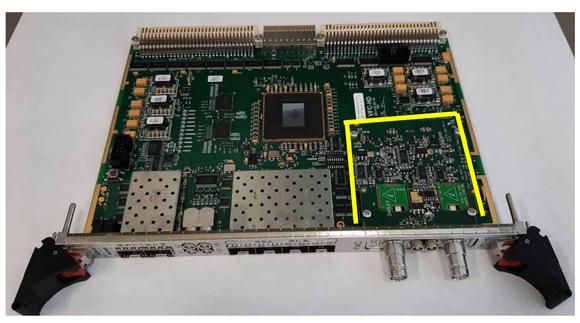
- A single wire connects the SHV connector to the HV DC/DC converter and the PCB pad for the HV divider.
- Except for the soldering pad of the HV wire (bottom side), all copper is removed in all PCB layers up to the top side in the HV high area.
- The minimum distance between HV copper and all other lines is greater than 5 mm in all directions.
- The PCB substrate has a Comparative Tracking Index (CTI) 0 for voltages greater than 600V.

## Firmware




A low-level generic firmware was designed to validate the HV FMC prototype. The firmware implements control and status signals, 3 PWM modules, 5 SPI masters associated with a custom Finite State Machine (FSM) managing the ADC and DAC protocols and an I2C master with a standard Wishbone slave input interface.

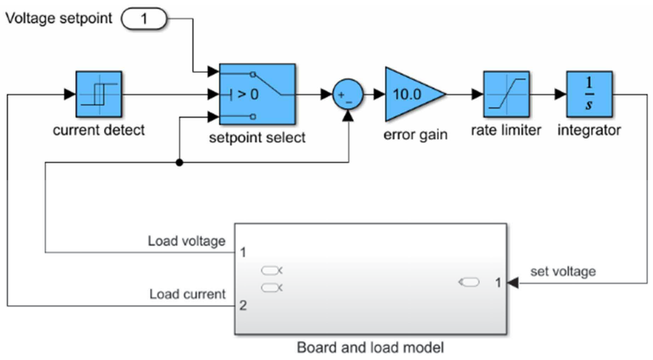
This basic firmware was tested on a complete GHDL/ GTKWave testbench instantiating a model of every component of the FMC. All the files are available on the Open Hardware Repository (OHWR).



Integration on the Intel Arria V based VME64x carrier for one High Pin Count (HPC) FPGA Mezzanine Card (FMC, VITA 57) called VFC-HD

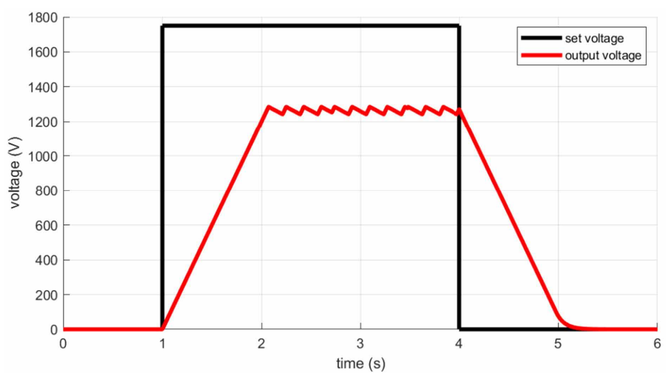
## Control Algorithm

A control algorithm with two main functions is required inside the FPGA to operate the board efficiently. Firstly, it oversees the output voltage and steers it as close as possible to the set point, especially in the case of unknown load behaviour, i.e. capacitive or inductive. Secondly, it makes sure that the sensitive core module of the board that generate the high voltage is operated safely, protected against overvoltage and overcurrent.




The algorithm is modelled with Matlab/Simulink to test the different strategies for the feedback controller. The left figure shows, as blue blocks, the feedback-based voltage and current controller topology that was selected. It is built around one integrator with a gain and a saturation to set the maximum voltage rate.

The current controller is built with a comparator that switches the voltage setpoint in case of overcurrent. The right figure shows a simulated example of current limiting mode in case of a low impendence load. The comparator hysteresis is programmable to adjust the voltage oscillation around the maximum current (red line).

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