Fast Orbit Feedback Upgrade at SOLEIL

R. Broucquart, N. Hubert
Synchrotron SOLEIL

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SPECIFICATIONS	Actual FOFB	Future FOFB (SOLEIL II)
# BPM	122	~ 180
# Corrector	50 H & V	*To be defined*
Data rate	10 kHz	100 kHz
Correction Bandwidth	150 Hz	1 kHz
Latency (communication and computation)	100 µs	10 µs
Stability	10% of beam size 20 µm H & 0.8 µm V	5% of beam size 50 nm H & V

CONTEXT & GOALS

Obsolete BPM electronics (eBPM) will soon be upgraded.
They currently carry most part of the FOFB application.

We will relocate the FOFB application to a new, dedicated system platform.

This new platform will evolve with time.
- New specifications for the smaller beam of SOLEIL II
- Upgraded boundary systems: eBPM, corrector magnet power supply controller (PSC), timing system
- New features: improved monitoring, fast lattice parameters measurement...

System deployed on versatile hardware platforms, linked into a dedicated network.

Boundary systems are connected to Cell Nodes.
Custom interface for each system.
eBPM data aggregated and transferred to the Central Node.
Correction data received from the Central Node and dispatched to the proper PSC.

Centralized computation on the Central Node.
This allows more complex scheme for correction algorithm.

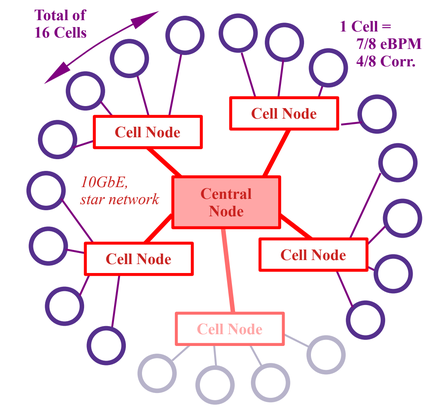
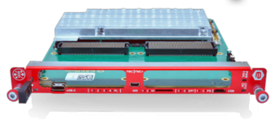


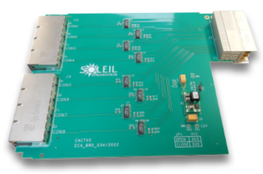
Figure 1 - Proposed two level star topology. As SOLEIL II increases the number of systems, the network will expand by adding a Cell Node.

MTCA PLATFORM

1U simple MTCA.4 chassis
11850-029, nVent
eMCH, no PCIE switching
Point to point backplane



AMC, Ultrascale+, Double FMC carrier
DAMC-FMC2ZUP, CAENels
Ultrascale+ SOC: FPGA+ARM cores
16+8 transceivers on FMC
White Rabbit support or dual LVDS signals for timing



Custom RTM with 32 RS485 TX
CACTUS, SOLEIL
8 RJ45 with 4 pairs each
Only TX drivers on board.
MTCA standard not fully implemented.

FMC quad SFP+
FMC-4SFP, CAENels

DEDICATED NETWORK

10GbE backbone communication
IP, UDP/TCP not needed.
Custom packets encapsulated in Ethernet frames.
One full frame = 149 position data or 248 correction data
One full frame transferred in 1.2 µs.

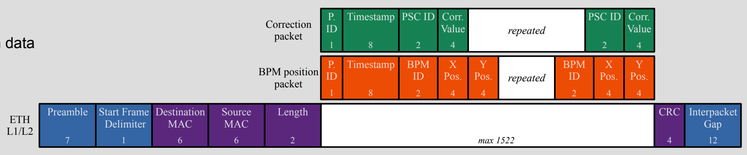


Figure 2 - Proposed Ethernet frames with encapsulation of a correction packet or a BPM position packet. Field size given in bytes.

Custom boundary system network
Interface, protocol dependent of the system (eBPM, PSC…)
For current eBPM: rocketIO serial data read (Diamond CC)
For current PSC: UART RS485 1.25Mbps

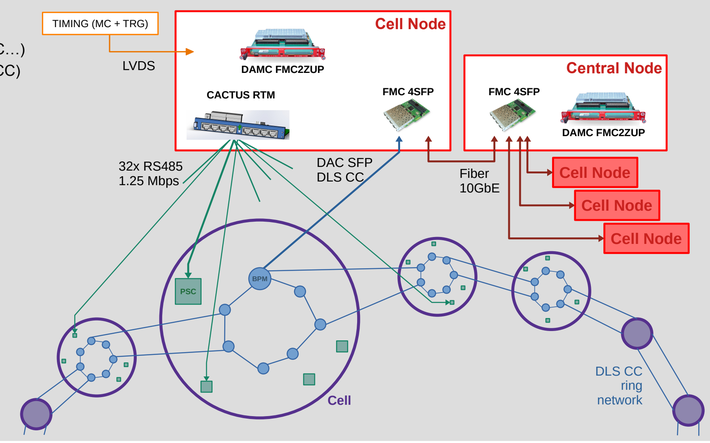


Figure 3 - Overview of boundary network with current systems. We still use the ring network until the upgrade of eBPM.

FPGA FIRMWARE

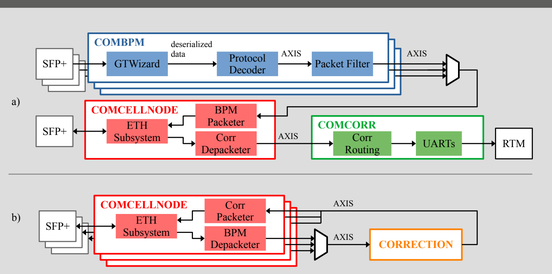


Figure 4 - Overview of FPGA firmware modules for a) Cell Nodes and b) Central Node.

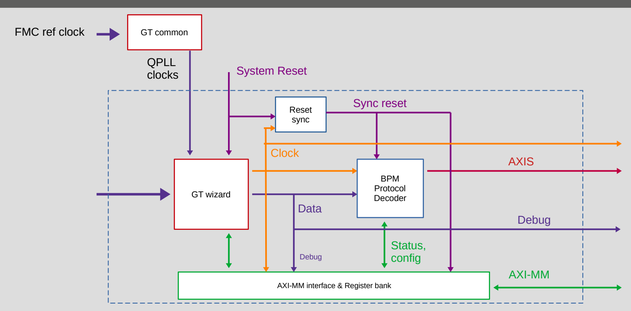


Figure 5 – COMBPM module structural architecture

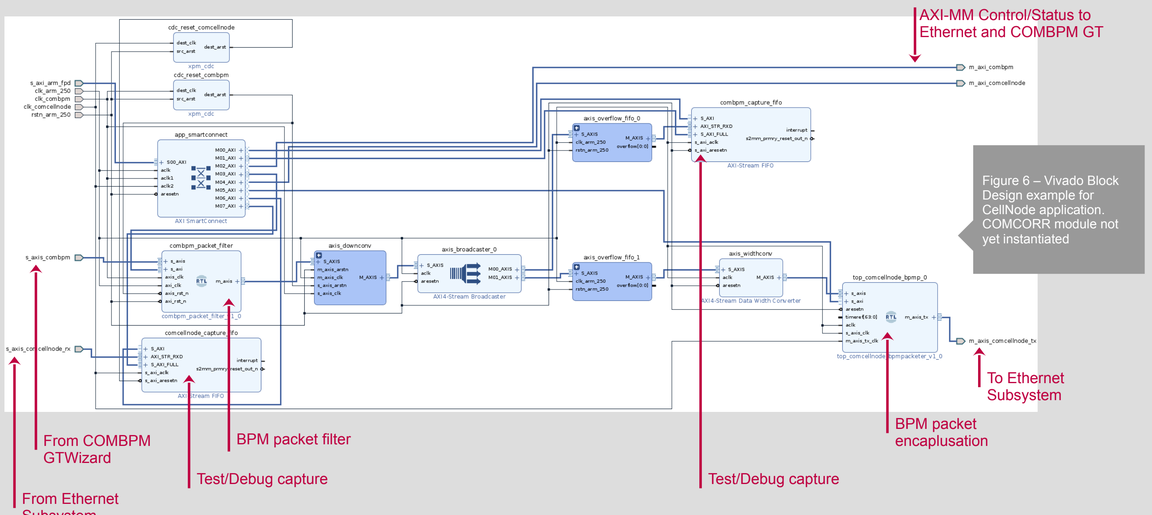


Figure 6 – Vivado Block Design example for CellNode application. COMCORR module not yet instantiated

DESY FWK
Automated project build, address map.
Compatibility with ChimeraTK.
Work exchange eased.

AXIS bus
Allow usage of generic, Xilinx IP

COMBPM Module
GTWizard configured for DLS CC
QPLL common used for COMBPM and COMCELLNODE

SOFTWARE CONTROL

Maximize auto-configuration
Follow system evolution: easy FPGA register mapping.
OPCUA discovery, generic Tango Server, ChimeraTK map configured with map files…

Step by step transition to new control
Support current operation (Matlab scripts)

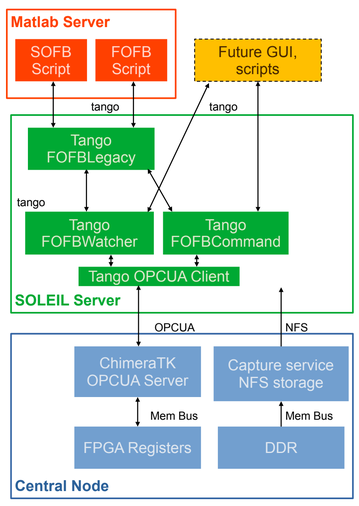
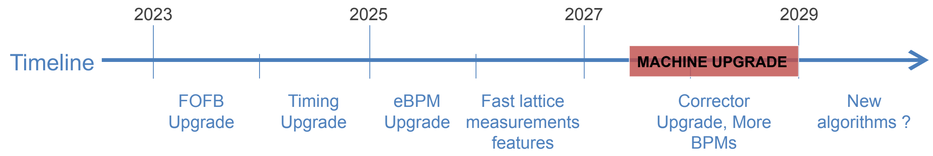


Figure 7 - Proposed software stack for system control.

NEXT PROJECT PHASES



BPM electronics upgrade
Data aggregation on the future eBPM ? Ring, grape ?
Use of Ethernet protocol ? Enable Ethernet switch usage.

Power Supply Controllers upgrade
Which protocol, command aggregation ?

Platform evolution
Increase SFP+ interface density: additionnal FMC, dual QSFP, MTP…
On the shelf AMC ?
New custom RTM ?

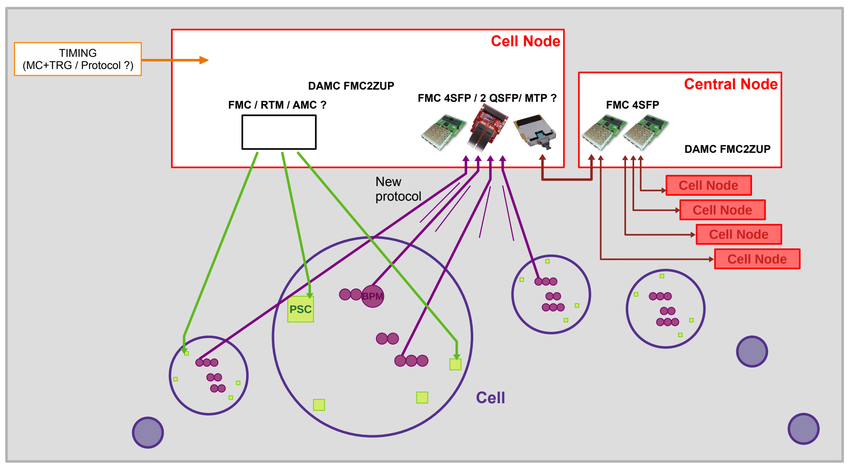


Figure 8 – Envisioned future boundary systems topology.