Design and Implementation of an FPGA-Based Digital Processor for BPM Applications

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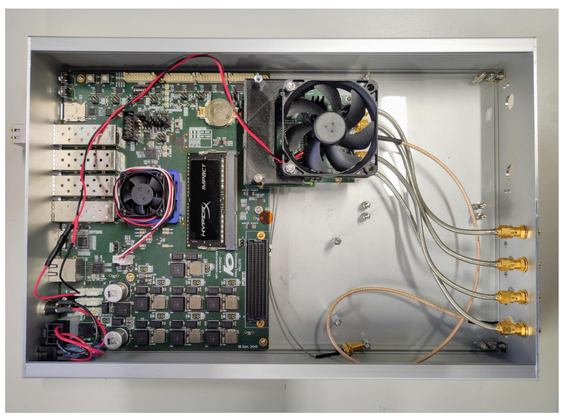
Digital Platform

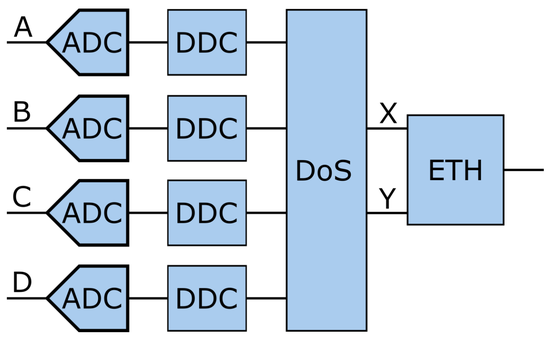
Digital signal processing has become a standard approach for realizing beam position monitor system, thanks to the availability of high-performance ADCs and FPGAs. In synchrotrons, it is well known that information about beam position lies in the amplitude of the detected signal from the pickups: due to typical beam fill patterns used in those machines and after a mandatory analog signal conditioning, the latter can be seen as a sine with a frequency equal to the RF frequency of the accelerator. So, to extract its amplitude after digitization, there is the need for a digital receiver and demodulator that can do it properly for extracting its amplitude after digitization, having a selectable data rate suitable for feedback applications. Then, position calculation algorithm like difference-over-sum can be applied on demodulated amplitudes, converting them into a real beam position, related to vacuum chamber dimensions using the scale factor. This architecture will be used for the new eBPM system of Elettra 2.0, the low-emittance upgrade of the current machine. The overall modular system and some of its components have been already presented in previous conferences, but in this paper we will focus on simulation and FPGA implementation of the complete digital processing chain, from ADC data to calculated position. The digital platform used has already been presented in previous papers: analog signals from the front end are digitized by an FMC card with four LTC2107, 16-bit ADCs running at 150.38 MS/s, that is 130 times the revolution frequency and phase-locked with it.

Thanks to the bandpass sampling technique there is no need for an analog downconversion stage: the 499.654MHz signal is seen by the ADCs as a 48.514 MHz sine, since it is folded back in the Nyquist zone corresponding to three times the sampling frequency. Obviously, this approach needs a high-performance, low-jitter clocking stage and an analog bandpass filter to reduce noise.

Then, ADC data is processed by an Intel Arria 10 GX FPGA: the high amount of logic gates and DSP resources render it possible to realize in digital the complete processing chain. Connections with external devices are assured by internal transceivers attached to SFP+ modules capable to go at a speed up to 10 Gb/s.

After demodulating the four amplitudes, the position is calculated with the well-known difference-over-sum algorithm (DoS). For an effective debug, user can choose data source and data rate nearly at every processing stage. High amount of samples can be stored in 8 GB an external DDR3 RAM memory, otherwise real-time data stream at 10 kHz (FA) or 1.156 MHz (TbT) can be sent to external systems through multiple Ethernet connections (1 Gb/s or 10 Gb/s).

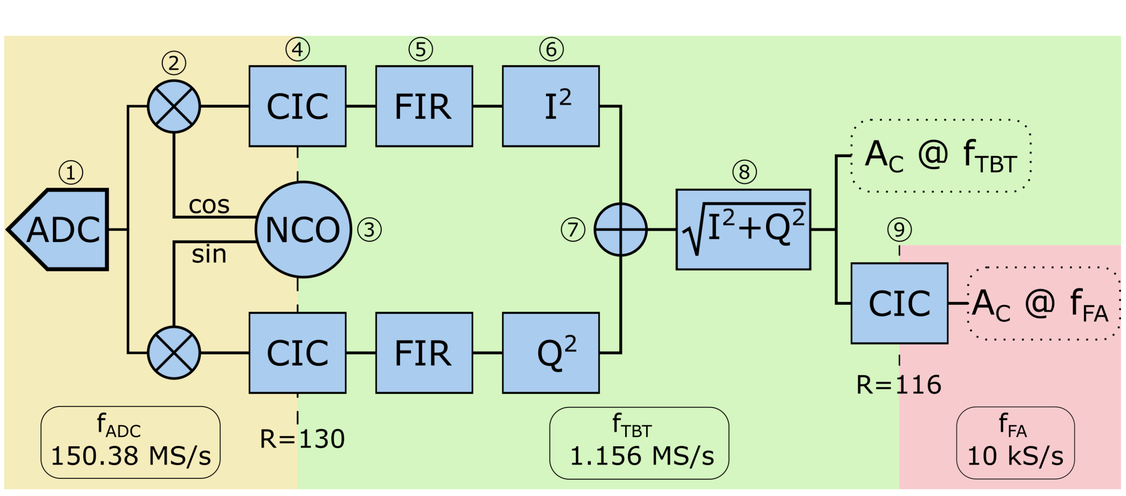




Digital Receiver

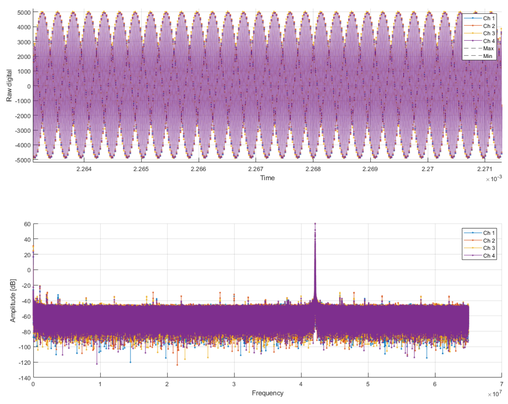
Moving to the digital domain, we chose a direct conversion digital receiver (or digital down converter DDC) paired with a quadrature demodulator. The input signal from the ADCs is shifted to the baseband by mixing (multiplying) it with a sine generated by a numerical controlled oscillator (NCO). A low-pass CIC decimator filter suppresses the high frequency components and reduces the data rate to turn-by-turn (TbT) frequency. Since CIC filters have a magnitude response that causes a droop in the passband region, a compensation FIR corrects it. To avoid dealing with complex numbers, there are separate I and Q paths so that it is possible to reuse the same filters for both components. Then, amplitude demodulation is performed by squaring I and Q, summing them and taking the square root of the result. All the processing is done using integers and not floating point numbers. More details on the implementation are listed in figure below, where only one channel is depicted:

1. ADC 16-bit signed data (two's complement) running at 150.38 MHz;
2. multipliers: digital version of mixers. They perform frequency translation of the input signal near to the DC and implemented using 18x18 bit hardware multipliers in DSP cells;
3. NCO (digital version of local oscillator): it generates a sine and cosine for I and Q processing with sufficient precision (18 bit), higher than ADC data and running at sampling frequency;
4. CIC decimator filter: suppresses the high frequency component generated by multiplication and reduces data rate to TbT frequency. The rate change factor is 130, 6 stages, differential delay equal to 1. Input and output are 32-bit wide, bits are reduced with Hogenauer pruning;
5. FIR compensator: it corrects CIC magnitude response, generated with a MATLAB appropriate routine. Symmetrical coefficients, 19 taps with 17 bit lengths, input and output 32-bit wide;
6. square: it is implemented directly in DSP cells, with 32-bit input and 64-bit output;
7. sum of I and Q square: it consists in a simple 64-bit adder;
8. square root: it is implemented using Intel IP integer arithmetic core, 64-bit input, 32-bit output;
9. second CIC decimator for changing data rate to 10 kHz as required by feedback. Rate change factor of 116, 6 stages, input and output 32-bit wide.

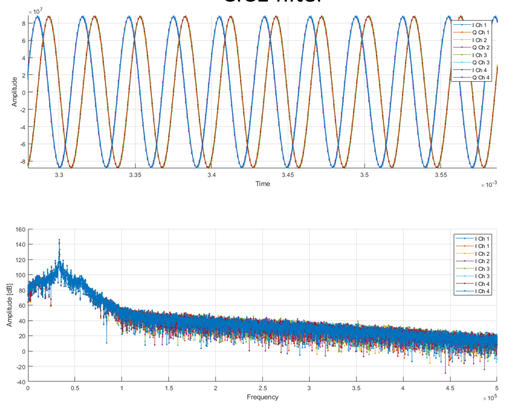


Simulation and Results

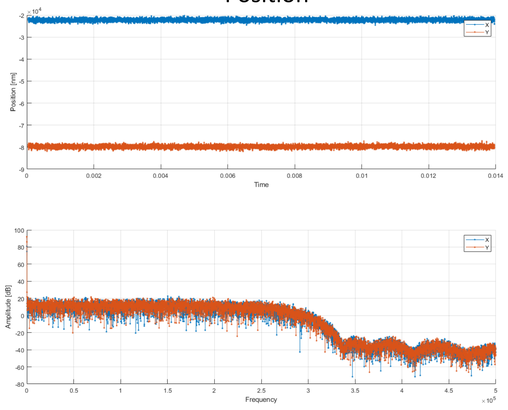
ADC raw data



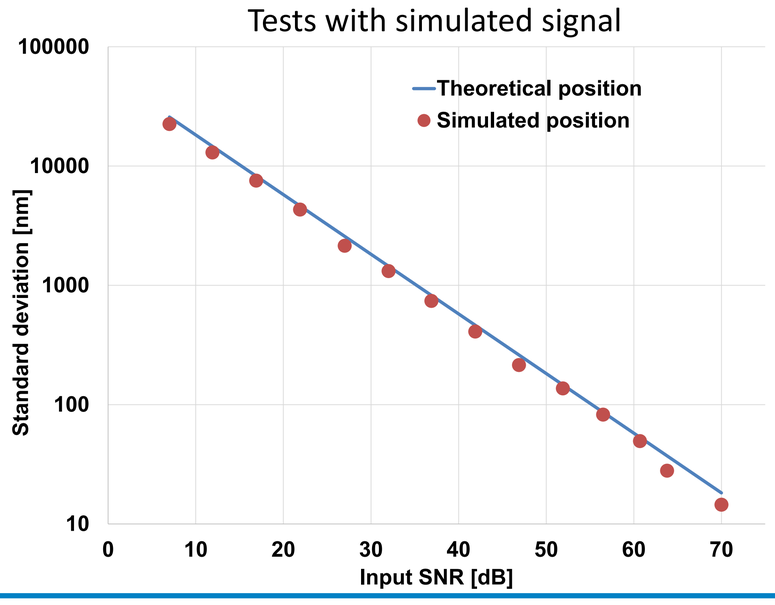
CIC1 filter



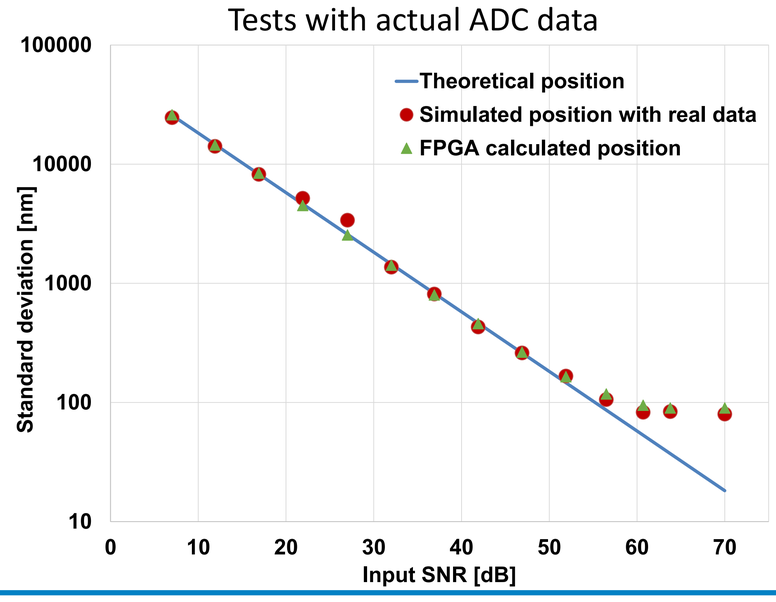
Position



Tests with simulated signal



Tests with actual ADC data



First of all, we decided to check the entire MATLAB chain, generating a sinusoidal signal with an additive white gaussian noise (different realizations of the statistic process for every channel) to emulate a stable and centred beam. Checks on effective and expected SNR are performed at every stage of the simulation, to understand if quantization or processing errors could corrupt it. Varying input SNR, resulting noise on position follows in a good way the theoretical reference, meaning that the entire processing does not limit the resolution up to wanted specifications, at least 200 nm at 10 kHz data rate for Elettra 2.0 for 60 dB of input SNR. Then, as an intermediate step, we moved to real data: a 499.654 MHz signal from a RF generator, splitted in four and fed to ADCs, has been used to emulate a stable beam. Raw data from these latter have been acquired and used in MATLAB simulation. Standard deviation on position saturates at about 90 nm, even if SNR is increased. This means that there is a noise contribution that increases with the signal amplitude and dominates thermal noise after a break even point (located at about 9000 ADC bins, corresponding to -3 dBm at ADC input). ADC full scale is about at +3 dBm, so there is a range of 11 dB where there is no improvement. Since raw data are involved, ADCs are the most likely suspects for causing this: further investigations are ongoing, mainly related to jitter of ADC sample-and-hold stage; the absolute jitter of sampling clock is not involved because, by simultaneously affecting all four amplitudes, can be compensated by the difference-over-sum algorithm, while the observed effect is related to a difference between the channels. Same behaviour is observed moving to full FPGA processing: in that case all the calculations are done inside the unit, logging only the positions, which confirms the correct operation of the overall processing chain.

REFERENCES

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FUTURE WORK

- Include online pilot-tone compensation feature in FPGA
- Code optimization for new SoC platform
- Tests for increasing achievable resolution due to ADCs behaviour