FIRST APPLICATION OF A MULTIPROCESSING SYSTEM-ON-CHIP BPM ELECTRONICS PLATFORM AT SwissFEL

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Abstract

We have developed a new BPM electronics platform based on a MultiProcessing System-on-Chip (MPSoC). This contribution introduces the first application of the platform at the Paul Scherrer Institute (PSI), which is the cavity BPM system for the SwissFEL soft X-ray undulator beamline called "Athos", where a larger number of systems are now operational. Measurement results and differences to the predecessor system will also be presented.

INTRODUCTION AND MOTIVATION

PSI has several particle accelerator facilities, including, the High Power Proton Accelerator (HIPA), the Swiss Light Source (SLS), and SwissFEL, a hard X-ray free electron laser. The RF beam position monitors (BPMs) for the proton and electron beams of these accelerators [1-3] as well as the European X-ray FEL BPMs [4] have electronics - developed mainly by PSI - that were so far based on the VME64x form factor, with analog-to-digital converters (ADCs) using parallel data outputs.

However, for the BPMs of the latest SwissFEL undulator line called "Athos" [5] that generates soft X-rays as well as for future upgrades of SLS and HIPA BPMs, we decided to develop a new platform called "DBPM3". It has a form factor tailored to future PSI BPM systems based on MPSoCs and ADCs with multi-gigabit serial interconnect. MPSoCs integrate several performant CPUs, rich FPGA fabric, various external interfaces and high-speed interconnect on a single chip, enabling the design of more compact and cost efficient BPM systems.

Table 1: PSI Accelerators and RF BPM Systems

PSI Facility	BPM Type	Frequency		FPGA/ASIC Type
		Beam	BPM	
HIPA	Coil	50 MHz	100 MHz	2x Virtex-2 Pro & DDC-ASICs
SLS	Button	500 MHz	500 MHz	DDC-ASICs
Swiss-FEL Linac ...	Cavity (Two Resonators)	2-bunch ΔT=28ns 100 Hz	3.3 GHz	2x Artix-7/ 1x Kintex 7
... Aramis Undulators ...		1-bunch 100 Hz	4.9 GHz	
... Athos Undulators				1x Zynq UltraScale+ MPSoC

In the following sections, we describe the hardware, software and firmware architecture of the DBPM3 platform.

Measurement results and commissioning experience of the first DBPM3 application, the Athos undulator cavity BPM system, are also presented. Besides Athos, we plan to use the DBPM3 platform also for the SLS 2.0 project [6], which is a major upgrade of SLS with a new low-emittance storage ring. Another application will be the upgrade of the 18 years old HIPA BPM electronics. Due to the smaller number of BPMs in Athos compared to SLS 2.0, Athos enabled us to get experience with the platform before producing larger quantities for SLS 2.0, where first beam is expected in 2025.

DBPM3 PLATFORM

Hardware

A DBPM3 unit has a 3 height unit (HE) 19" wide housing. As shown in Figs. 1 to 3, up to six single-width RF front-ends (RFFEs or "daughterboards") can be inserted from the rear side, or three double width RFFEs (for SLS 2.0), or two with triple-width RFFEs (for Athos). The number of BPMs per DBPM3 unit is four for Athos and three for SLS 2.0.The redundant power supply is also inserted from the rear side.
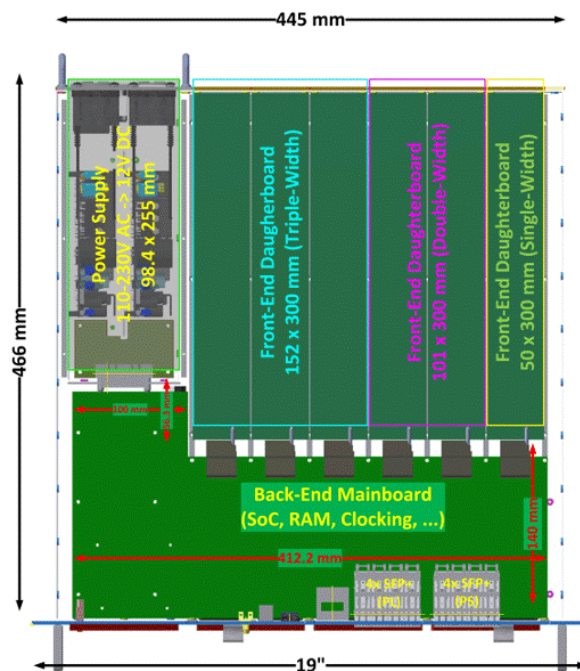

Figure 1: Top view of a DBPM3 unit with cover removed.

The digital back-end mainboard is mounted behind the front panel, having a direct coplanar 120-pin connectors to each daughterboard. The connector is self-centering, and
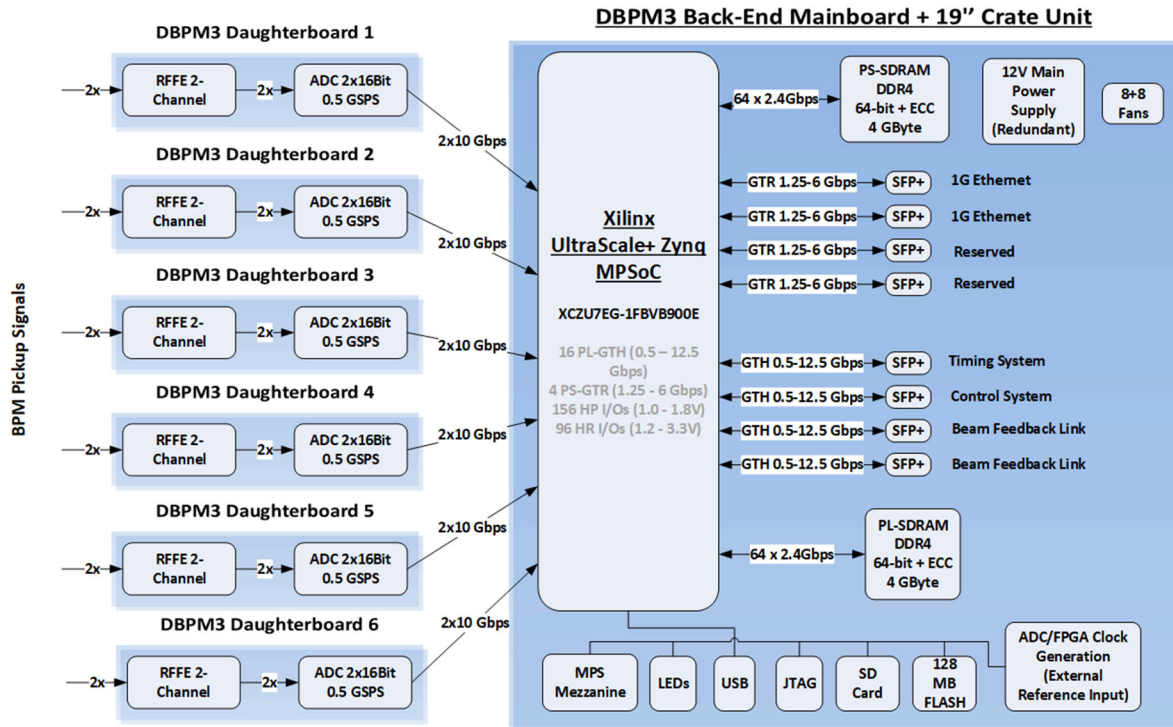
Figure 2: Simplified block schematics the of DBPM3 platform. Up to six front-end electronics modules ("daughterboards") can be plugged into the unit, each connected to the digital back-end mainboard with a 120-pin high-speed connector. The RFFE of the Athos cavity BPMs has two triple-width daughterboards, each serving two BPMs.

supports up to 25 Gbit/s data rate per connector pin pair for differential signals. The back-end has a single MPSoC of type Zynq UltraScale+ ("ZynqU+") from the company Xilinx/AMD. The ZynqU+ integrates on a single chip: A 4-core 64-bit ARM CPU ("APU" = Application Processing Unit), a 2-core 32-bit CPU ("RPU" = Real-time Processing Unit), and an FPGA with programmable logic (PL). Moreover, the MPSoC has various interfaces (Ethernet, I2C, DRAM, multi-gigabit links, USB, SD Card, JTAG, ...), combined with high-bandwidth interconnect structures.

The back-end board has two 64-bit wide DRAMs with 4 GByte size each and 8-bit ECC, 8 SFP+ transceivers at the front panel, and a generic clock synthesis unit supporting external accelerator reference clocks from all PSI accelerators, ranging from 50 to 500 MHz.
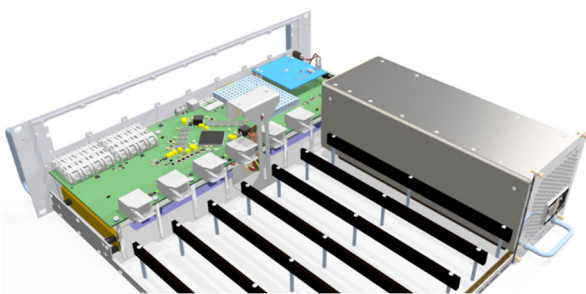

Figure 3: DBPM3 unit, view from rear side with top cover, daughterboards and fan trays removed. The digital back-end mainboard is shown at top left (green PCB). The redundant plugged power supply and guide rails for daughterboards are shown at the right top and bottom side.

In contrast to previous BPM electronics generations based on VME64x, the new Athos DBPM3 electronics has RFFE and ADCs on the same PCB, thus avoiding cable connections between RFFE and ADCs needed for previous systems. The Athos DBPM3 electronics as well as a first SLS 2.0 button BPM electronics prototype both use the same dual-channel ADCs of type ADS54J69 with 16-bits and up to 500 MSamples per second (MS/s). The ADC data is transmitted to the back-end mainboard via the JESD204B standard, using differential multi-gigabit signal lanes working at up to 10 Gbit/s per lane, depending on the adjustable ADC sample rate as well as on the optional on-chip data decimation and filtering supported by the ADC.

Table 2: Comparison of DBPM3 with the Previous MBU Platform

	MBU	DBPM3
ADC Interface	parallel (LVDS)	serial (JESD204B)
RFFE to ADC Connection	differential co-axial cables	PCB traces on common PCB
Integrated Timing Event Receiver	yes	yes
Integrated EPICS IOC	no (but planned)	yes
# Printed Circuit Boards per BPM	3.25	1.33
# FPGAs per BPM	1.75	0.33

Each of the six daughterboard connectors of the DBPM3 back-end supports two multi-gigabit full duplex link pairs, enabling the use of both JESD204 ADCs and DACs on

daughterboards. This makes the DBPM3 platform also suitable for other applications like fast feedbacks. The connector provides clock and synchronisation signals for JESD204B ADCs or local oscillators on the daughterboards, using LMK04828 and LMK01020 clock synthesis chips on the back-end. There are also additional connector signals for fast and slow data, control and synchronization, hot-swap power supply voltages, board serial number and type identification. An EEPROM on the RFFE contains gain and phase calibration tables.

The power supply voltages and currents of back-end and daughterboards are remotely monitored, supporting also remote power cycling. The speed of the fans at the front side of the DBPM3 unit (shown in Fig. 4) can be regulated individually to optimize thermal stability.

Figure 4: DBPM3 front side with two rows of eight fans.

Thanks to new technologies like JESD204B and MPSoC, the hardware complexity, production effort and costs could be significantly reduced compared to previous BPM electronics generations, see Table 2. Due to the smaller number of PCBs and much smaller number of connector pins per BPM and reduced number of cables, we also expect a reduction of the long-term maintenance effort and an even higher MTBF than the present systems.

Cavity BPM RFFE/ADC Hardware

Figure 5 shows the RFFE electronics for the Athos undulator BPMs, with six SMA connectors for BPM input signals. The electronics has symmetric channels for position and charge signals of the cavity BPM pickups, with three dual-channel ADCs close to the mainboard connectors. One ADC is shared by two BPMs, with negligible crosstalk.
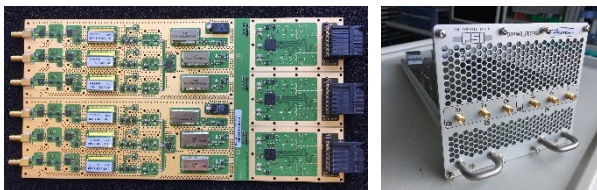

Figure 5: Athos cavity BPM RFFE board for two BPMs. Left: Printed circuit board (PCB). Right: Board with rear panel and metal RF shields mounted on both PCB sides.

The RF input stage of the DBPM3 RFFE for Athos is nearly identical to the previous VME-based electronics platform called MBU (Modular BPM Unit) installed in the SwissFEL linac and hard X-ray undulator line ("Aramis")

[4]. However, the electronics production cost per undulator BPM was reduced about 2.5 times by the new DBPM3 platform (Fig. 6).
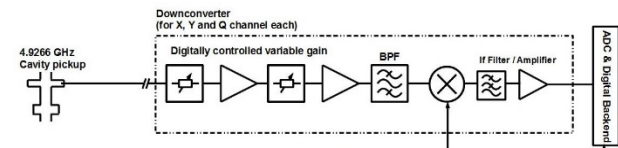

Figure 6: Simplified block diagram of a cavity BPM RFFE input channel. The 4.9266 GHz signal of the two position resonators and the reference resonator of the cavity BPM pickup (loaded quality factor ~1000) are mixed to an intermediate frequency of 134 MHz, digitized, and then mixed digitally to baseband by the PL in the MPSoC.

Software and Firmware

In general, the DPBM3 software and firmware is split into a BPM specific part and a generic part. The latter is used for all DBPM3 applications, including remote management of the DBPM3 unit, health status monitoring, DRAM and ADC interfaces.

The 4-core 64-bit "APU" CPU of the MPSoC is booting Linux at power-up, where the bit stream of the FPGA part of the chip is then loaded in a 2nd step, either from an external SD card, or from an external file server via Ethernet. Loading an EPICS control system IOC on top of EPICS as a 3rd and last step of the booting process enables remote access to various generic and BPM specific settings and measurement data.

The calculation of the beam position from the ADC data is done in FPGA firmware programmed in VHDL, while tasks like automatic range control of the digital step attenuators (DSAs) of the RFFEs are implemented in software on the 2-core 32-bit "RPU" CPU, supporting bare metal C code on one CPU core and FreeRTOS on the other core. The signal processing algorithms for the Athos BPMs are mainly identical to the previous BPM platform "MBU" [4] and will thus not be described again here again. The RFFEs are precalibrated in the lab with an RF generator, and calibration tables are stored in an EEPROM on the RFFE. The tables are used by the MPSoC to digitally correct the attenuation and phase of the channels for each DSA setting, compensating production tolerances of the DSA chips.

The MPSoC also contains a so-called embedded event receiver (EEVR) implemented in firmware that decodes the protocol of the global a timing/event system delivered via fiber optic cables to the DBPM3 units. For SwissFEL, this enables time stamping of the BPM data with a unique global bunch ID directly on the MPSoC, thus making sure the data delivered to the control and archiving system has a correct time stamp and bunch ID.
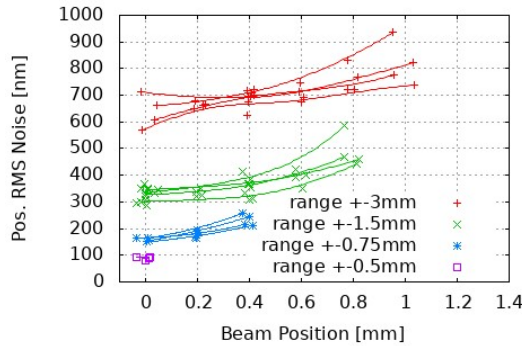
MEASUREMENT RESULTS

Figure 7: Beam position noise of the Athos DBPM3 BPM electronics vs. beam position offset, measured at ~200pC bunch charge with 25 Hz rep rate, for different position measurement ranges.

Figure 7 shows the RMS noise of the DBPM3 electronics as a function of the beam position offset, for different measurement ranges. The maximum limit of the range is defined as the beam position where the ADC reading reaches the ADC full scale, for a given fixed setting of the digital step attenuators (DSAs). The DSAs of the RFFE are used for position and charge range adjustment with 63 dB range. The beam position at three adjacent Athos undulator BPMs was moved simultaneously in steps of 0.2mm for a given range. Athos was operating with single bunches, 200 pC bunch charge and 25 Hz repetition rate. The position noise was calculated from a 10 second data interval, by correlation of the readings of the three BPMs, assuming that all three have the same electronics noise. The calculation also assumes that all orbit perturbations occur upstream or downstream of the three BPMs, but not in between them. Thus, the values are a pessimistic estimate for the upper limit of the BPM electronics noise.
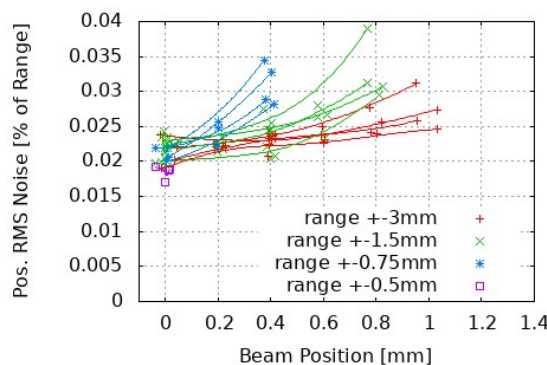

Figure 8: DBPM3 electronics beam position measurement noise in percent of the measurement range.

Figure 8 shows the position noise, normalized to the position range by dividing the absolute noise by 50% of the peak-to-peak range. For small beam position offsets close to 0mm, the dependence of the position on the range is rather small. This shows that the contribution of the thermal noise of the RFFE analog input chain remains smaller than the noise contribution of the ADC during the measurements. The digital step attenuators of the RFFE position cavity signals were varied by 16 dB overall for the ranges shown in the plot.

The inner aperture of the Athos undulator BPM pickups is only 5mm, compared to 8mm for the Aramis hard X-ray undulators of SwissFEL. Therefore the beam offsets during user operation of Athos are usually only reach some 100 µm. Quadrupole magnets and BPMs in the Athos undulators are mounted together on a motorized 2D mover, thus the BPMs and quadrupoles are usually well centered close to the "golden orbit" that provides optimal lasing conditions.

CONCLUSION AND OUTLOOK

A new BPM platform based on RF front-ends with JESD204B ADCs and a digital back-end with a MPSoC has been successfully commissioned at the SwissFEL Athos beamline, being in operation since end 2020. The next DBPM3 application is SLS 2.0, where RFFE prototypes are presently being tested at the SLS. After putting SLS 2.0 in operation in 2025, the next DBPM3 application will be the upgrade of the HIPA proton BPM system, where the present ageing BPM system is operational since 2005 [3]. In addition to BPMs, the DBPM3 unit is also suitable for general beam diagnostics, measurement and feedback systems, where the 3HE unit and large volume available for daughterboards/RFFEs supports also PCBs with larger components, like photomultipliers for beam loss monitors.

ACKNOWLEDGEMENTS

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