ISBN: 978-3-95450-241-7 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2022-MOP32

ANALOG FRONT END FOR MEASURING 1 TO 250 pC BUNCH CHARGE AT CLARA

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Abstract

As part of the development of the CLARA electron accelerator at Daresbury Laboratory, a new analog front end for bunch charge measurement has been developed to provide accurate measurements across a wide range of operating charges with repetition rates of up to 400 Hz. The qualification tests of the front end are presented. These include tests of the online calibration system, compared to a bench Faraday cup test setup; online beam test data with a Faraday cup from 1 to 200 pC; online beam test data with a wall current monitor from 1 to 200 pC, and tests using signal processing such as singular value decomposition. This is demonstrated to enable the measurement of bunch charges in the order of 100 fC using both Faraday Cups and Wall Current Monitors.

INTRODUCTION

The CLARA front-end is the first phase of the CLARA 250 MeV Free Electron Laser (FEL) test facility, based at Daresbury Laboratory. The front-end has been used to provide high energy electrons for experiments during two experimental runs in 2018/19 [1] and 2021/22 [2]. The combined CLARA/VELA facility currently incorporates two Wall Current Monitors (WCMs), four Faraday Cups (FCs) and one Integrated Current Transformer (ICT) for bunch charge diagnostics, and plans for the full CLARA facility, due to be commissioned in 2024, will include further charge devices.

The existing charge diagnostics system installed on the CLARA/VELA FCs and WCMs is based on an *LC* integrator circuit with a resonance frequency of 30 MHz [3]. This system has many problems: It relies on out-of-production components, it requires interpolation after being digitized to accurately measure charge, each front-end requires two multi-core cables run through the radiation shielding and it lacks important features, such as automatic calibration or multiple sensitivity settings to better support low charge operations.

This paper presents results from the final production version of an upgraded front end for charge detection, based on an earlier presented prototype [4]. This final system is substantially improved over both the older *LC* integrator circuit and the previously presented prototype in many ways. First an overview of the front end will be presented briefly, followed by bench tests to verify the system's operation and quantify measurement uncertainty. Finally tests conducted as part of the CLARA 2021/22 experimental run are presented, including online measurement of ultra low charges.

SYSTEM DESIGN

The system design is presented in three sections: The analog signal chain that converts signals from charge devices into an output pulse with an amplitude proportional to charge, the charge injection circuit for onboard calibration of the analog signal chain; and the digital control circuitry to enable operators to adjust the settings of the front end. Figure 1 shows a functional diagram of the circuit.

Analog Signal Chain

The analog signal chain is divided into three sections: Input filter and buffer, charge integration circuitry and output buffer. The input filter consists of a 100 MHz cut-off low-pass filter which enables the front end to be agnostic about the bandwidth of the charge device it is connected to. The bandwidth of an FC is controlled through the impedance it is discharged through, but a WCM can have a bandwidth up to several GHz. The filter is a simple *RC* filter. Following the input filter is an analog switch that select any of three inputs: Charge device input with the input filter, an unfiltered input for front end testing, and the onboard charge injection circuitry. The input is buffered by a unity gain FET op-amp, and is enclosed within an RF shield to limit the effect of external noise sources.

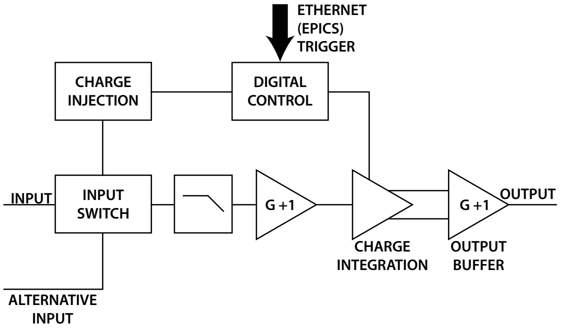

Figure 1: Block diagram of the presented front-end.

The charge integration circuit relies on an ADA4350 Analog Front End integrated circuit [5]. This circuit features a FET input amplifier with six switchable feedback paths, a differential output buffer and control via a serial interface. Five of the feedback paths are used for different integrator sensitivity settings, and the last one to amplify the signal without integration. The values of the components used in the feedback network were selected to ensure that each feedback path has the same frequency response. One goal of the new front end was to enable shot-by-shot measurement of both bunch charge and dark current simultaneously, a

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significant improvement over the previous system, which can only measure one or the other. As the charge integrator only integrates signals that are above the cutoff frequency, the cutoff frequency is selected such that dark current has a bandwidth below this cutoff and bunch charge has a bandwidth above it. Figure 2 shows the frequency response of each feedback setting, normalized by their DC gain for comparison purposes. The sensitivities and their expected range from simulations are listed in Table 1.

Table 1: Front End Sensitivity Settings and Their Design Operating Range

Sensitivity	Capacitance	Operating range
Highest	2 pF	0 – 10 pC
High	15 pF	2 – 20 pC
Medium	51 pF	2 – 40 pC
Low	300 pF	10 – 150 pC
Lowest	1 nF	10 – 250 pC

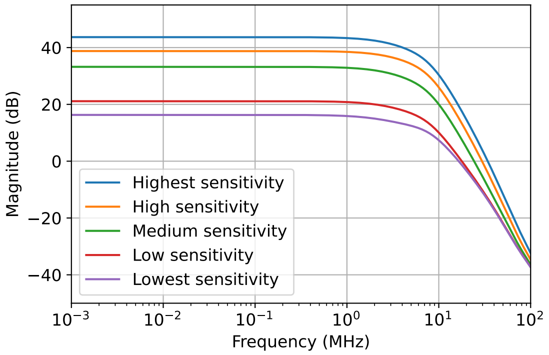

Figure 2: Simulated frequency response of each sensitivity setting. The front end integrates above 10 MHz.

Charge Injection Circuit

The charge injection circuit enables a range of known charges to be injected into the circuit as a calibration signal. The circuit charges a capacitor of a known capacitance C to a known voltage V and, by shorting the charging voltage to ground through an analog switch, discharges the stored charge into the front end's analog signal chain. The stored charge is given by $q = VC$. To provide a wide range of charges for calibration, four high precision voltage references, ranging from 500 mV to 4096 mV, and uses an 8-bit digital potentiometer are used to control the charging voltage. The available calibration charges ranges from 0 – 51 pC in 200 fC steps up to 0 – 418 pC in 1.64 pC steps. An external board with a similar circuit, charged from a higher resolution DAC and powered by a battery was used for the uncertainty quantification. This external calibration circuit has a range of 0 – 255 pC with a resolution of 4 fC.

Digital Control

CLARA uses EPICS as its control system, and the front end is designed to be controlled via Ethernet using EPICS. Ethernet connectivity is provided by a Raspberry Pi Compute Module 4 (CM4), a credit card-sized embedded computer running Linux. During the tests presented in this paper, the CM4 was running a simple server responding to bytes sent via TCP from a soft EPICS IOC, but in the future it is planned that the CM4 will run an IOC itself. The CM4 does not control the board directly, it instead sends commands to a microcontroller which then controls the board. This is mainly due to the deterministic timing available on the microcontroller, which is synchronized to the machine timing system via a trigger, simplifying signal processing. This ensures that settings are only changed outside the sampling window of the ADCs. As the serial interface clocks only run during transmission, this reduces cross-talk between the digital and analog sections. It also ensures that no spurious data during setting changes causes trips due to high instantaneous bunch charge.

RESULTS

Bench Testing

The front end was first bench tested using an external charge injection circuit connected to a calibrated 12-bit resolution oscilloscope. The charge injection circuit's output is discharged into a Faraday cup, which is connected to the front end. The oscilloscope stores the output of the front end, the reference voltage of the charge injection circuit's DAC and the output voltage of the DAC. The sensitivity of each setting was measured at ten points spaced out across the expected range of the setting using the external charge injection circuit. 100 samples were taken at each point. The results are presented in Fig. 3, showing that all sensitivity settings are linear across their operating ranges.

To determine the uncertainty of the bunch charge measurement, 1000 shots were recorded from an external charge injection circuit set to roughly the center of the operating range for each sensitivity setting. The results are shown in Table 2. The uncertainty for each sensitivity is around 1% of the injected charge, which is consistent with the results in Fig. 3.

Table 2: Uncertainty for Each of the Ranges

Sensitivity	Charge	Uncertainty ($\pm 2\sigma$)
Highest	5 pC	101.2 fC
High	10 pC	196.8 fC
Medium	20 pC	379.9 fC
Low	75 pC	1.38 pC
Lowest	150 pC	2.77 pC

Beam Testing

Tests with beam were carried out in three distinct setups. First the front-end was connected to a Faraday cup and

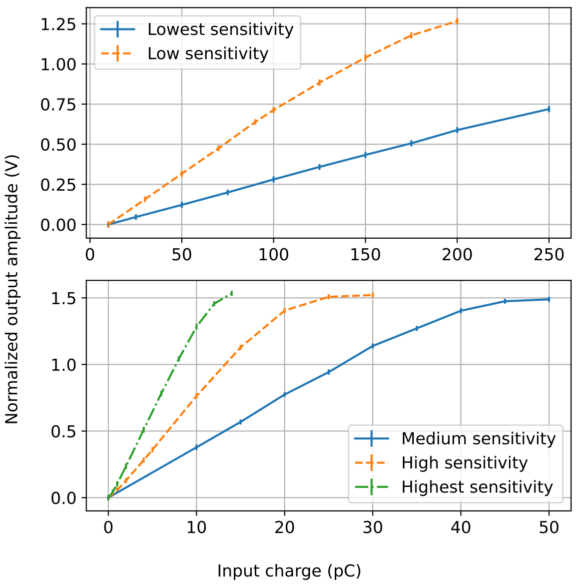

Figure 3: Calibration curves for each sensitivity setting, measured using an external charge injection circuit.

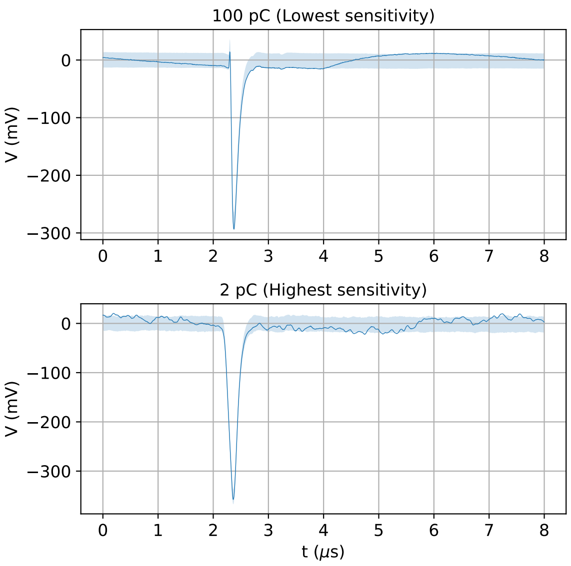

Figure 4: Measured output of the new front end when connected to a Faraday Cup at 100 pC, measured with the lowest sensitivity setting, and 2 pC, measured at the highest sensitivity setting. The shaded areas are ±2σ per sample.

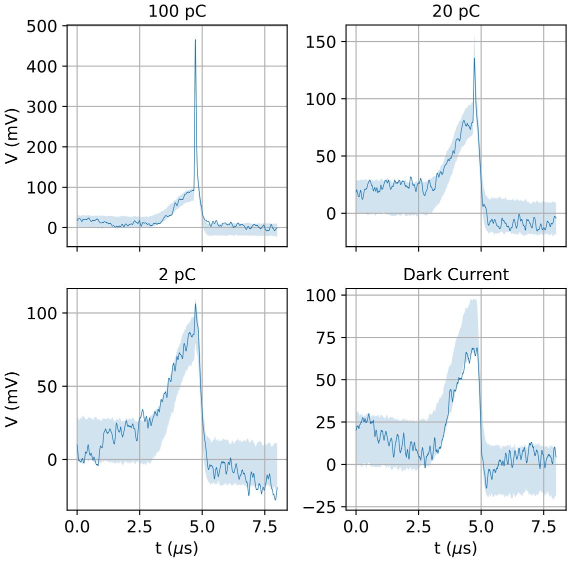

Figure 5: Measured output of the new front end when connected to a WCM at 100 pC, 20 pC and 2 pC, as well as with only dark current. The shaded areas are ±2σ per sample.

tests were run across the normal operating bunch charges of CLARA (2 – 100 pC). To verify the simultaneous measurement of bunch charge and dark current, the front end was then connected to the WCM installed at the exit from the CLARA gun. Finally, as part of one of the user experiments carried out on CLARA in 2022 the front end was used to measure ultra low charges < 500 fC.

Figure 4 shows the measured output of the front end when it is connected to a Faraday Cup. The bunch charge is proportional to the peak value of the output signal. At the highest sensitivity setting a bunch charge of 2 pC can be measured with roughly the same Signal-to-Noise Ratio (SNR) as with 100 pC on the lowest sensitivity setting. Previously the noise floor of CLARA's charge diagnostics was between 1 and 5 pC.

Figure 5 shows the output of the front end when connected to a WCM. These measurements were all taken at the highest sensitivity setting, due to the very low signal developed by the WCM. The signal is of the opposite polarity due to the WCM measuring the image current of the electron beam. The SNR for 100 pC and 20 pC bunch charges is shown to be well within detectable limits. A 2 pC bunch charge gives a much lower SNR, but is still detectable. Figure 6 shows how the bunch charge is determined when there is dark current present. When fully integrated into the control system, adjustable averaging windows for the base and top of the bunch charge pulse will be implemented.

Ultra Low Bunch Charges

While the main intended operating range of the front end is above 2 pC, during the recent CLARA experimental run some users requested very low charges. Using the highest sensitivity setting, an in-air Faraday cup and Singular Value Decomposition (SVD), which has previously been used to remove noise from ICTs [6], charges as low as 150 fC were measured shot-to-shot. This measurement was not done online, and was instead done by buffering 100 shots of data and then performing SVD on that buffer. Figure 7 shows a comparison between the single shot raw data, a simple 100 shot average and a single shot after SVD.

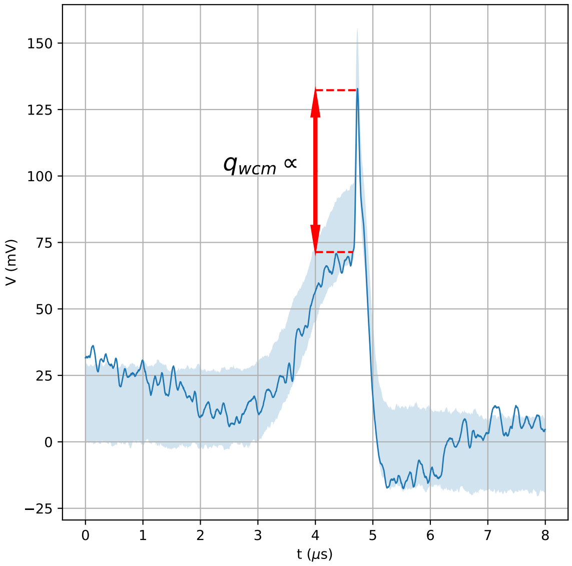

Figure 6: Illustration of how to measure the bunch charge (q_{wcm}) with dark current. The shaded areas are ±2σ per sample.

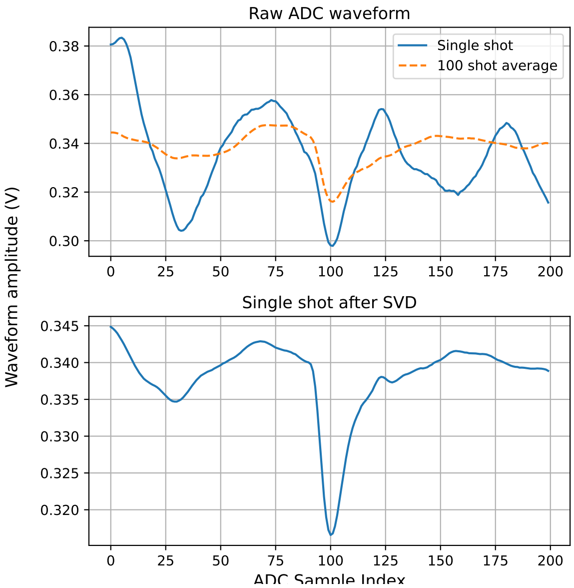

Figure 7: Output of the front end when connected to a Faraday cup exposed to 150 fC, compared to a 100 shot average and a single shot after SVD.

CONCLUSION

A new front end for charge devices, such as WCMs and FCs, has been demonstrated. The front end has multiple sensitivity settings, a charge injection circuit for calibration and is designed to operate across the 2 – 250 pC design specification for CLARA. Bench tests have confirmed that the sensitivity settings have linear outputs in their operating windows and that the uncertainty of the system's measurement is around 1%. Tests with beam have confirmed that the front end works as expected with FCs and WCMs, including simultaneous shot-by-shot dark current and bunch charge measurements. Finally, measurement of Ultra Low Bunch Charges (< 500 fC) using SVD has been demonstrated using offline data post-processing. The front end will be deployed as part of the CLARA Phase 2 upgrade, due to be commissioned in 2024.

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