



Use of RF-SoCs in Accelerator Instrumentation

A High Speed Digitizer (HSD) for the ALS based on the Xilinx ZCU111 demo-board

Eric Norum

International Beam Instrumentation Conference (IBIC)



Xilinx RF-SoC

Multiple generations of devices

ADCs:

- Differential inputs
- Maximum sampling frequencies from 2.5 to 5 GHz
- Resolution of 12 or 14 bits
- Channel counts from 2 to 16.
- Higher speeds use two converters and interleaved sampling
- Optional internal demodulation/downsampling/decimation

DACs:

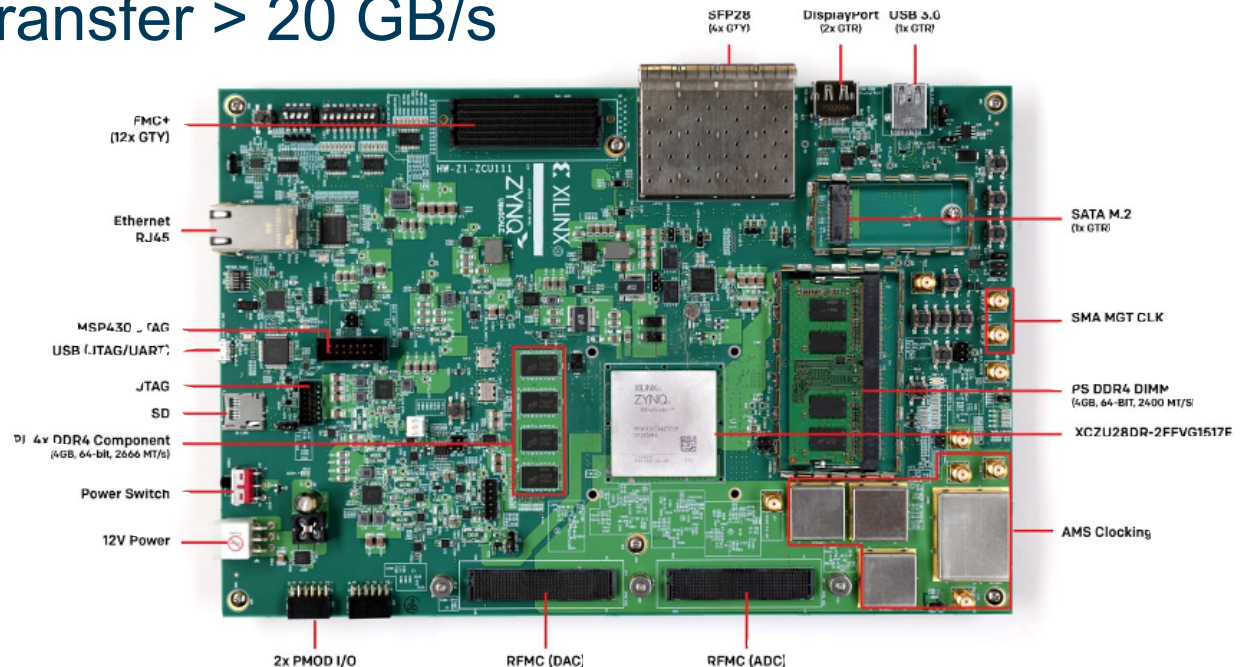
- Update frequencies from 6.554 to 9.85 GHz
- 14 bit resolution

Xilinx RF-SoC – Issues

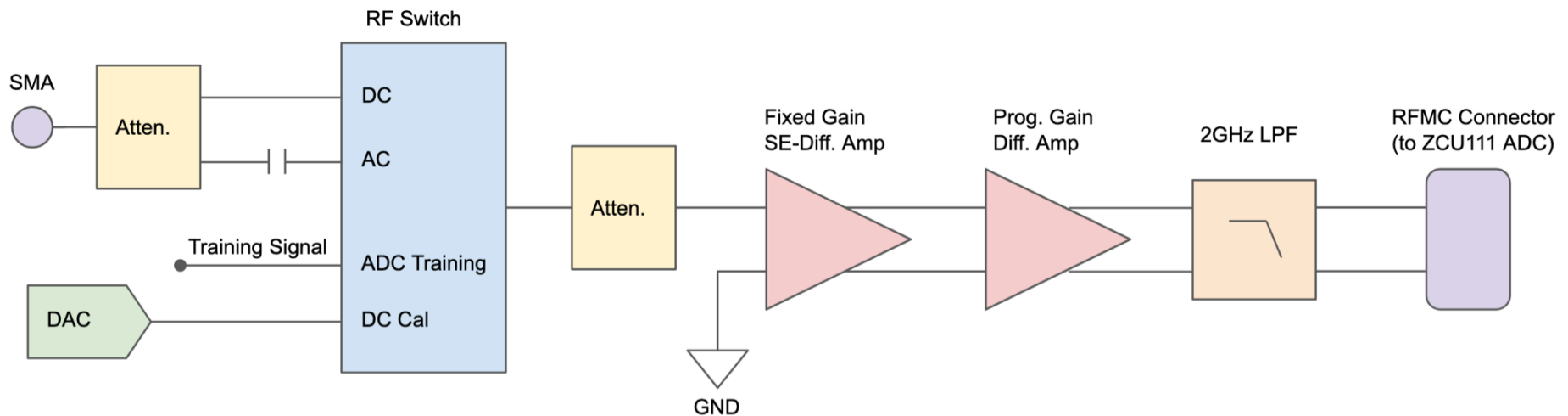
- Complex hardware/firmware/software procedure to obtain synchronized sampling
- Foreground and background ADC calibration
 - Foreground takes place at power-up and requires no signal at ADC inputs
 - Background continues during operation and requires signal with restrictions on power and bandwidth
- High quality reference clock needed
 - E.g. 12 bit converter sampling a 500 MHz signal
 - To have less than 1 count error the sampling clock jitter must be less than 156 fs
 - A 14 bit converter would require a clock with less than 39 fs jitter

HSD – Platform – ZCU111

- Based on first generation device (ZCU28DR)
 - 8 12-bit ADCs
 - 4.096 GHz maximum sampling frequency
 - 8 14-bit DACs, to 6.554 GHz
- 1000 Base-T Ethernet
- 4xSFP28 (up to 25 Gb/s each)
- DDR4 with peak transfer > 20 GB/s
- RF synthesizers

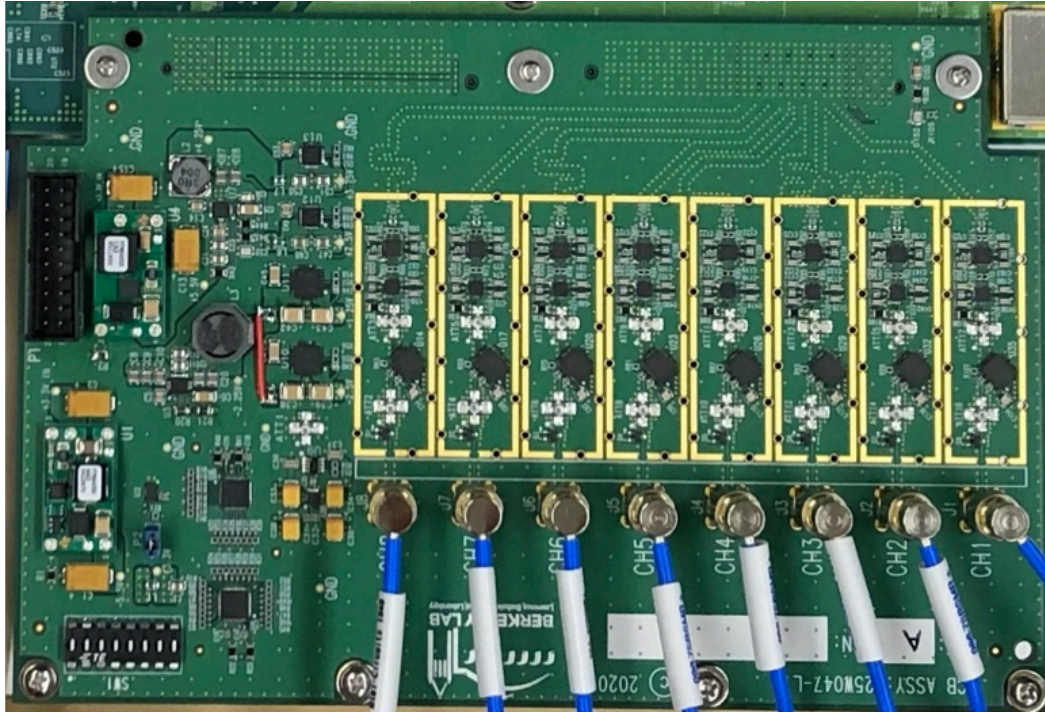


Analog Front End



- MEMS 4PST RF switch
 - DC
 - AC
 - ADC background calibration training signal
 - DC calibration signal
- Programmable gain (-6 dB to +26 dB)
- DC to 7 GHz single-ended to differential amplifier
- DC to 4.5 GHz programmable-gain amplifier

Analog Front End



- 8 independent channels
- Connector matches ZCU111 RF I/O
- Board shown before installation of RF shields

Calibration Procedure

Performed on every change of gain or coupling

1. Set amplifier to desired gain, MUX to calibration DAC
2. Set DAC to 0 V
3. Acquire and average to obtain value A
4. Set DAC to value corresponding to near full-scale ADC reading
5. Acquire and average to obtain value B
6. If new coupling is AC, open all MUX switches then acquire and average to obtain value C
7. Set MUX to training signal
8. Enable converter internal background calibration, then wait.
9. Lock values and disable background calibration
10. Set MUX to DC or AC coupled input signal

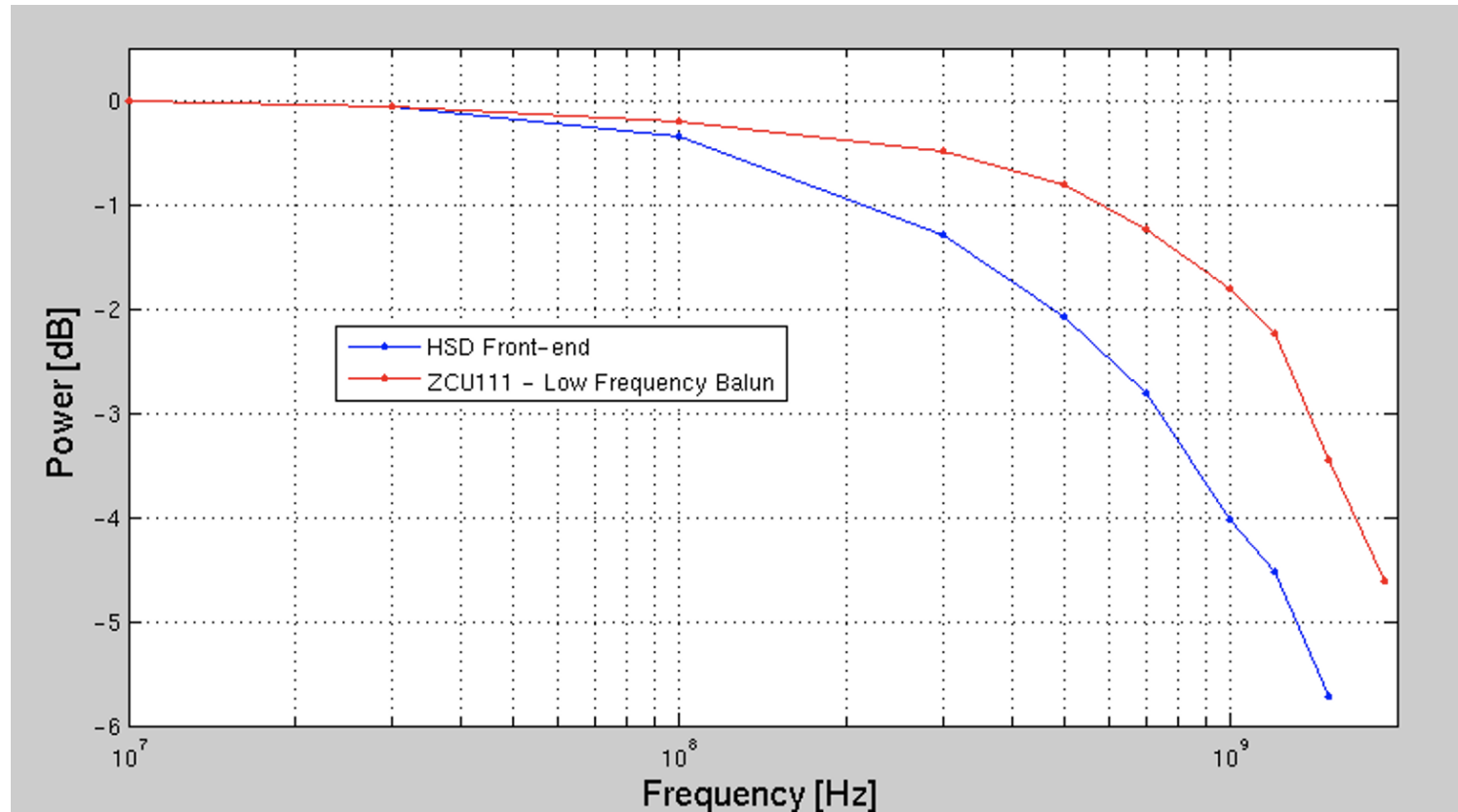
Unit Conversion (ADC counts to Volts)

DC-coupled mode: $V = (V_{\text{cal}} \div (B - A)) \times (\text{ADC} - A)$

AC-coupled mode: $V = (V_{\text{cal}} \div (B - A)) \times (\text{ADC} - C)$

- Amplifier input bias current blocked in AC-coupled mode
- Scaling done in IOC

AFE - Bandwidth

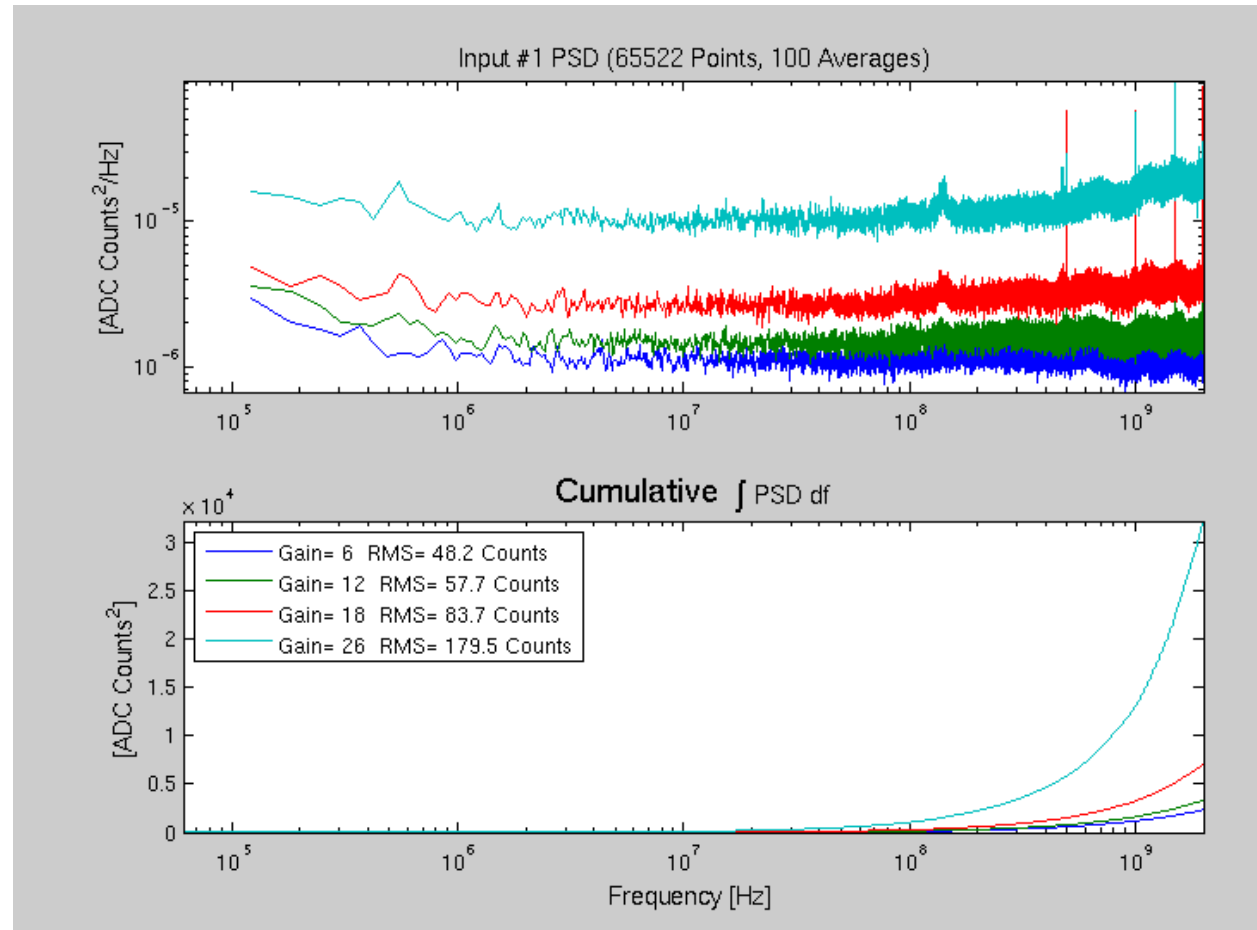


Analog front-end (AFE) components add filtering compared to default ZCU111 with only low frequency balun

Noise Performance

Power spectral density with no input for various AFE gain settings

- Counts are based on 16-bits even though ZCU111 is 12-bit ADC
- So 48.2 counts in the plot is about 3 counts for 12-bit ADC

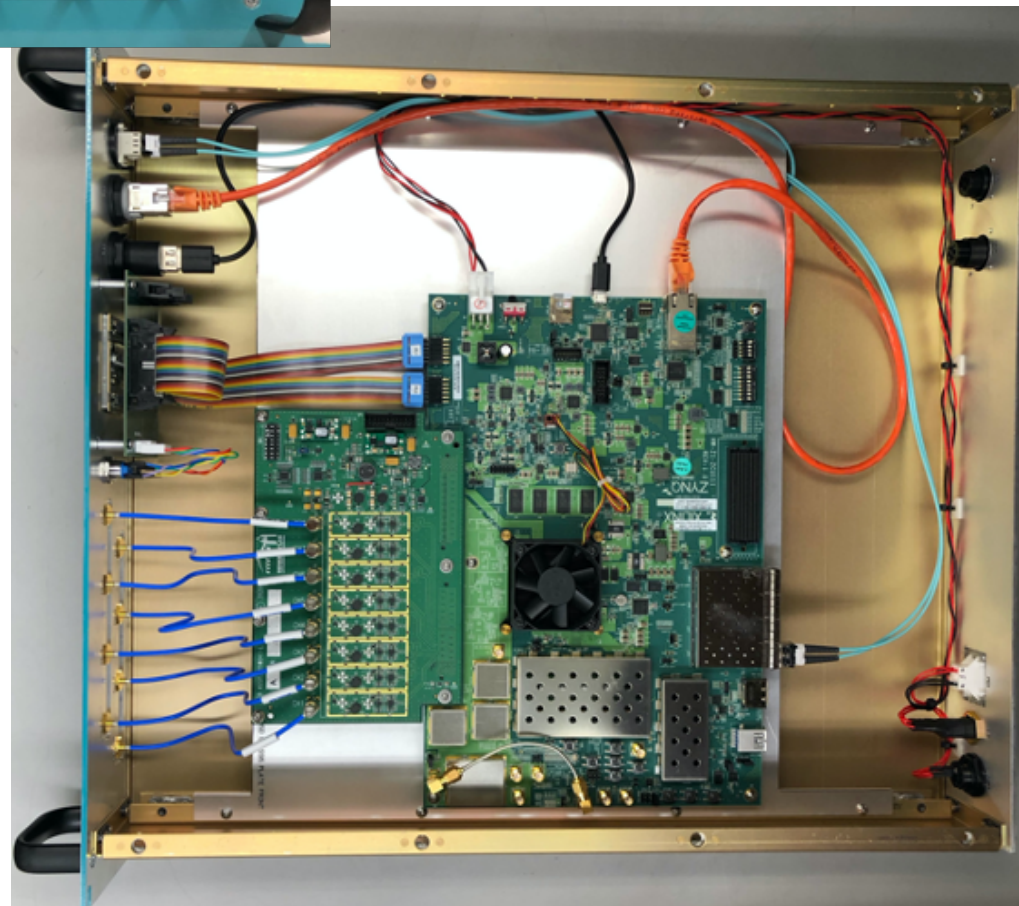


Complete Chassis



Features

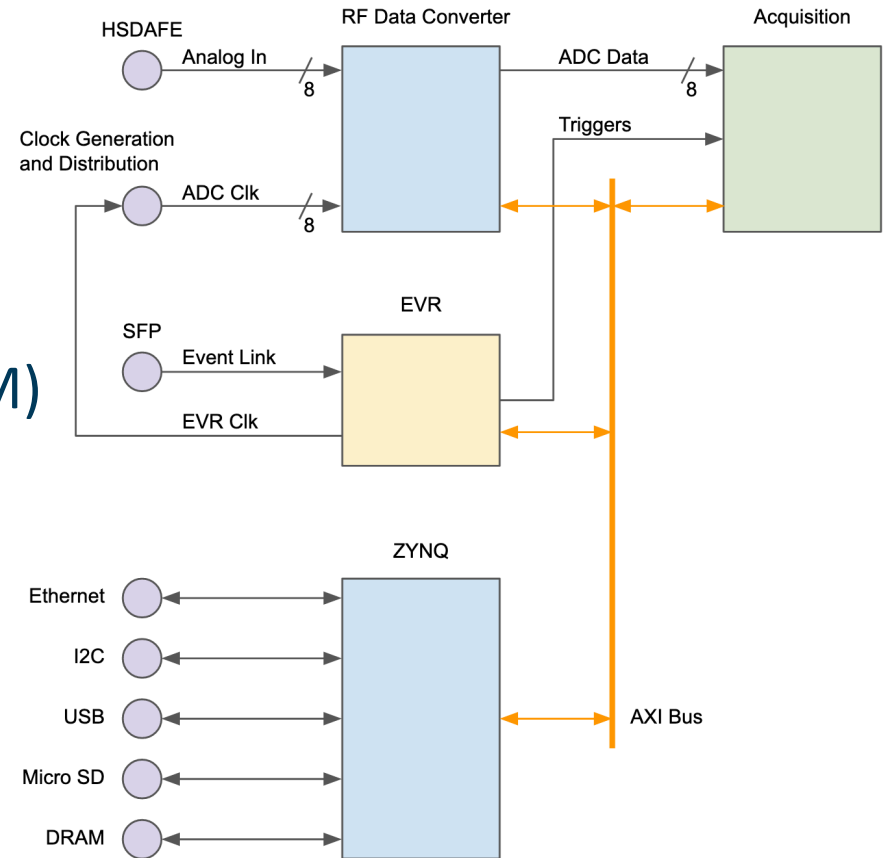
- Front panel display
- Display control button
- Reboot/Recovery button
- 8 SMA connectors
- USB Console/JTAG
- RJ45 1000BaseT ethernet
- Optional rear panel interlock output



Firmware

2 versions of firmware:

- Fast Scope (FS)
- Bunch Current Monitor (BCM)
- Versions are identical except for the sampling frequency and the acquisition logic

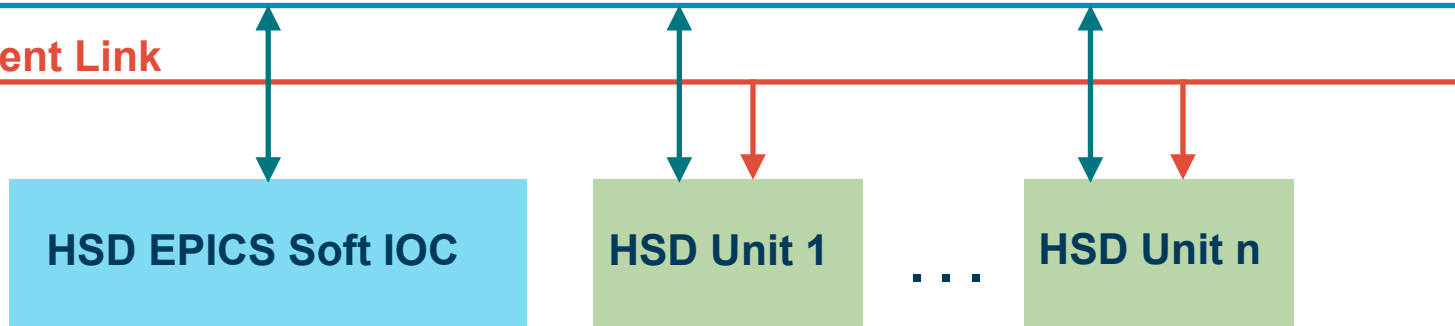


Firmware Version	Sampling Frequency	Acquisition Logic
Fast Scope (FS)	$f_{RF} \times 8$ (~4GHz)	<ul style="list-style-type: none"> - EVR or self-triggered mode - Continuous or segmented acquisition
Bunch Current Monitor (BCM)	$f_{RF} \times 80/11$ (~3.6GHz)	Computes and stores sum at each point over a 'turn', with interleaved sampling similar to sampling oscilloscope

System Architecture and EPICS Integration

Control System Network

Timing Event Link



- Timing Event Link provides synchronization to ALS clocks and triggers
- Ethernet UDP interface to central EPICS soft IOC

SR01:HSD1:

Trigger Mask							Disarm	Arm	
0	0	0	0	0	1	0	Disarm	Arm	1
0	0	0	0	0	1	0	Disarm	Arm	2
0	0	0	0	0	1	0	Disarm	Arm	3
0	0	0	0	0	1	0	Disarm	Arm	4
0	0	0	0	1	0	0	Disarm	Arm	5
0	0	0	0	1	0	0	Disarm	Arm	6
0	0	0	0	1	0	0	Disarm	Arm	7
0	0	0	0	1	0	0	Disarm	Arm	8

Inputs...
 1 Single View Independent
 2 Single View Independent
 3 Single View Independent
 4 Single View
 5 Single View Independent
 6 Single View Independent
 7 Single View Independent
 8 Single View

View 1-4 View 5-8 View All

1 2 3 4 5 6 7 8 More...

Overvoltage! Overrange

Delay From Event To Trigger (~8ns/step)

Trigger Bus	Value
Trigger Bus 2	15625
Trigger Bus 3	25587
Trigger Bus 4	1
Trigger Bus 5	1
Trigger Bus 6	1
Trigger Bus 7	1

Timing System Event

1	0	0	0	0	0	Booster start (10)
0	0	0	0	0	0	Linac modulator scope (12)
0	1	0	0	0	0	BR Injection Kicker (30)
0	0	1	0	0	0	Gun on (36)
0	0	0	1	0	0	BR extraction kicker (48)
0	0	0	0	1	1	SR bump trigger (60)
0	0	0	0	0	0	Post SR Injection (68)
0	0	0	0	0	0	Post SR Injection, continuous (70)
0	0	0	0	0	0	Heartbeat (122)

Fast Scope – Sampling Schemes

- Direct Sampling
 - Single buffer, up to about 131000 points
- Segmented Sampling
 - 2048 short segments (50 points each)
 - 512 long segments (498 points each)
 - Arbitrary spacing between segments

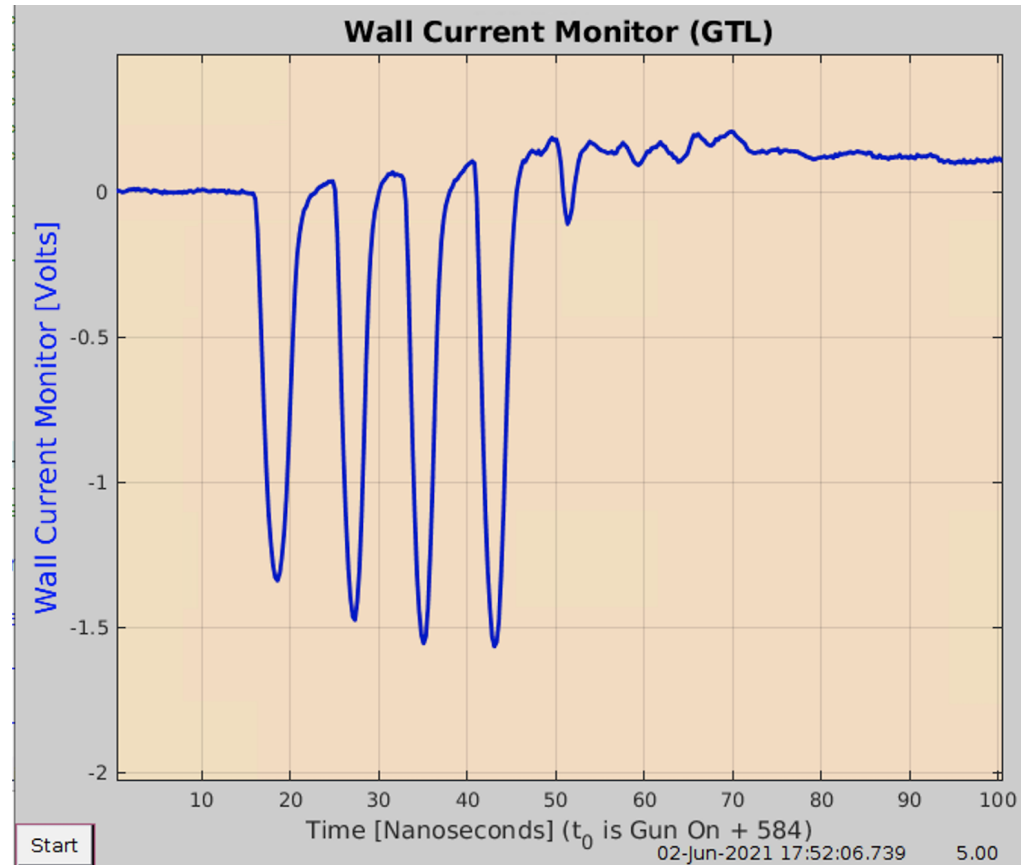
The screenshot displays the control interface for 'LN:HSD1: Input 1'. It features three main control panels, each with a cyan slider and 'save'/'rest' buttons:

- Gain (dB):** Slider from -6 to 5, currently set at 1.
- Trigger Level (V):** Slider from -3 to 10.0000, currently set at 1.0000.
- Pretrigger Samples:** Slider from 1 to 131024, currently set at 1.

Additional controls include an 'ADC Range' section with two input fields (both at 0) and a 'Max' button. A 'Rising' checkbox is also present. Below the sliders, the 'Segment Interval (ADC AXI clocks between leading edges)' is set to 'Contiguous' with 'Early' and 'Late' values of 10. A dropdown menu is open, showing options: 'Contiguous', '256 long segments', and '2048 short segments'.

Fast Scope – Direct Sampling

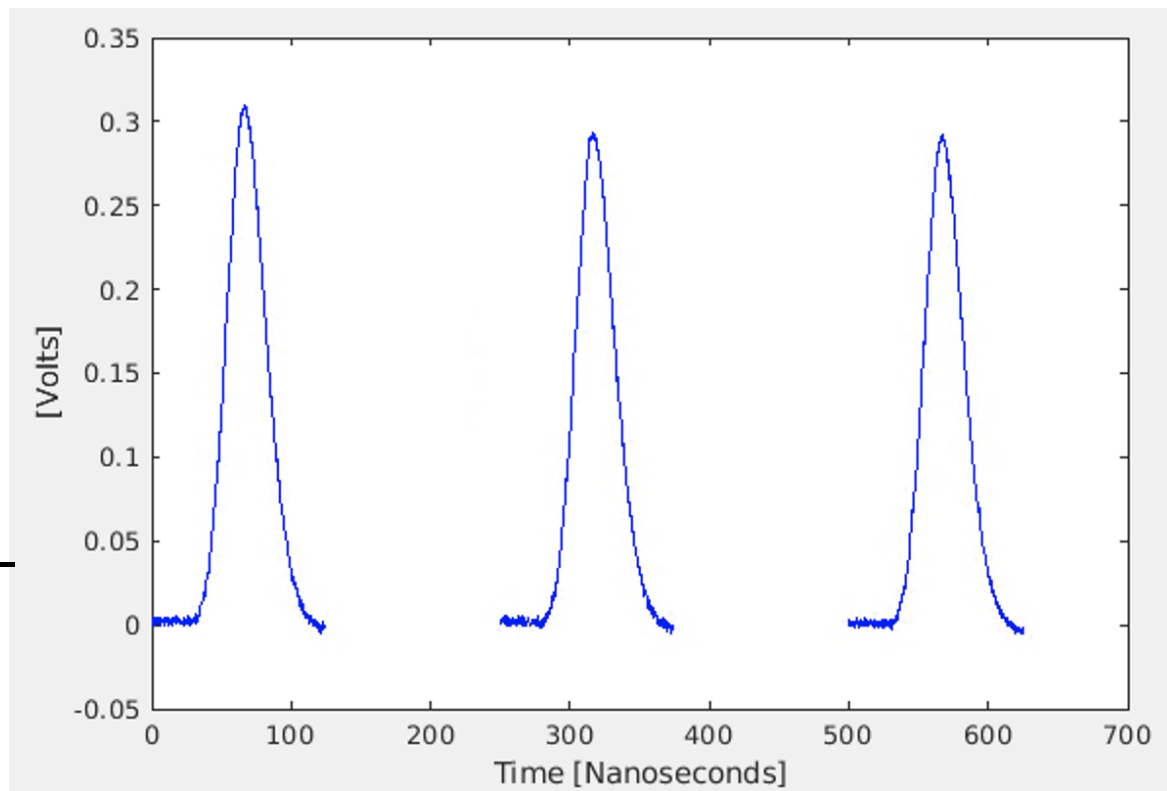
- Direct sampling of wall current monitor signal just downstream of ALS electron gun
- Shows relative charge in each bunch
- The time base is relative to 'gun on' timing system event
- The gun is emitting four bunches at 8 ns spacing.



Segmented Sampling

Beam Charge Monitor Example

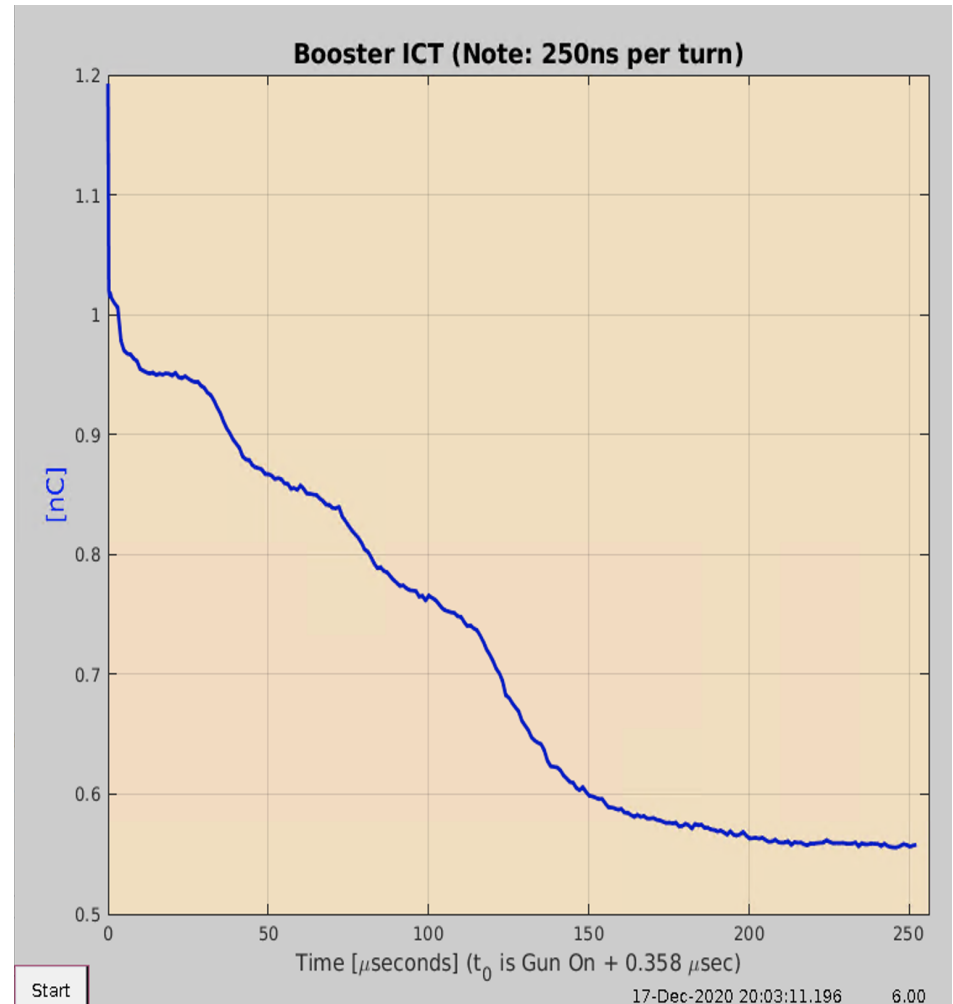
- Allows for saving data only when signal of interest is present
- Adjustable time between segments
- Gap here is set to acquire booster ring turn-by-turn values



Integrating Current Transformer (ICT) Raw Output

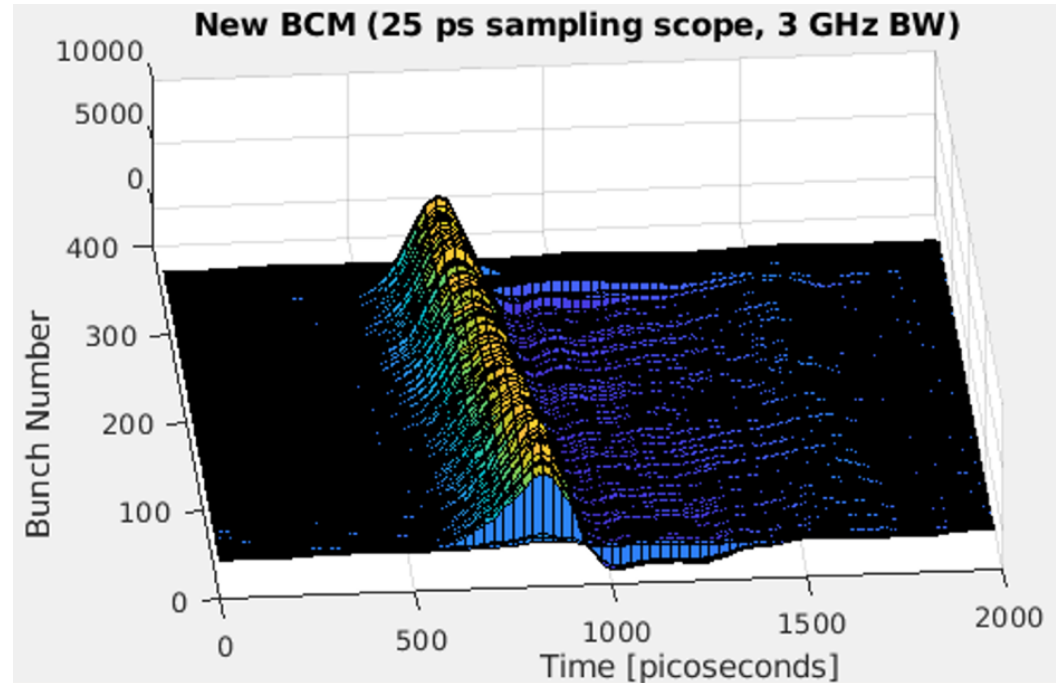
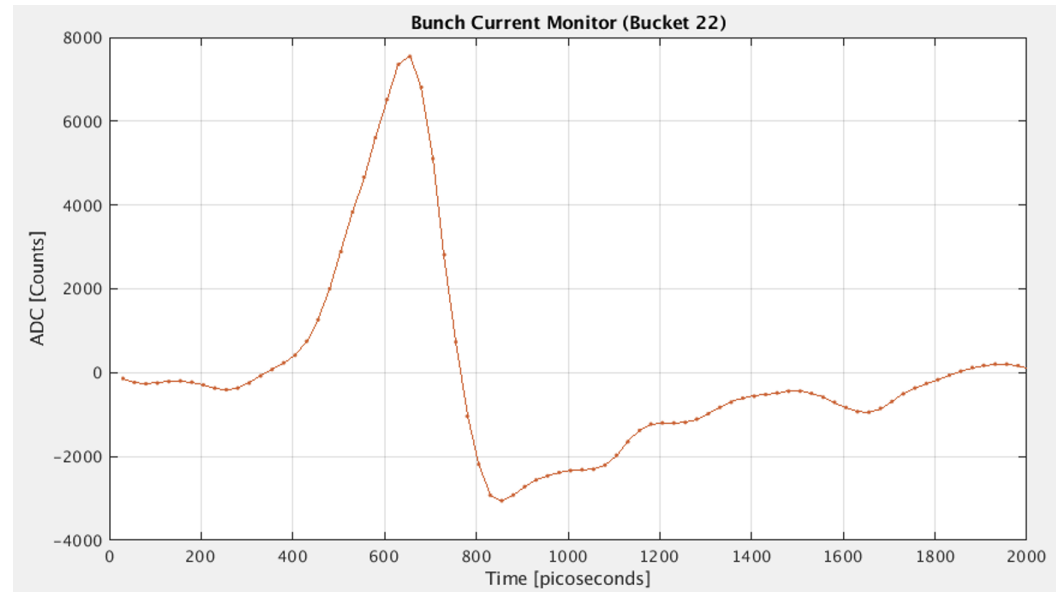
Segmented Sampling - Beam Charge Monitor Example

- Integrate the area under the pulses in the preceding image to obtain charge in booster.
- Gap can differ through the acquisition
- Plot shows turn-by-turn charge for the first 10 turns following injection and then one turn every millisecond for the next quarter second.



Sampling Scope - Bunch Current Monitor

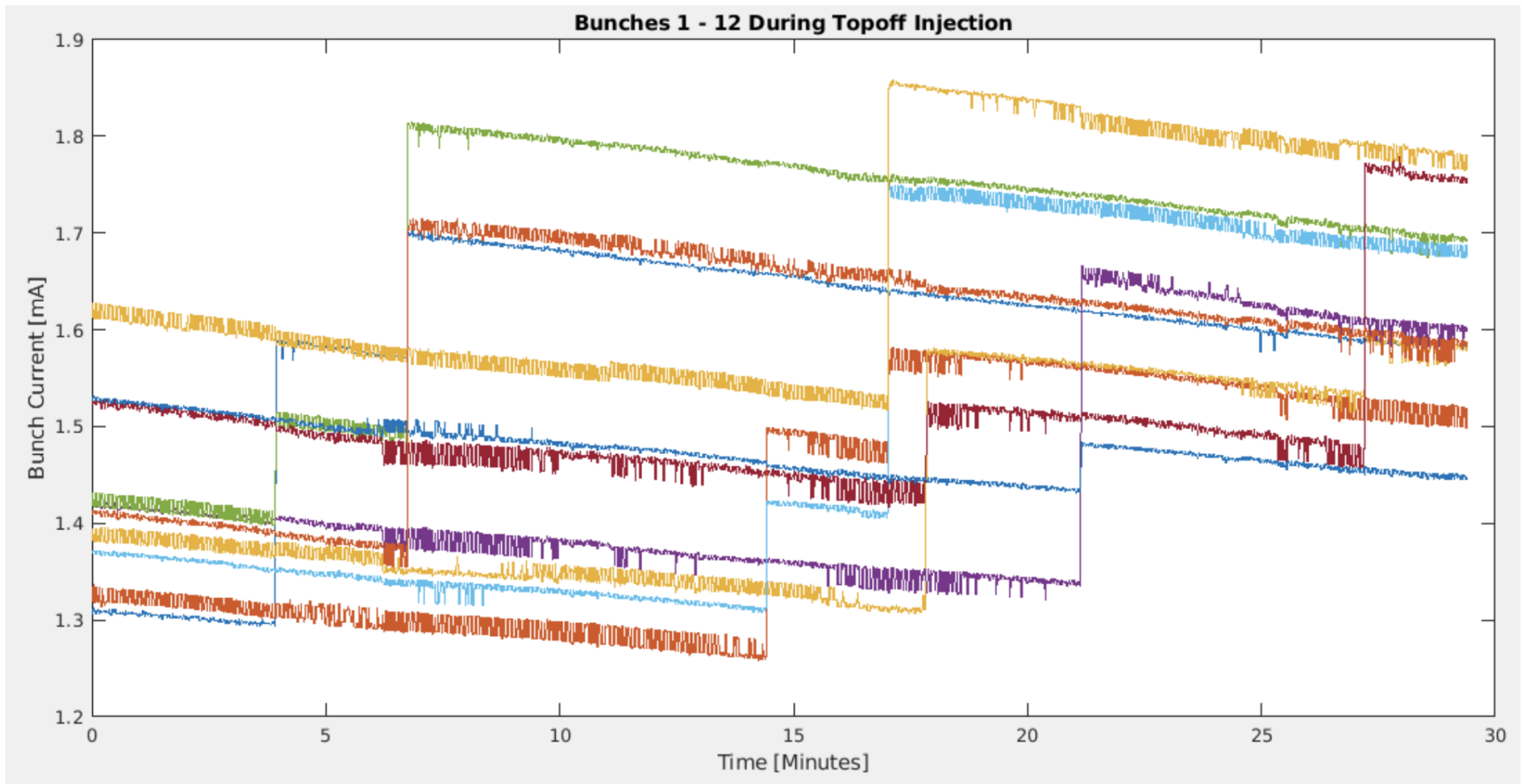
- 3.6 GHz Sample Rate ($F_{RF} * 80/11$)
- Sampling scope mode
- Effective 40 GHz sampling rate
- Connect to button or stripline to measure current in each storage ring bucket



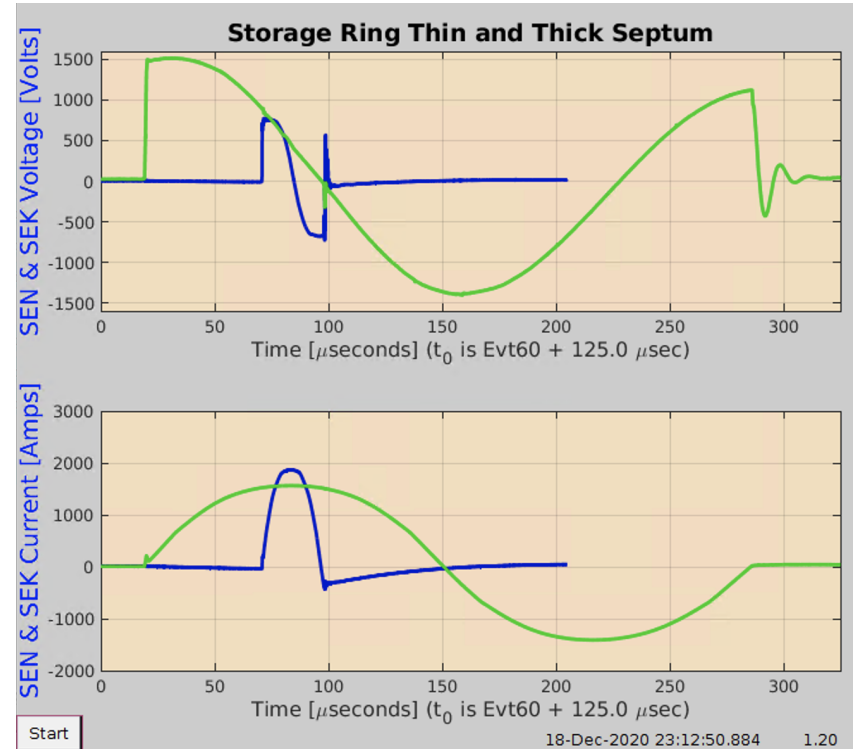
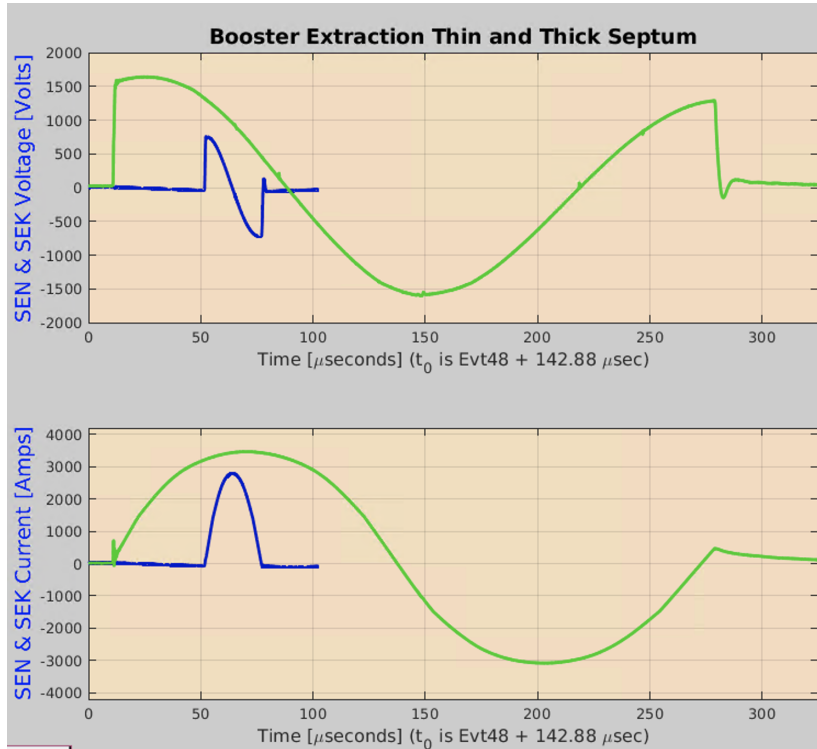
Bunch Current Monitor

Useful for monitoring:

- Fill patterns
- Injection
- Decay rate



Triggering Schemes - Independent or Grouped



- Individually triggered by input channel
- Off any timing system event
- Software triggered
- Multiple channels can be triggered together

Conclusions

- Embedded event receiver allows sampling to be synchronized to the ring RF and provides very flexible triggering
- Meeting timing constraints with full speed raw ADC values is challenging
- ADCs tightly coupled to programmable logic is a great platform for developing instrumentation and control applications
- Nine months of trouble-free operation of six units, more to be commissioned soon

Acknowledgements

- Gregory Portmann
- Jonah Weber
- Jacqueline Bell