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HIGH SPEED PARALLEL DIGITAL SIGNAL PROCESSING STRUCTURE IN BUNCH-BY-BUNCH POSITION MEASUREMENT BASED ON FPGA



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Abstract: In storage ring, the measurement of bunch-by-bunch positions can help to obtain abundant beam dynamics characteristic information, diagnose the instability of beam motion and provide a basis for the suppression of instability. However, the measurement of bunch-by-bunch requires one analog-to-digital converter (ADC) with high sampling rate and one processor with fast digital signal processing (DSP) ability. With the development of electronics, high sampling rate ADCs are no longer a problem. Therefore, high-speed DSP has become the key. In this paper, a parallel digital signal processing architecture based on polyphase decomposition is proposed. This architecture realizes the GHz DSP speed on the programmable gate array (FPGA), which can be used as the infrastructure of high-speed DSP in the bunch-by-bunch position measurement system.

INTRODUCTION

In storage ring, the measurement of bunch-by-bunch positions can help to obtain abundant beam dynamics char acteristic information, diagnose the instability of beam motion and provide a basis for the suppression of instability. However, the measurement of bunch-by-bunch requires one analog-to-digital converter (ADC) with high sampling rate and one processor with fast digital signal processing (DSP)ability. With the development of electronics, high sampling rate ADCs are no longer a problem. Therefore, high-speed DSP has become the key.

In this paper, a parallel digital signal processing architecture based on polyphase decomposition is proposed. This architecture realizes the GHz DSP speed on the programmable gate array (FPGA), which can be used as the infrastructure of high-speed DSP in the bunch-by-bunch position measurement system.

THE BUNCH-BY-BUNCH BPM SYSTEM IN DESIGN

DATA PARALLELIZATION



M-Input Single-Output -- MISO



[2] Gangadharan, S. and S. Churiwala, Constraining Designs for Synthesis and Timing Analysis - A Practical Guide to Synopsys Design Constraints (SDC). 1 ed. 2013: Springer, New York, 226.

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[4] Xilinx, UltraScale Architecture DSP Slice User Guide. 2020.[5] Hawkes, G.C., DSP: Designing for Optimal Results. 2005: Xilinx Advanced Product Division.

[6] P, V., Multirate Systems And Filter Banks. 1993: Prentice Hall. 900.

RESEARCH POSTER PRESENTATION DESIGN © 2019 WWW.PosterPresentations.com processing rate requirement.

At present, the conventional bunch-by-bunch BPM mostly uses simple time-domain algorithms, such as difference-ratio-sum algorithm, interpolation algorithm and look-up table matching algorithm, but there are very few al gorithms in digital frequency domain. The main reason is that the digital frequency domain algorithm is limited by its implementation structure, and it is difficult to realize the frequency domain processing under the condition of high data input rate. The parallel data processing method based on polyphase decomposition breaks through this limitation, can easily deal with the data with GHz input rate, and makes a variety of frequency domain processing methods possible in bunch-by-bunch BPM.