IBIC 2021

MOPP24

Signal processing architecture for the HL-LHC Interaction Region BPMs

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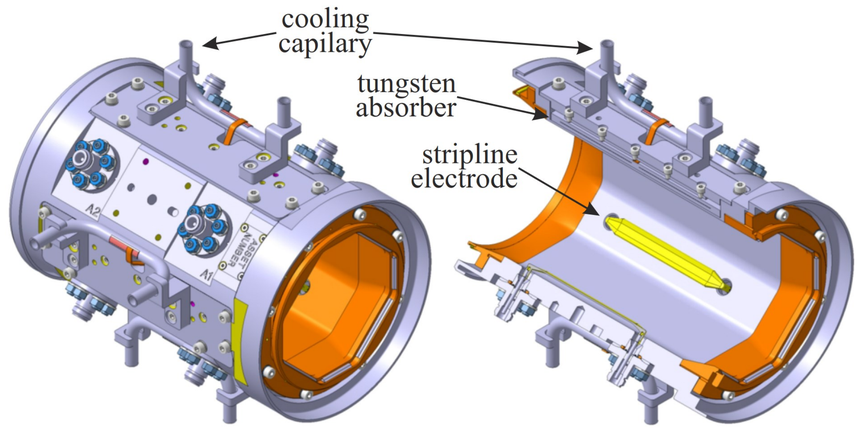
In the HL-LHC era, the Interaction Regions around the ATLAS and CMS experiments will be equipped with 24 new Beam Position Monitors (BPM) measuring both counter-propagating beams in a common vacuum chamber. Numerical simulations proved that, despite using new high-directivity stripline BPMs, the required measurement accuracy cannot be guaranteed without bunch-by-bunch disentanglement of the signals induced by both beams. This contribution presents the proposed signal processing architecture, based on direct digitisation of RF waveforms, which optimises the necessary computing resources without a significant reduction of the measurement accuracy. To minimise the number of operations performed on a bunch-by-bunch basis in the FPGA, some of the processing takes place in the CPU using averaged data.

Introduction

HL-LHC: HIGH LUMINOSITY UPGRADE OF THE LHC
- Goal: deliver **3000 fb^{-1} of integrated luminosity** over twelve years of operation from 2027 [1].
- **New Inner Triplets** (IT) consisting of several high-gradient focusing magnets around ATLAS and CMS experiments will squeeze the proton beams to a **7.1 µm RMS beam size** at the collision point [2].

INTERACTION REGION BEAM POSITION MONITORS
- BPMs of two different types per triplet [3].
- Installed in regions where **both proton beams circulate in a common vacuum chamber**, so must be able to clearly distinguish between the positions of the two counter-propagating particle beams.



Tungsten-shielded cryogenic directional coupler BPM design

STRIPLINES
- Four long electrodes parallel to the beam axis, connectorized on both ends.
- **Directivity**: beam couples predominantly to upstream port with only a relatively small signal generated at the downstream port.
- Longitudinal positions of BPMs optimised to guarantee **temporal separation of beams > 3.9 ns** (≈3x bunch length).
- Except for the BPM closest to the IP, installed with electrodes aligned at **45°/135°** to accommodate **tungsten absorbers** protecting the superconducting magnets from the high-energy collision debris [4].

BRAND NEW ACQUISITION SYSTEM
- Based on **nearly-direct digitization** by an RF System-on-Chip (RFSoC) [5].
- Under development

RFSoC: AN ACQUISITION SYSTEM ON A SINGLE DIE
- Analogue-to-Digital Converters (**ADC**)
- Digital-to-Analogue Converters (**DAC**)
- Programmable Logic (**PL**)
- Several embedded CPUs, referred to as the Processing System (**PS**)

RAW DATA ACQUISITION AND DIGITAL SIGNAL PROCESSING
- 8 BPM ports will be sampled at 5 GSPS by RFSoC 14-bit ADC channels
- The digital electronics and software will use this data to compute beam position
- **Correction algorithm to minimize the parasitic contribution of the other beam** as well as taking into account the BPM rotation, non-linearity and scaling factors.

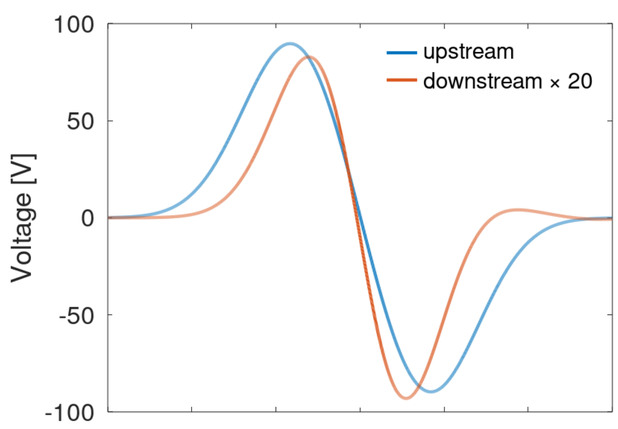
Acquisition electronics: design criteria

BEAM PROPERTIES
- Trains of up to 2808 bunches
- Spaced by multiples of 25 ns
- Intensity in range $5 \times 10^9 - 2.2 \times 10^{11}$

ACQUISITION MODE
- **Trajectory**: on demand bunch-by-bunch, turn-by-turn for a set number of turns
- **Orbit**: continuous multi-bunch, multi-shot with averaging

OPERATIONAL SCENARIOS
- Intensity variation: factor 4 intra-beam, factor 10 inter-beam
- Bunch length: in range $0.5 - 1.2$ ns (4σ)
- Temporal separation: 3.9 ns minimum, 10.5 ns maximum
- Position range: half the BPM aperture of 120 mm

PERFORMANCE GOALS
- **RMS resolution: 15 µm** (trajectory mode)
- **Measurement reproducibility: ±5 µm** (orbit mode, 10 hrs)
- **Max two-beam disentanglement error: ±20 µm** (orbit mode)



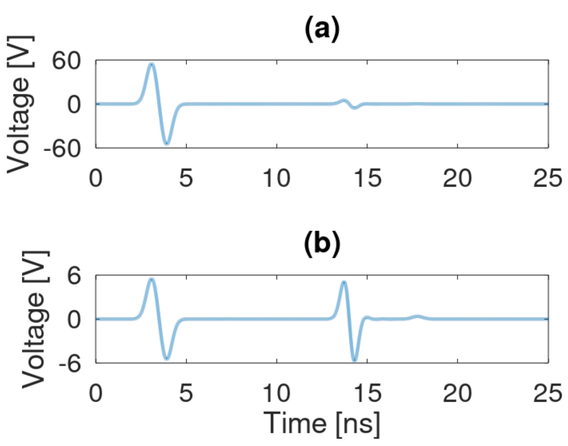
Simulated stripline signals from the CST model of the HL-LHC IT BPMs.

The beam has a Gaussian bunch profile (width $\sigma = 0.3$ ns) and an intensity of 2.3×10^{11} and travels along the BPM axis.

The beam arrives first at the upstream end of the BPM. The downstream signal has been amplified by a factor 20.

Overview of signal processing

DESCRIPTION OF THE INPUT SIGNALS
A CST Microwave Studio model of the BPM was used to calculate the signals generated by the passage of a single bunch of charged particles. **At each port, both beams produce signal**. Each beam "couples" to the set of ports at the entrance end of the BPM; for a given port, the coupled beam is also known as the "main beam", and the other beam as the "counter beam". Each port signal thus consists of two sub-signals: **a coupled signal from the main beam and an isolated signal from the counter beam.**



Expected signal on a specific port. For this port, the main beam arrives first; the plot thus shows a coupled signal from the main beam followed by an "isolated" signal from the counter beam.

The main beam intensity is reduced by a factor 10 in (b) compared to (a). The intensity imbalance, combined with a large position offset of the two beams, results in a **counter beam signal that is comparable to that of the main beam.**

FULL SIGNAL PROCESSING CHAIN
- **Calculate the sum** of squares for each waveform vector
- **Scale the sum** to account for: variable attenuation, measured signal gain imbalance
- **Power compensation**
- **Position calculation** using the Δ/Σ method
- **Polynomial correction** to account for non-linearity and BPM rotation.

EXPECTED PERFORMANCE
Simulation results suggest meeting the performance goals will be **challenging**:
- **RMS resolution:** 10-15 µm; in line with the requirement, but real life performance unlikely to meet that of the simulation.
- **Measurement reproducibility:** to achieve the target, uncorrected imbalance in signal gain between a pair of ports must not exceed 0.01%.
- **Maximum two-beam disentanglement error**: 20 µm comfortably achieved using the power compensation procedure.

BEAM DISENTANGLEMENT ALGORITHM
The **power compensation method** subtracts the power of the counter beam from the total power measured on each port in order to recover the main beam power. A full derivation of the algorithm is available in [6]; here, we note the beam disentanglement algorithm amounts to **solving a quadratic equation for each port** to give the value of κ, the amplitude of the main beam signal in each case.

$$\kappa_1^2 + \left(2\frac{\chi}{\psi_c}\sqrt{\frac{\psi_2}{\psi_c}}\right)\kappa_1 + \left(\frac{\psi_i}{\psi_c}\frac{\psi_2}{\psi_c} - \frac{\psi_1}{\psi_c}\right) = 0 \quad \text{where} \quad \psi_1 = \sum_{n=1}^{N} V_1[n]^2$$

$V_1[n]$ represents the sequence of samples observed on port 1

ψ_c, ψ_i and χ also represent the sums of sequences of samples, but they are calculated from **predictions of the signals** induced by the passage of a **reference beam**. ψ_c and ψ_i correspond to the predicted coupled and isolated signals multiplied by themselves; χ corresponds to the cross-term.

System architecture

Available resources	Position calculation in RFSoC	Position calculation in SW
ADCs (8)	100%	100%
Block RAM (38 Mb)	3%	4%
PL DSP (4,272)	6%	5%
PL LUT (4,255,280)	3%	2%
PL FF (850,560)	3%	2%
DDR (32 Gb)	3%	6%
DDR BW (95 Gbps)	10%	18%
Read-out BW (500 Mbps)	3%	6%
Max trajectory rate	1.25 s^{-1}	0.55 s^{-1}

ESTIMATED RESOURCES
- When **computing the beam position** solely in the RFSoC versus partly in SW running remotely
- Available resources on a **Generation-3 RFSoC**.
- PL use accounts only for algorithm, not full acquisition system.
- Available DDR bandwidth (BW) estimated at ~70% of declared peak performance in datasheet [5].

DISTRIBUTION OF PROCESSING
The resources will be used as follows:
- **PL** - fast signal processing.
- **Block RAM** - store raw data for calibration, debugging, implementing filters.
- **DDR** - store high-volume data of trajectory mode.
- **PS** - control acquisition, implement calibration, connect to the remote computer.
- Delegating beam position calculation to SW saves PL resources but doubles bandwidth, required memory.

DATA READ-OUT
- **Orbit mode data**: streamed out continuously at a slow rate (10s of Hz)
- **Trajectory mode data**: sent out on demand

Summary

The analysis indicates that **an RFSoC could meet the basic performance goals**. The distribution of required processing between RFSoC and SW will be decided based on the experience gained with **a proof-of-principle system foreseen for 2022**.

References

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