TESTS OF DIGITAL BPM SIGNAL PROCESSORS FOR SHINE*

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Abstract

Digital signal processors that can handle 1 MHz bunch rate BPM signal processing is under development for SHINE. At the same time, two general purpose processor prototypes for all BPM signal sampling and processing have been developed. One uses 14bits ADC, the other uses 16bits ADC. Both processors have been completed. This paper will introduce the tests of the processors and the related performance evaluations.

INTRODUCTION

Shanghai HIgh repetitioN rate XFEL and Extreme light facility (SHINE) is a 3 km long hard X-ray FEL facility built underground in Shanghai. The designed beam repetition rate is 1 MHz. The project was initiated at the end of 2018. Now the research of key technologies has entered the final stage. There will be three types of BPMs located in different parts of the machine, including stripline BPM, cold button BPMs, and cavity BPM. The required BPM system resolution is 10 μm, 50 μm and 200 nm at 100 pC respectively.

BPM electronics will use independent RF front-end modules and digital signal processors. Different RF front-end modules will be designed to meet the signal characteristics requirements of different BPM types. The design of the RF front-end modules will not be introduced here. All three types of BPM will use unified digital signal processor hardware. The processor will be used for signal processing of different BPMs through the development of corresponding FPGA firmware and software [1]. The processor mainly contains 4 channels ADCs for sampling, FPGA for signal processing and ARM for system control and communication. Considering the beam dynamic range and the required system performance, the relative resolution of the processor should be better than 0.1%.

The processor is designed as a 1U height standalone instrument. The processor consists of a FPGA carrier board and an ADC daughter board. The boards are connected through FMC connector. The sampled data from ADCs are transmitted to FPGA through the JESD204B protocol. Another FMC connector is reserved for a WRN timing board. Figure 1 is the structure of the processor. Other interfaces including a Ethernet port, serial port, JTAG, SD slot, et al. Table 1 lists the specification of the processor. Except for the generic BPM processor, another direct RF sampling processor for cavity BPM also has being developed, the

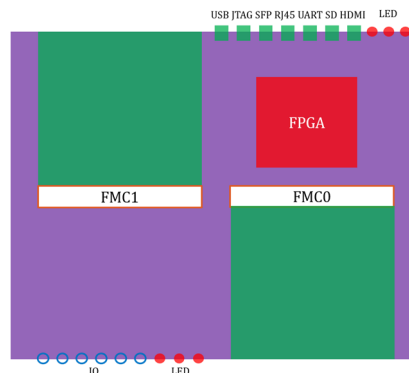hardware is completed but firmware is still in progress, it will not be introduced here.

Figure 1: Processor structure.

Table 1: DBPM Specifications

Parameter	Value
Channels	4
Bandwidth	≥ 1 GHz
ADC bits	≥ 14
Max ADC rate	≥ 500 MSPS
FPGA	Xilinx Zynq Ultra+MPSoC
Clock	External
Trigger	Ext./Self/Period
SFP	≥ 2
Interlock	Lemo
DDR	≥ 512 MB
Software	Arm-Linux/EPICS
Relative resolution	≤ 0.100%

In order to cultivate qualified vendors for SHINE, two processor prototypes were developed at the same time. One processor uses 14 bits ADCs, the other two uses 16 bits ADCs. The maximum sampling rate of all ADCs is 1 GSPS. The development of the processors has been introduced in previous conference paper [2]. Recently, all the two processor prototypes come to the final stage. The tests of the processors will be introduced here.

TESTS OF PROCESSOR A

Processor A uses 14bits ADCs and Xilinx FPGA XCZU9EG. 8V19N490 is used to provide low jitter clock for ADCs and the system. Figure 2 is the PCB of the ADC card and FPGA card. The ADC card is designed according to FMC standard.

Figure 2: Processor A.

The processor has been tested in lab with a vector RF signal generator. A 29.75 MHz RF signal was divided into 4 channels and fed into the processor. At the same time, a 119 MHz signal from the generator was used as synchronized external clock of the processor. The clock was multiplied to 595 MHz with PLL 8V19N490, and then used as ADC sampling clock. Figure 3 is the spectrum of sampled data. The 2nd, 3rd and 4th harmonics were higher than -60dB. The relative position was calculated with Δ/Σ algorithm like orthogonal stripline BPM. The calculated relative position resolution is $3.47e^{-5}$. Beam tests have not yet been done.
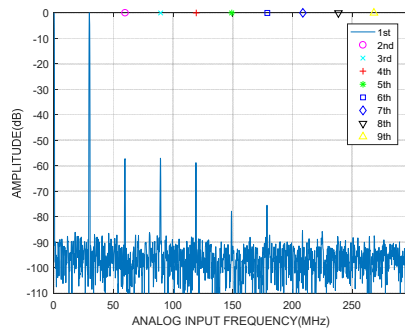

Figure 3: Spectrum of processor A sampled data.

TESTS OF PROCESSOR B

Processor B using 16 bits ADCs and Xilinx FPGA XCZU9EG. LMK04832 is used to provide low jitter clock for ADC and the system. Figure 4 is the PCB of the processor. The ADC board is wider than the FMC standard. Lab test conditions were the same as the processor A test, but the sampling clock was multiplied to 833 MHz.

Figure 4: Processor B.

Lab Test

Figure 5 is the spectrum of sampled data. The 2nd harmonic was lower than -60dB, and 3rd harmonic were lower than -70dB. The relative position resolution is $1.74e^{-5}$. The performance of processor B shows better than processor A.
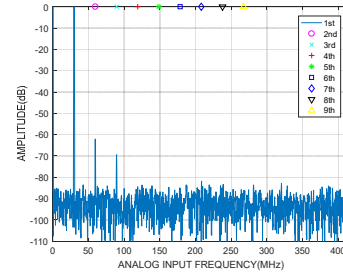

Figure 5: Spectrum of processor B sampled data.

Beam Tests on SXFEL

The processor has been used to sample the signal from stripline BPM and cavity pickup on SXFEL. Figure 6 is the block diagram of the test on stripline BPM. The output signals of pickup B and D were filtered with 20 MHz band pass filters firstly, then adjusted to proper range with amplifiers and attenuators, and then divided and fed into processor. 119 MHz signal from timing system is used as synchronized external clock.
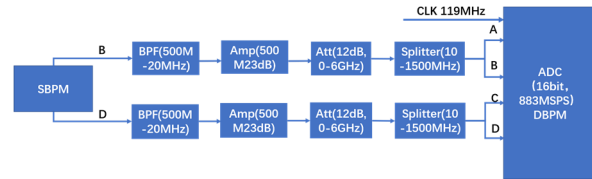

Figure 6: Block diagram of stripline BPM test.

Two unified positions can be obtained from the test. Figure 7 shows the relative position resolution is $1.80e^{-4}$.
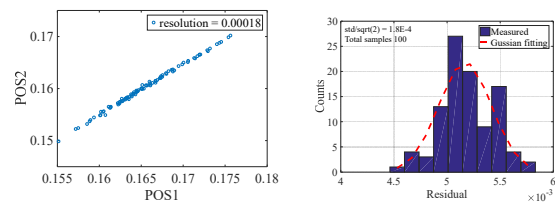

Figure 7: Relative position resolution of test with stripline BPM.

During the test, there was no available cavity BPM nearby. Fortunately, two cavity pickups IN_BAM01 and LA_BAM01 for beam arrival time measurement (BAM) can be used. The output signals of the two cavities were treated as the signals from position cavity and reference cavity of a BPM. Figure 8 is the block diagram of the test. The output signal from the cavities were down converted to 34 MHz IF signal with front-end module, and then attenuated and divided to feed into the processor.
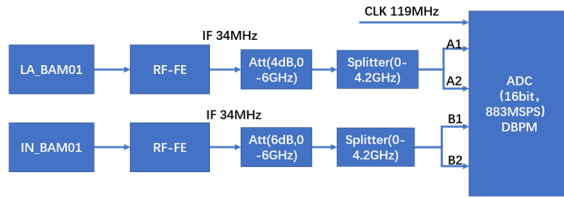
WEPP32

Figure 8: Block diagram of cavity BPM test.

The relative position resolution is $1.24e^{-4}$ as in Figure 9 (left). The beam flight time (BFT) between IN_BAM01 and LA_BAM01 also can be obtained from the same data. The relative BFT resolution is 3.9 fs shown in Figure 9 (right).
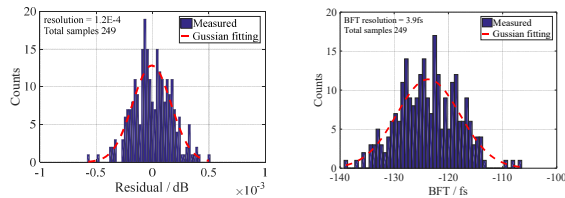

Figure 9: Relative resolution of measured position (left) and BFT (right).

SUMMARY

Two general processor prototypes for stripline BPM, cold button BPM and cavity BPM have been developed for SHINE. The ADCs are 14bits and 16bits respectively. The lab tests with RF signal generator shown the performance of processor B is better than processor A. The beam tests on SXFEL show that the relative position resolution of processor B is better than $1.80e^{-4}$, which is far better than the 0.1% requirement of the BPM system.

Next we will focus on developing firmware and software to make the processor a fully functional equipment for SHINE.

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