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Batch Applications of Digital BPM Processors from the SINAP*

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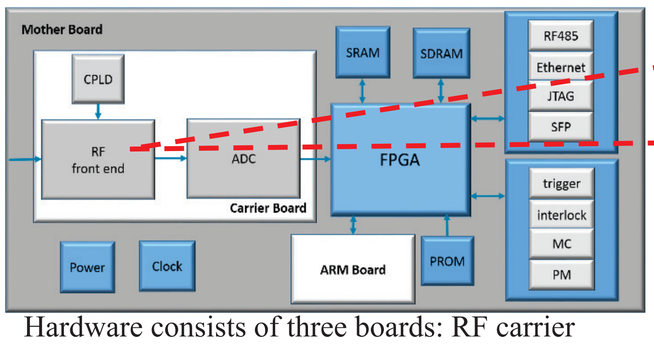
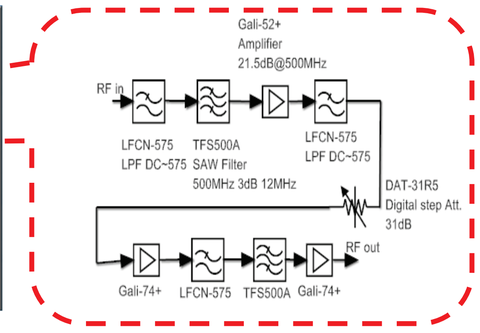
Introduction

A prototype of the DBPM has been developed successfully at the SINAP during the past few years. Some tests and applications have been carried out at the Shanghai Synchrotron Radiation Facility (SSRF). Since 2015, two FEL facilities, DCLS and SXFEL, have been under constructions. Dozens of stripline BPMs and cavity BPMs are planted along the LINAC accelerators and the undulators. To handle the BPM data acquisitions and the position calculations, a new in-house BPM processor has been designed.

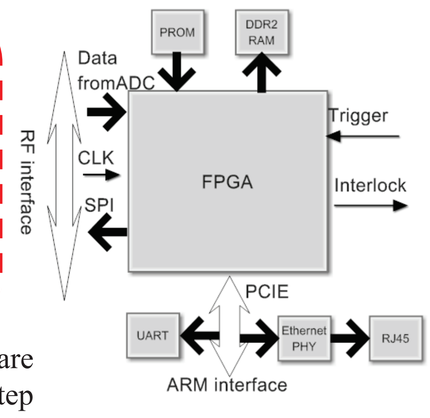
Hardware



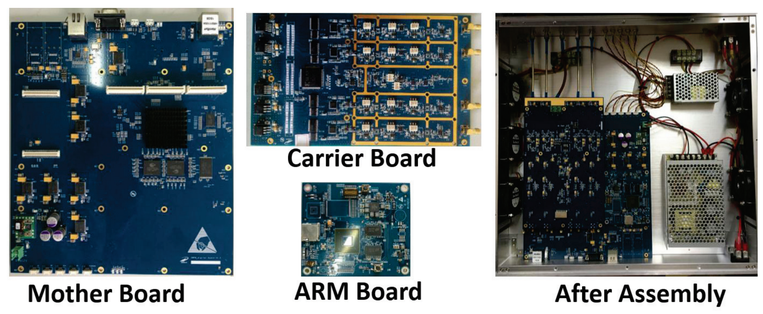
Hardware consists of three boards: RF carrier board, digital mother board, and ARM board.
ADC 16bits@120MHz
FPGA XC5VSX50T
ARM IMX6Q



Two bandpass SAW filters are centeralized at 500MHz. A step attenuator enables 32dB dynamic range.

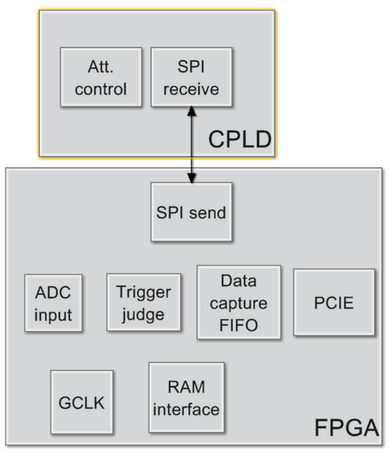


Mother board

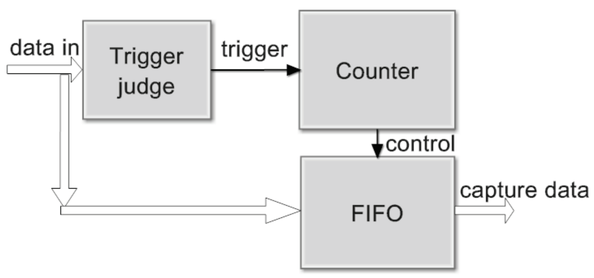


Clock can be set internal and external. And trigger can be self generated or from external.

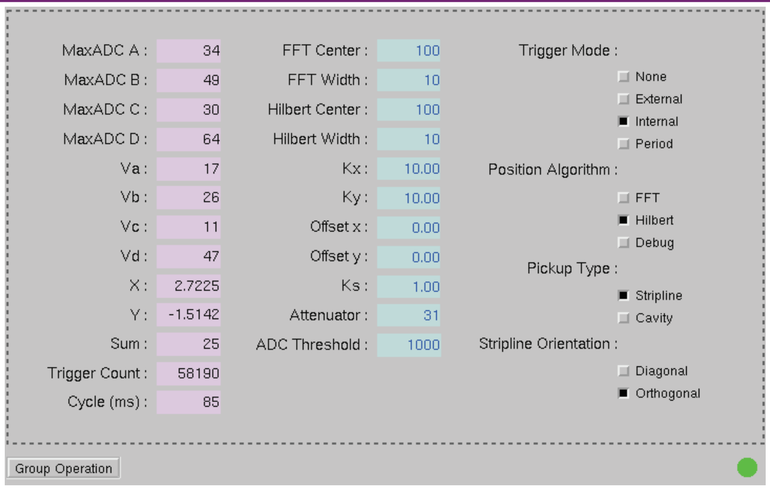
Firmware and software



Firmware developments including CPLD on RF board and FPGA on motherboard. CPLD is used to control RF attenuation, and the setting value comes from SPI bus between CPLD and FPGA. Communication between FPGA and ARM board is through PCIE .

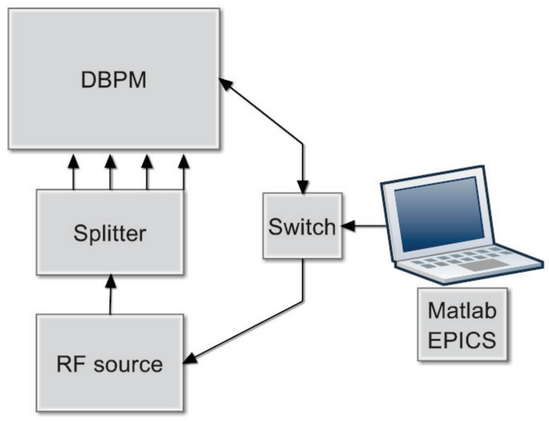


An innovative self-trigger generation module has been implemented, which enables the processor running without external trigger and improves the adaptability.

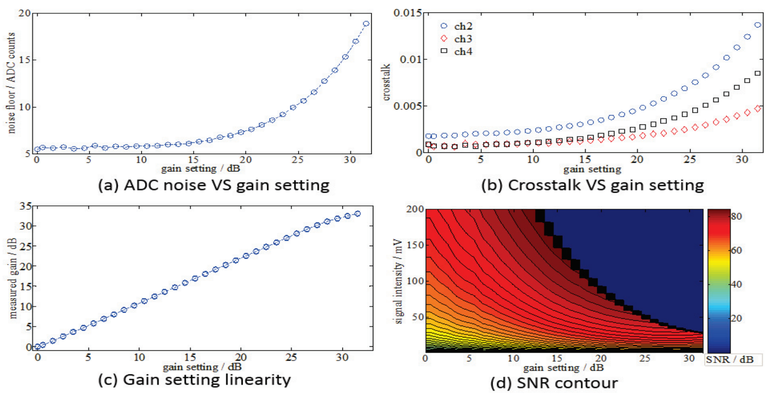


The control system is based on EPICS. Both Hilbert and FFT algorithms. And different position calculations are supplied according to different BPM types.

Lab tests

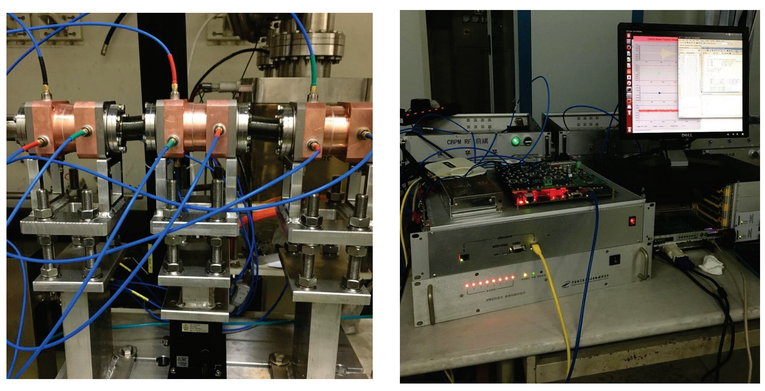


An automatic test platform has been design to improve the test efficiency. A PC running Matlab and EPICS controls the RF output signal source and the DBPM attenuator settings through TCP/IP protocol.

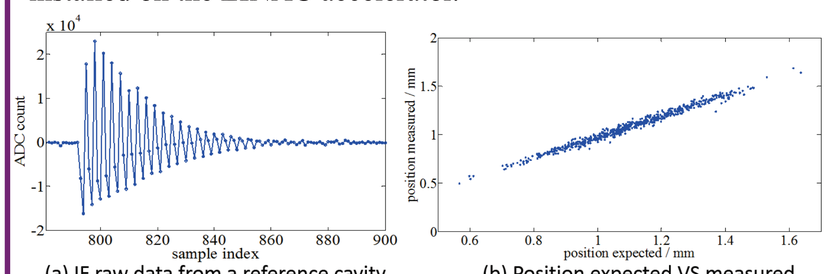


Figures (a) and (b) show that the noise level and the crosstalk keep almost the same low level when the attenuator is set to be 16~31dB. Figure (c) shows the good linearity between the setting and the output of the gain. Figure (d) indicates that the SNR can be better than 76dB, which means that the effective bits is greater than 12bits.

Tests at the SDUV



Tests has been carried out on the SDUV, which is a FEL test facility in SINAP. Three adjacent high Q cavity BPMs are installed on the LINAC accelerator.



Test results show that DBPM can capture the intermediate frequency (IF) cavity BPM signal correctly, and the resolution can be better than 1 μm, which reaches the performance requirement of the cavity BPM system.

Application at the DCLS

There are 8 stripline BPMs and 10 cavity BPMs at the DCLS. Because the accelerator is still under commissioning, precise BPM system performance evaluation will be carried out in the future.

Conclusions

A new DBPM processor has been designed for both stripline and cavity BPM. The effective bits can be greater than 12 when the input signal level and attenuation value are fitted. SDUV tests show that the DBPM works correctly. DBPMs have been applied on DCLS, because the accelerator is still under commissioning, system performance evaluation will be carried out in the future.

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