A prototype of the DBPM has been developed successfully at the SINAP during the past few years. Some tests and applications have been carried out at the Shanghai Synchrotron Radiation Facility (SSRF). Since 2015, two FEL facilities, DCLS and SXFEL, have been under constructions. Dozens of stripline BPMs and cavity BPMs are planted along the LINAC accelerators and the undulators. To handle the BPM data acquisitions and the position calculations, a new in-house BPM processor has been designed.

A new DBPM processor has been designed for both stripline and cavity BPM. The effective bits can be greater than 12 when the input signal level and attenuation value are fitted. SDUV tests show that the DBPM works correctly. DBPMs have been applied on DCLS, because the accelerator is still under commissioning, system performance evaluation will be carried out in the future.

The control system is based on EPICS. Both Hilbert and FFT algorithms. And different position calculations are supplied according to different BPM types.

Lab tests

Firmware developments including CPLD on RF board and FPGA on motherboard. CPLD is used to control RF attenuation, and the setting value comes from SPI bus between CPLD and FPGA. Communication between FPGA and ARM board is through PCIe.

Tests at the SDUV

Tests has been carried out on the SDUV, which is a FEL test facility in SINAP. Three adjacent high Q cavity BPMs are installed on the LINAC accelerator.

Application at the DCLS

There are 8 stripline BPMs and 10 cavity BPMs at the DCLS. Because the accelerator is still under commissioning, precise BPM system performance evaluation will be carried out in the future.