The SLAC LINAC LLRF CONTROLS UPGRADE

SLAC NATIONAL ACCELERATOR LABORATORY

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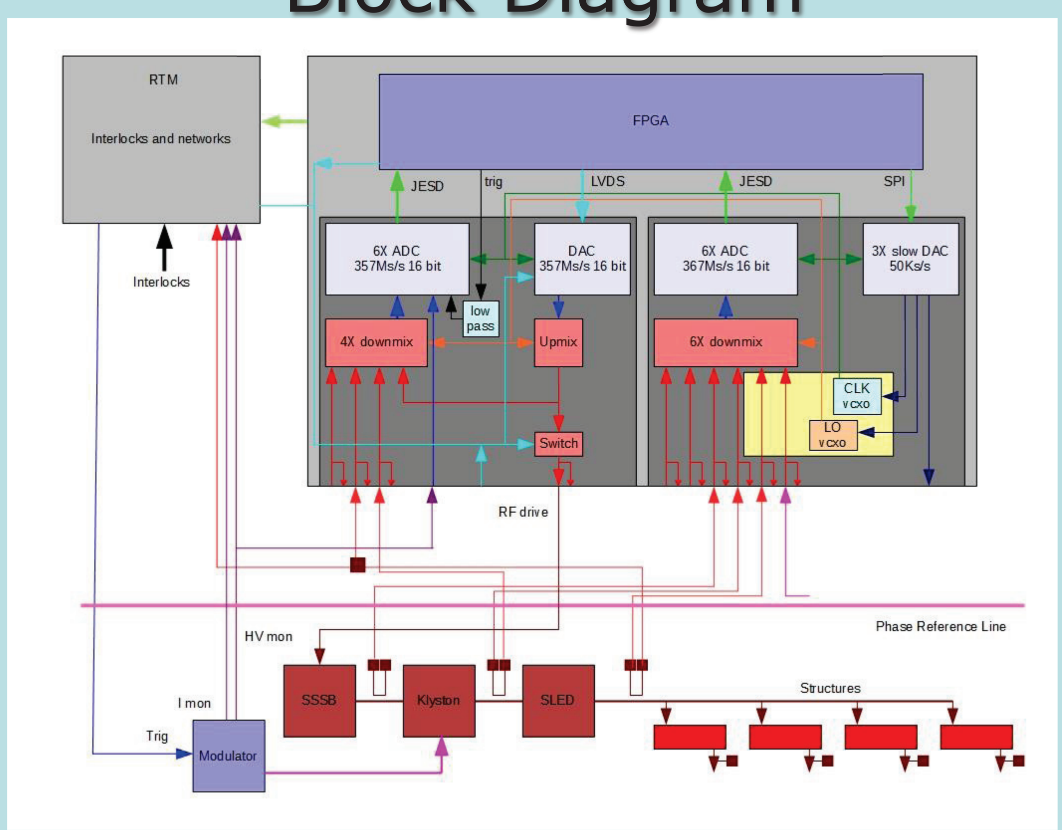
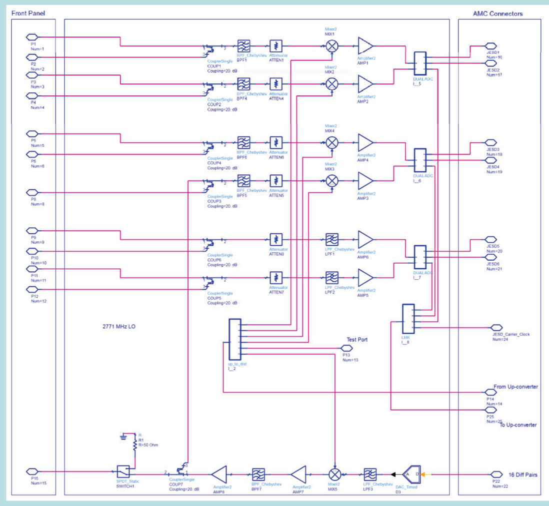
Abstract

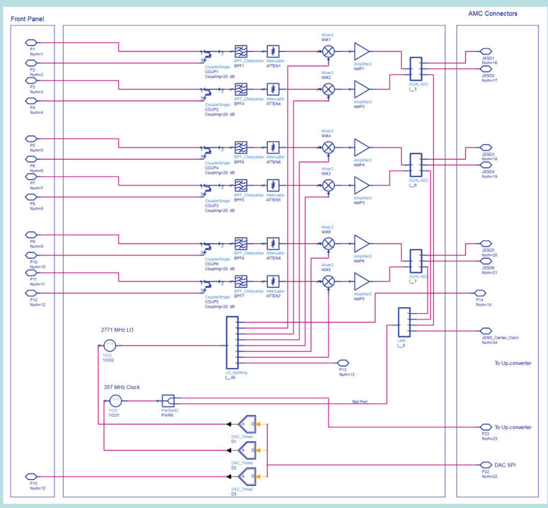
The low level RF control for the SLAC LINAC is being upgraded to provide improved performance and maintainability. RF control is through a high performance FPGA based DDS/DDC system built on the SLAC ATCA common platform. The klystron and modulator interlocks are being upgraded, and the interlocks are being moved into a combination of PLC logic and a fast trip system. A new solid state sub-booster amplifier will eliminate the need for the 1960s vintage high RF phase shifters and attenuators.

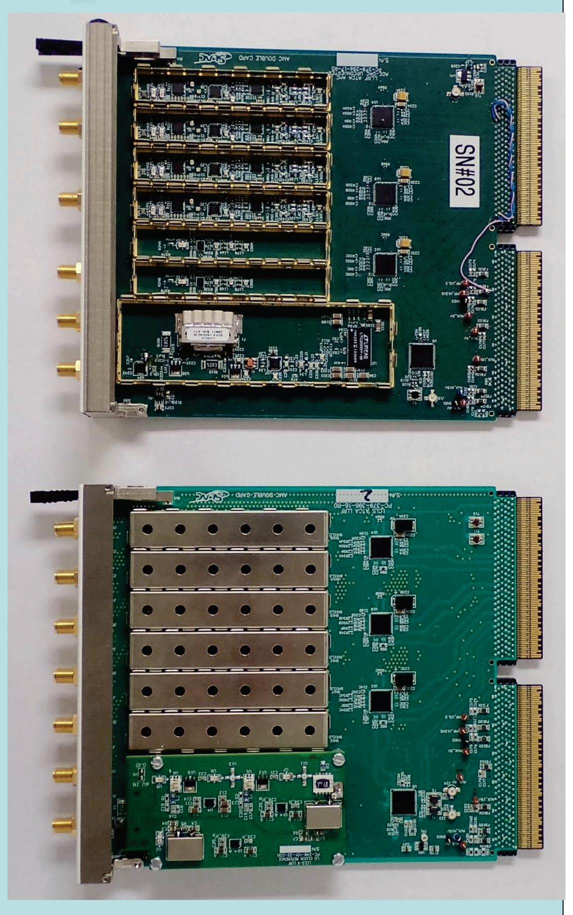
Block Diagram



AMC Board Design Overview

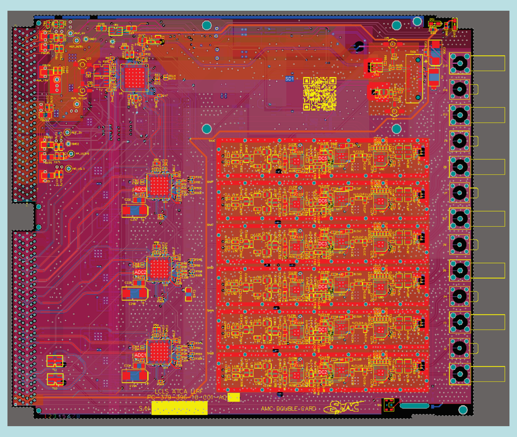


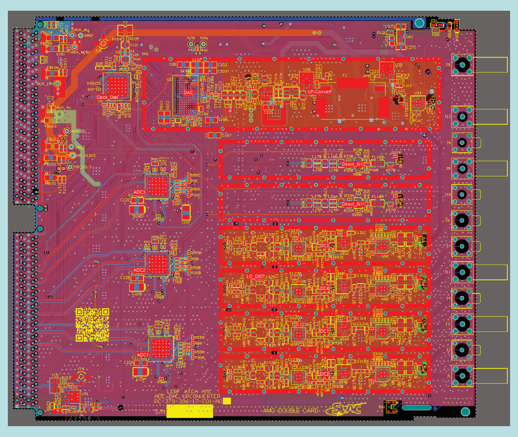




The Board layout design was challenging due to several factors. One is the sheer number of ADC inputs per board (6). The other was the fact that the LO’s and clocks are running all over the board, and need to be carefully routed and shielded so as not to cause interference (and spurs) on the input to the ADC.

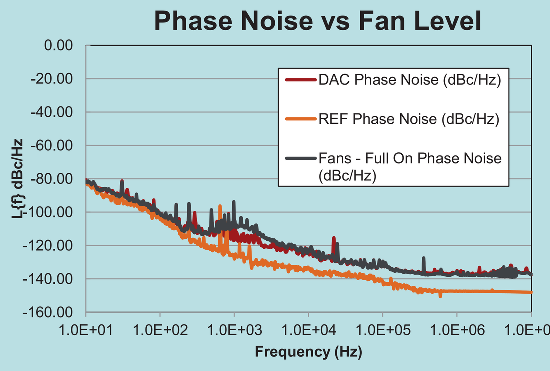
Revision 1 of Board Layouts

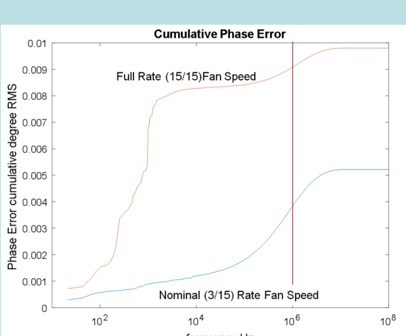




We are pleased with the initial testing results. Shown below are some of the key things we were “worried” about due to both the new platform as well as the density of the boards. Phase noise vs fan speed and isolation channel to channel.

Phase Noise vs Fan Level

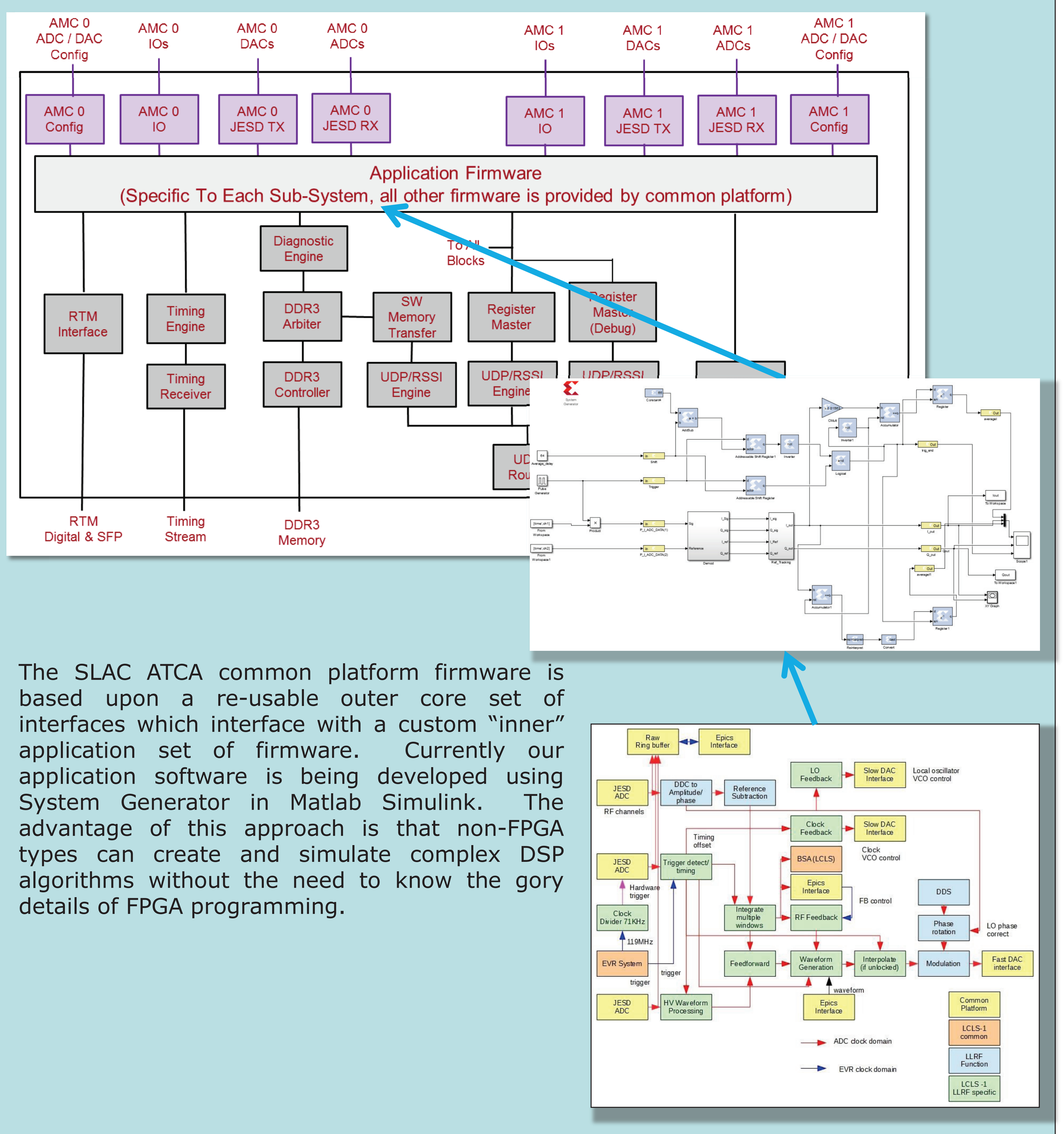




READ	DRIVE	ADC1A	ADC1B	ADC2A	ADC2B	ADC3A	ADC3B	ADC1A	ADC1B	ADC2A	ADC2B
		B0Ch1	B0Ch2	B0Ch3	B0Ch5	B0Ch4	B0Ch6	B1Ch1	B1Ch2	B1Ch4	B1Ch3
ADC1A	B0Ch1	-3.683	-69.2	-64.46	-77.7	-73.6	-79.5	-97.8	-93.4	-95	-98.9
ADC1B	B0Ch2	-73.16	-7.836	-67.95	-83.7	-80.6	-86.5	-98.6	-92.3	-91	-92.9
ADC2A	B0Ch3	-63.17	-64.5	-5.06	-72.7	-74.7	-80.2	-89.7	-85.7	-89	-88.5
ADC2B	B0Ch5	-81.37	-76.55	-77.98	-7.79	-71.4	-28.5	-87.5	-92.7	-96	-89.1
ADC3A	B0Ch4	-72.94	-89.02	-77.46	-77.2	-5.5	-82.9	-89.6	-91.9	-89	-84.8
ADC3B	B0Ch6	-74.37	-74.55	-84.27	-28.5	-73.1	-5.16	-84.9	-83	-84	-99.6
ADC1A	B1Ch1	-91.5	-90.3	-90.9	-89	-89	-80	-7.201	-71.08	-62.6	-72.02
ADC1B	B1Ch2	-92.3	-90.8	-83.7	-84	-81	-76	-68.51	-6.855	-71.7	-75.16
ADC2A	B1Ch3	-81.9	-75.4	-77.6	-79	-85	-76	-72.24	-72.05	-14	-64.39
ADC2B	B1Ch4	-84.2	-92.4	-88.2	-97	-83	-83	-75.22	-84.61	-73.3	-7.567

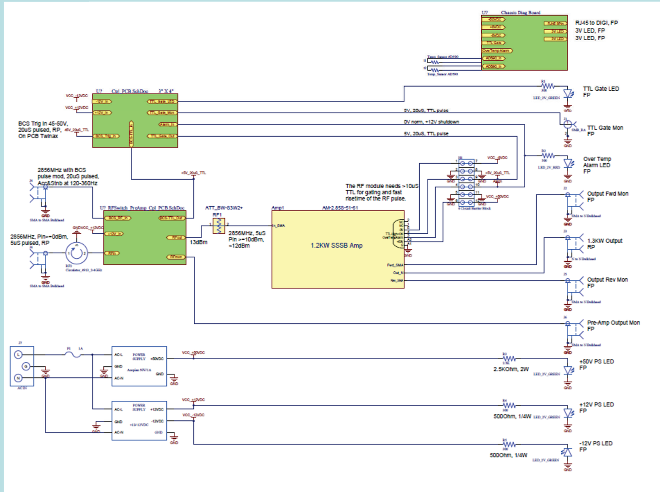
Isolation measurements in general meet our specifications. The board turn will improve these numbers by adding many extra ground shielding vias between channels as well as inputs. The Isolation issue between ADC3B and ADC3A is well understood and has been rectified as well.

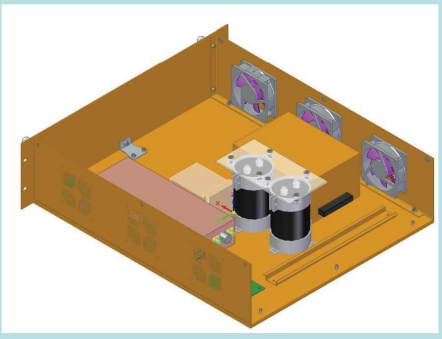
Firmware/Common Platform

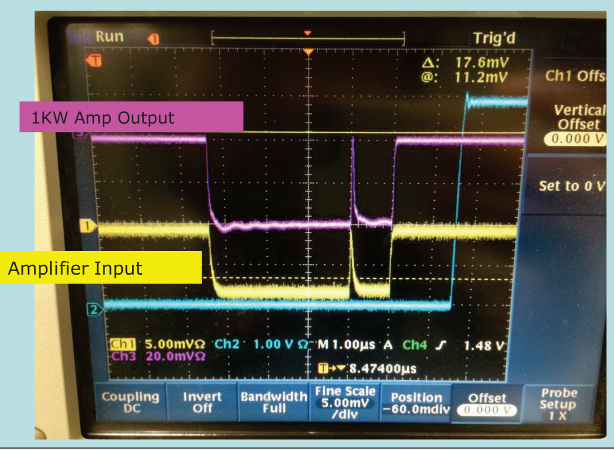


The SLAC ATCA common platform firmware is based upon a re-usable outer core set of interfaces which interface with a custom “inner” application set of firmware. Currently our application software is being developed using System Generator in Matlab Simulink. The advantage of this approach is that non-FPGA types can create and simulate complex DSP algorithms without the need to know the gory details of FPGA programming.

Solid State Sub-Booster

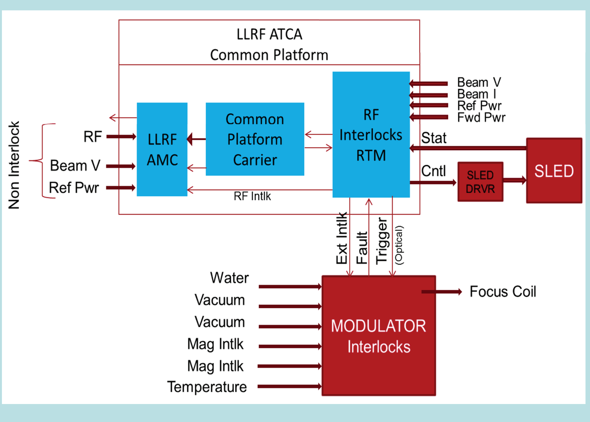


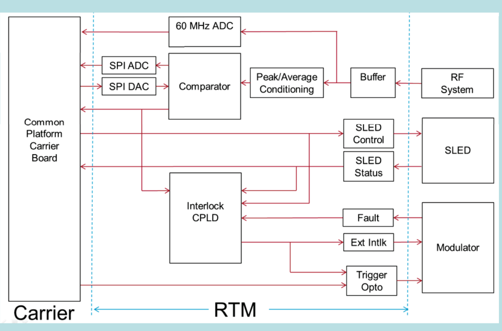


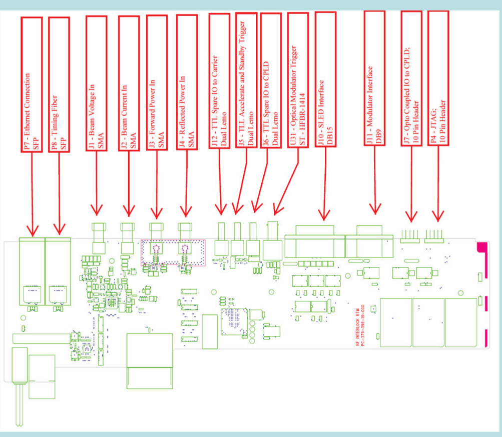


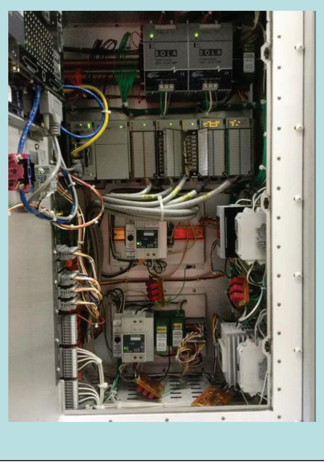
The new SSSB amplifier is a completely new design based upon an amplifier “brick” purchased commercially. The chassis, power supply and “brick” will be combined together using industry assembly houses. Testing and final verification will be completed at SLAC.

Interlocks









The original station protection interlocks used to be handled by a separate chassis called the Modluator Klystron Support Unit (MKSU). In the new design the functionality will be split into two. Part will be handled by a new ATCA RTM and the other will be handled by the PLC in the previously upgraded modulators.

RTM Handles
- Beam Volts
- Beam Current
- Reflected Power
- Forward Power
- SLED Interlock
- SLED Control

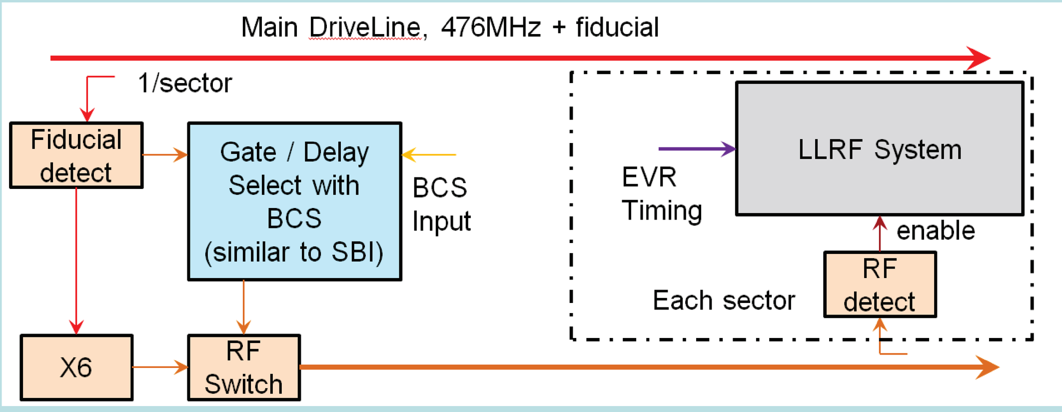
Modulator Handles
- Modulator On/OFF/Reset
- Modulator 12 Status bits (HV on, HV off, HVOC, etc.)

New PLC functions Transferred from MKSU
- Water
- Vacuum
- Klystron Solenoid Power Supply
- RF Station temperatures (Klystron delta T, RF window)

Beam Containment

Beam Containment is a critical function partially maintained via the RF system. When a beam containment trip occurs, rather than shut off the RF stations which would result in a cool down of the accelerating structures, klystrons, etc, the timing of the RF pulse is shifted to a standby time. To maintain compatibility with the existing system while we are potentially upgrading and to keep the approval process to hopefully a manageable level of bureaucratic finagling, we’ve come up with a system that can coexist with the legacy system while still maintaining the overall robust nature of the system.

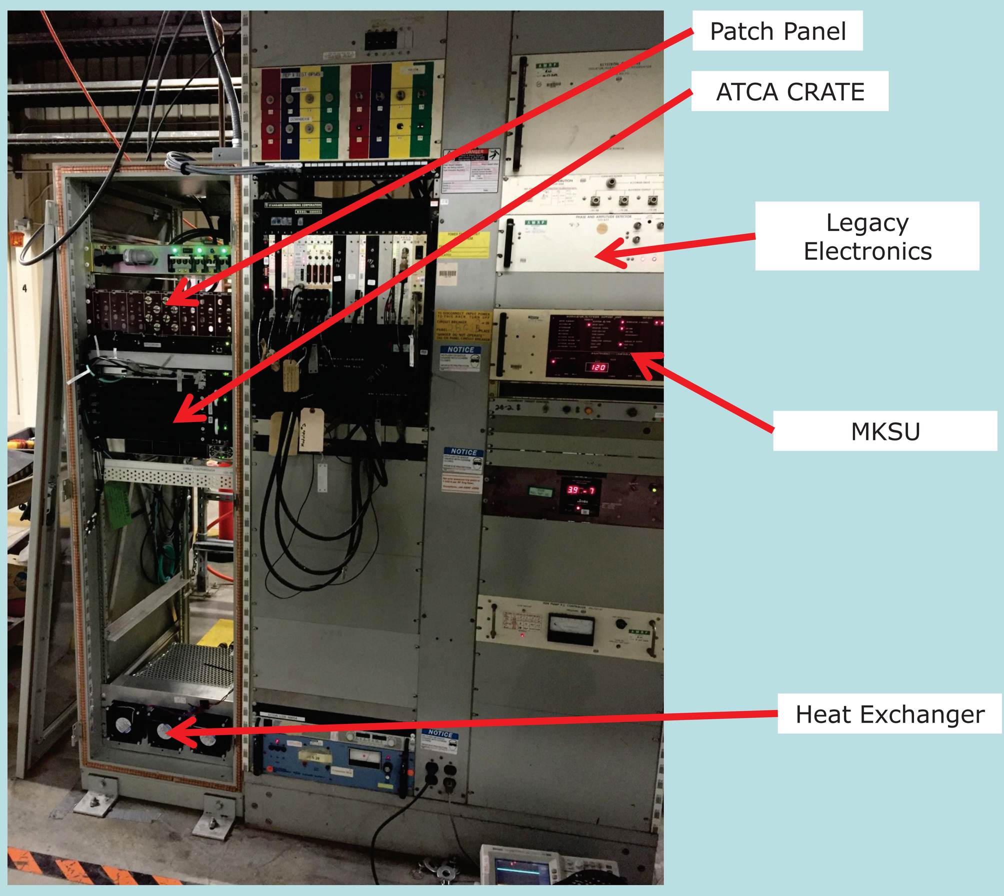
- BCS gate generated at the sector start – transmitted to stations as a S-band tone burst on the sub drive line.
- Tone burst on SDL gates the RF output (hardware switch) for each station EVR fiber read by LLRF system also shifts timing (similar to existing system)



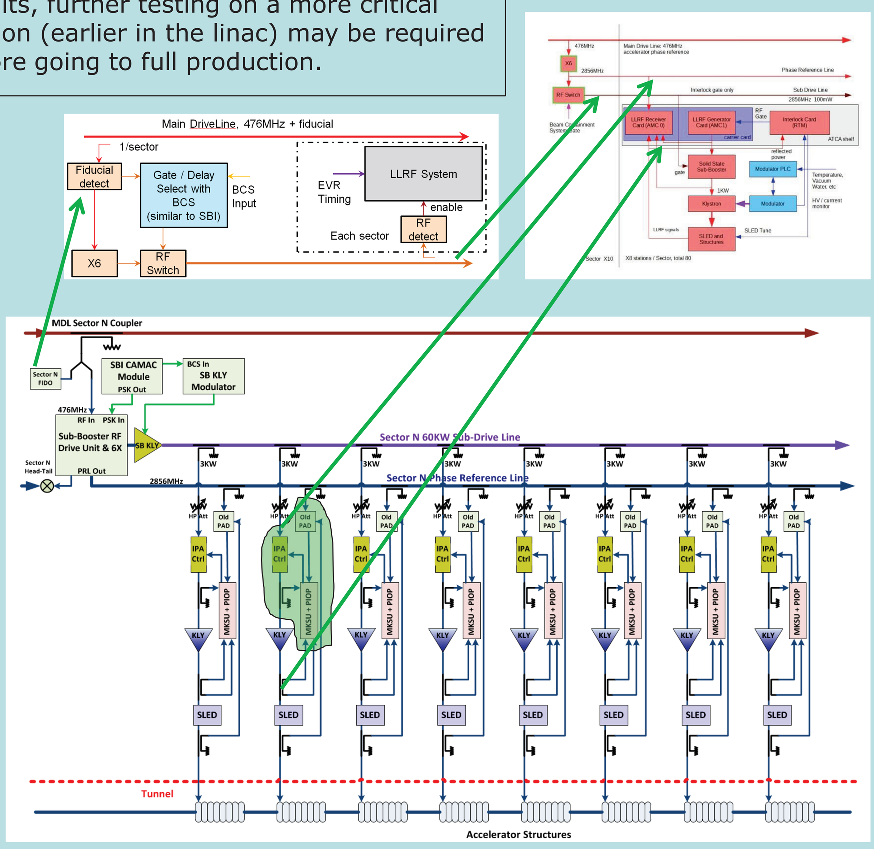
- Design allows a mix of old and new MR stations in a sector:
  - Sector sub-booster is used as long as any legacy stations are in a sector
  - Sub Drive Line signal attenuated by high power attenuator to provide a low level input to the BCS gate for each station.
- Reliability
  - Natural redundancy from multiple stations used in legacy system and for new system
  - Independent time shift from timing system and BCS gate.

Next Steps

We are in the process of installing/upgrading a rack in one station of the existing LCLS-I linac. This station will sit next to an existing rack of LLRF equipment and is designed to be “easily” switchable between configurations. This testing must be complete before SLAC goes into a six month down at the end of this calendar year (for LCLS-II construction activities). We need to get this valuable live testing on our existing linac so that when we come up from the down we will (hopefully) be able to begin upgrading stations all down the linac..



This test will provide invaluable information about our integration plan as well as actual beam performance (although somewhat limited) due to this station. Depending on results, further testing on a more critical station (earlier in the linac) may be required before going to full production.



Acknowledgments

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