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Collider-Accelerator Department

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A Versatile BPM Signal Processing System Based on the Xilinx Zynq SoC*

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Abstract

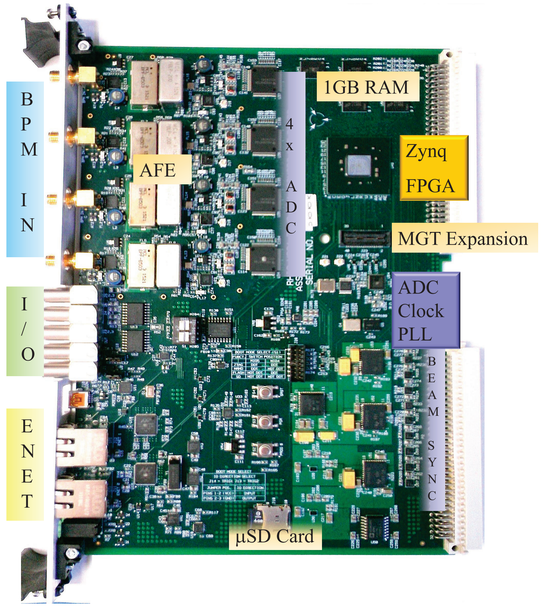
A new BPM electronics module has been developed at BNL that makes use of the latest System on a Chip (SoC) technologies to provide a system with better performance and lower cost per module than before. The future of RHIC ion runs will include new RF conditions as well as a wider dynamic range in intensity. Plans for the use of electron beams, both in ion cooling applications and a future electron-ion collider, have also driven this architecture toward a highly configurable approach. The RF input section has been designed such that jumpers can be changed to allow a single board to provide ion or electron optimized analog filtering. These channels are sampled with four 14-bit 400MSPS A/D converters. The SoC's ARM processor allows a Linux OS to run directly on the module along with a controls system software interface. The FPGA is used to process samples from the ADCs and perform position calculations. A suite of peripherals including dual Ethernet ports, µSD storage, and an interface to the RHIC timing system are also included. A second revision board which includes ultra-low jitter ADC clock synthesis and distribution and improved power supplies is currently being commissioned.

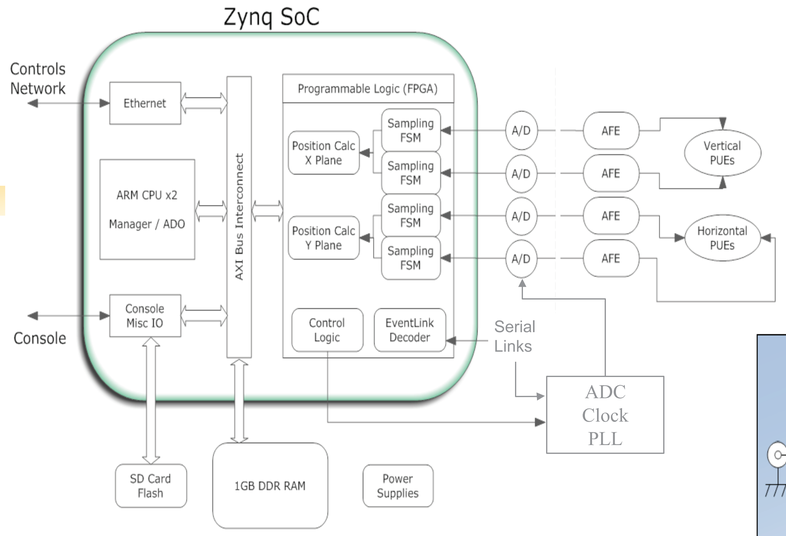
History and Purpose

After a proof of principle prototype was successfully tested using off the shelf evaluation boards, work began to design a complete BPM system on a VME form factor, with specific enhancements to suit the RHIC's timing infrastructure.

The board shown right is the second hardware revision of that endeavor. This design has proven to be extremely flexible, with many different analog filtering options being used on the hardware. Meanwhile, the firmware which runs on the FPGA and performs most of the processing has also constantly improved and allows for a variety of measurement applications, at various different particle accelerators at BNL.

A few examples of the variety of uses this system has had even in its prototype stage are shown below. There are future electron beam BPM systems coming online (LEReC) that will be using this hardware as well.



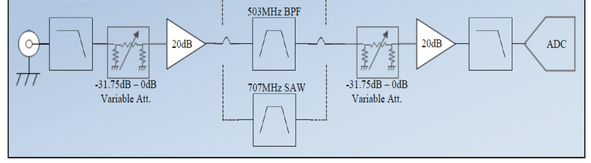


Analog Front End

(2) Gain Stages & (2) Digital Step Attenuators

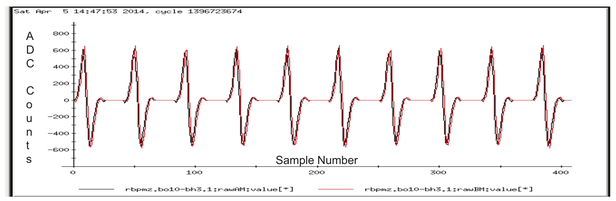
(4) Signal Paths (Solder Jumper Selectable)

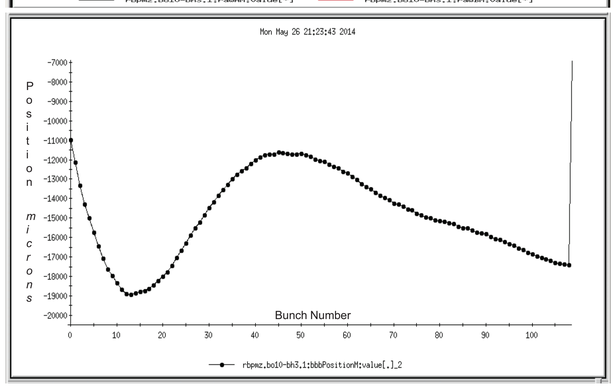
- ➢Low Pass (39MHz and 200MHz)
- ➢Band Pass (503MHz)
- ➢Band Pass SAW (707 MHz)
- ➢Bypass



RHIC Dump BPM Bunch-by-Bunch Position

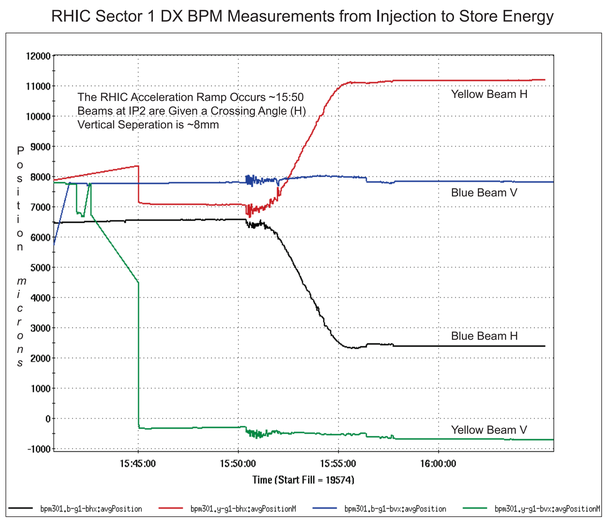
As the abort kicker voltage varies each bunch is kicked differently, as seen here using a BPM installed between the kicker and absorber. The raw data shown above is sampled at ~400MHz and uses an external 39MHz low pass filter. The plot below shows each of the 111 bunch's position in microns after they are kicked by the abort magnets.





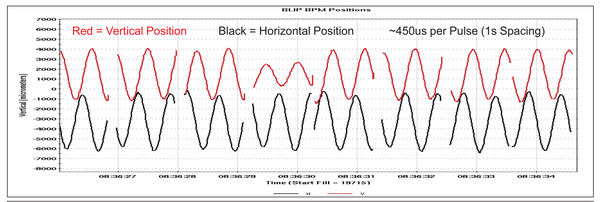
RHIC DX BPM – Pickup Common to Two Beams

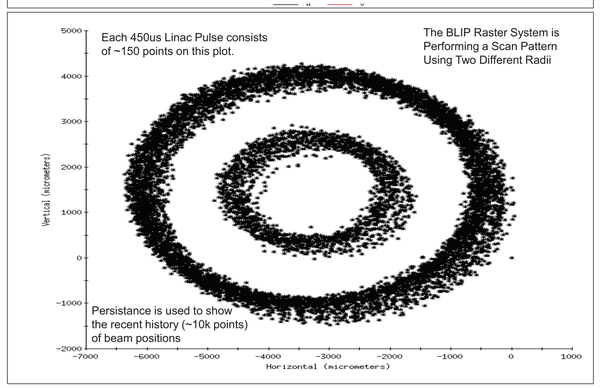
Both Blue and Yellow RHIC ring ion beams travel trough the same BPM pickups on either side of each intersection region. Here the electronics is simultaneously processing two different sets of bunches, allowing both beam positions to be calculated by the same pair of hardware channels.



BLIP Raster Upgrade BPM

As the Linac beam is scanned by the raster magnet, a dual plane BPM mounted downstream measures its circular motion. The same hardware and similar firmware used at RHIC for bunch by bunch measurements is used to slice the 450µs Linac pulse into small pieces, each having its position calculated separately and put into an array.





ATF Electron Beam Tests

At the Brookhaven Accelerator Test Facility the signal from a stripline BPM is shown here, using the 503MHz band pass filter in the analog chain. The ATF produces a single electron bunch at a 1Hz rate which causes the filter to ring, allowing us to record 15-20 samples for each pulse. A plot of positions vs. time is also shown below.