FIRST BEAM TESTS OF THE APS MBA UPGRADE ORBIT FEEDBACK CONTROLLER*

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Abstract

The new orbit feedback system required for the APS multi-bend acromat (MBA) ring[1] must meet challenging beam stability requirements. The AC stability requirement is to correct rms beam motion to 10% the rms beam size at the insertion device source points from 0.01 to 1000 Hz. The vertical plane represents the biggest challenge for AC stability which is required to be 400 nm rms for a 4 micron vertical beam size. In addition, long term drift over a period of 7 days is required to be 1 micron or less at insertion device BPMs and 2 microns for arc bpms. We present test results of the MBA prototype orbit feedback controller (FBC) in the APS storage ring. In this test, four insertion device BPMs were configured to send data to the FBC for processing into four fast corrector setpoints. The configuration of four bpms and four fast correctors creates a 4-bump and the configuration of fast correctors is similar to what will be implemented in the MBA ring. We report on performance benefits of increasing the sampling rate by a factor of 15 to 22.6 kHz over the existing APS orbit feedback system, limitations due to existing storage ring hardware and extrapolation to the MBA orbit feedback design. FBC architecture, signal flow and processing design will also be discussed.

4x4 Test Layout and Beam Stability Requirements

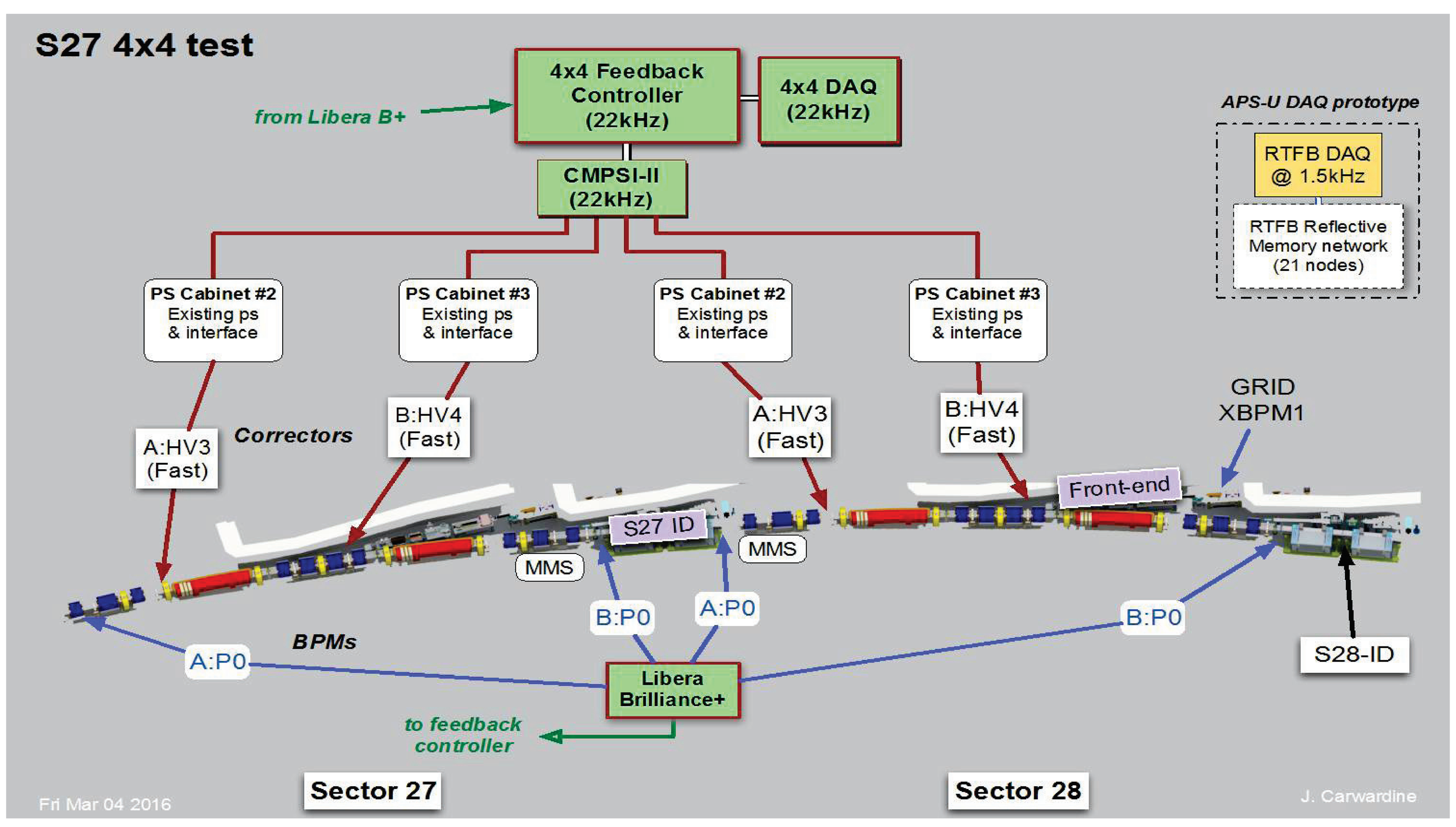

Figure 1. Four corrector, four BPM "4x4 test" layout in sectors 27 and 28 of the APS storage ring. New signal processing hardware is indicated in green

- Figure 1. shows the "4x4 test" consisting of four insertion device (ID) "P0" bpms and four horizontal or vertical fast correctors (the [A,B]:HV[3,4] combined H and V correctors)
- New hardware shown in green:
  - Libera Brilliance+ (LB+) commercially available bpm processor (Instrumentation Technologies, Solkan, Slovenia)
  - Feedback controller to process bpm data at the turn-by-turn (TBT) rate (271 kHz)
  - Data acquisition system (DAQ) to acquire data at 22.6 (every 12th turn) rate
  - CMPSI-II interface to transfer processed corrector setpoints to existing (CMPSI) fast corrector power supply interface
- Operations Orbit feedback system DAQ acquiring data from all correctors and bpms at 1.5 kHz (except for bpms and correctors used in the 4x4 test)
- Studies were conducted using 324 equally spaced bunches for a 60 hour lifetime at 102 mA stored beam current
- LB+ had nearly a CW signal at the bpm analog input end (switching and filtering off)
- No need for top-up due to the long lifetime so no top-up beam motion transients

Plane	AC Motion (0.01-1000 Hz) Position (rms)	AC Motion (0.01-1000 Hz) Angle (rms)	Long-term Drift (>100 s) Position (rms)	Long-term Drift (>100 s) Angle (rms)
Horizontal	1.7 μm	0.26 μrad	1.0 μm	0.6 μrad
Vertical	0.4 μm	0.17 μrad	1.0 μm	0.5 μrad

Table 1: Beam Stability Requirements for the MBA Ring

- Table 1. shows the challenging beam stability requirements for the proposed APS MBA ring upgrade
  - AC motion specified in the band 0.01-1000 Hz as 10 % the rms beam size at the insertion devices (IDs)
  - Long-term stability defined for times longer than 100 seconds up to 7 days (length of time between maintenance periods)
  - Long-term stability based on an estimate of diffusive ground motion
- Main goals for the test:
  - Increase the sampling rate - 22.6 kHz (factor of 15 above existing orbit feedback rate)
  - Demonstrate all hardware working together and measure closed-loop bandwidth and step response and compare to existing real-time orbit feedback (RTFB) system

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Feedback Controller Signal Flow, Processing, Control and Hardware

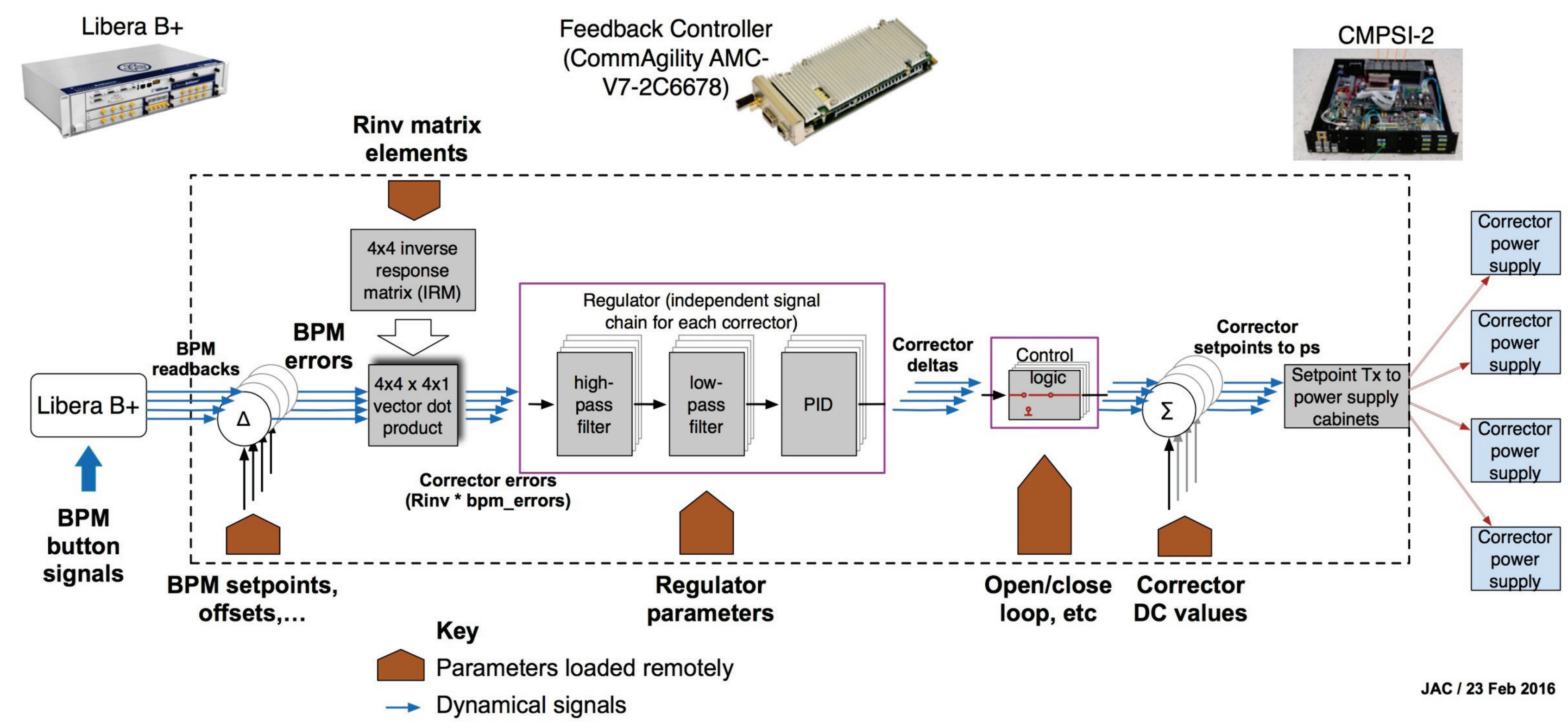

Figure 2. FBC signal flow diagram starting with bpm data on the left to fast corrector setpoints on the right. Shown at the top of the figure are pictures of the new hardware including: commercial BPM electronics (LB+) available from Instrumentation Technologies, the FBC CommAgility AMC-V7-2C6678 (microTCA based) board and the CMPSI-2 fast corrector interface which uses a Xilinx Zinq FPGA

- Figure 2. shows the signal flow from TBT bpm data to fast corrector setpoints
- FBC uses a microTCA based CommAgility AMC-V7-2C6678 with:a Xilinx Virtex 7 FPGA and dual TMS320C6678 DSPs with 8 cores each
- Reuse existing C code from RTFB system and put the feedback algorithm on one DSP core
- Can use the other 15 remaining cores for other fast processing of bpm and fast corrector data (PSDs, integrated PSDs, rms in a given bandwidth etc.)
- FPGA transfers TBT data to DSPs for processing and transmits processed fast corrector setpoints to the power supplies (ultimately transfer bpm/corrector data to other FBCs)
- DAQ software provides a convenient interface to acquire data sets at 22.6 kHz and generate bpm setpoint/corrector steps for frequency and step response measurements

Closed-Loop Bandwidth and Closed/Open-Loop Step Response

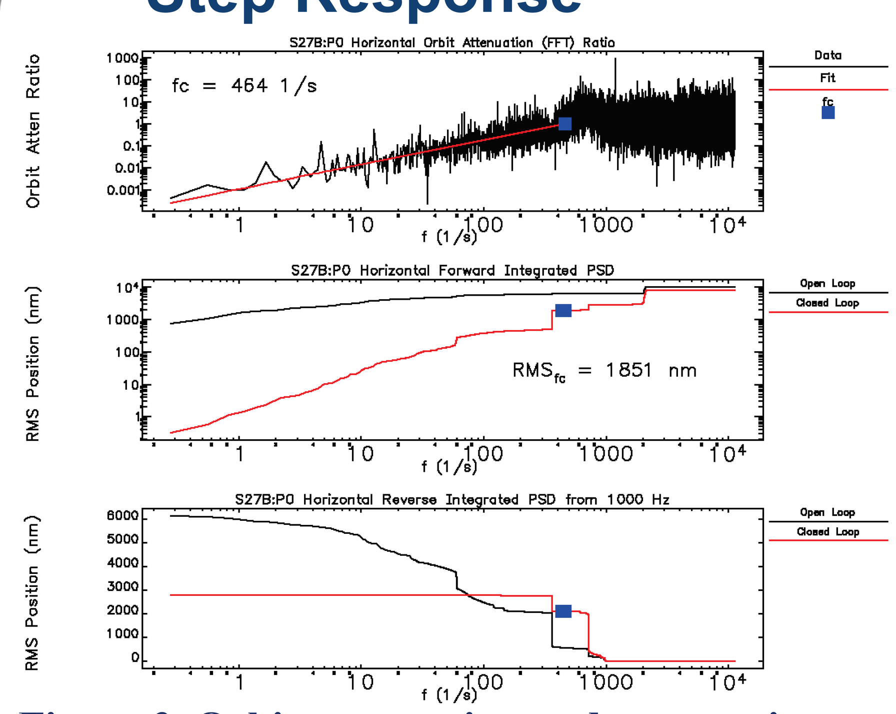

Figure 3. Orbit attenuation and rms motion

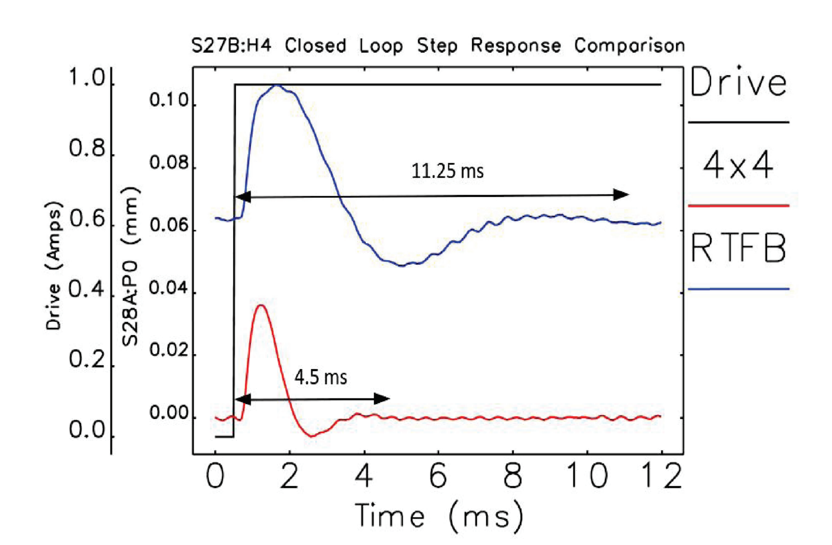

Figure 4. Closed-loop step response comparison

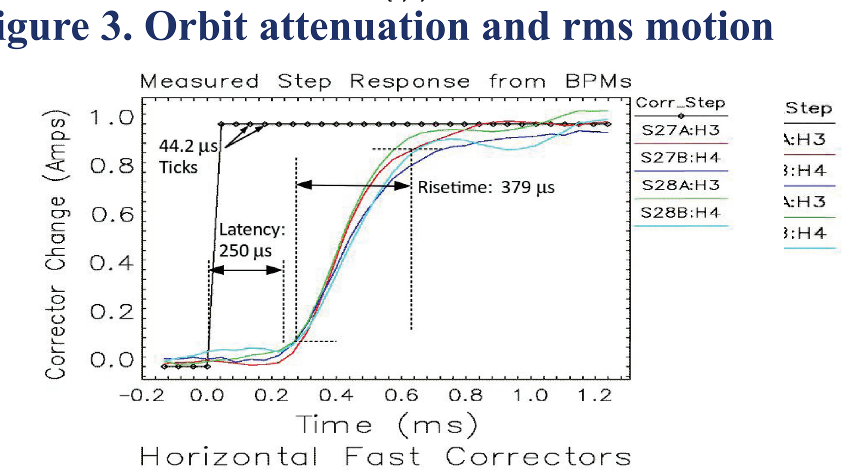

Figure 5. Open-loop horizontal fast corrector step response

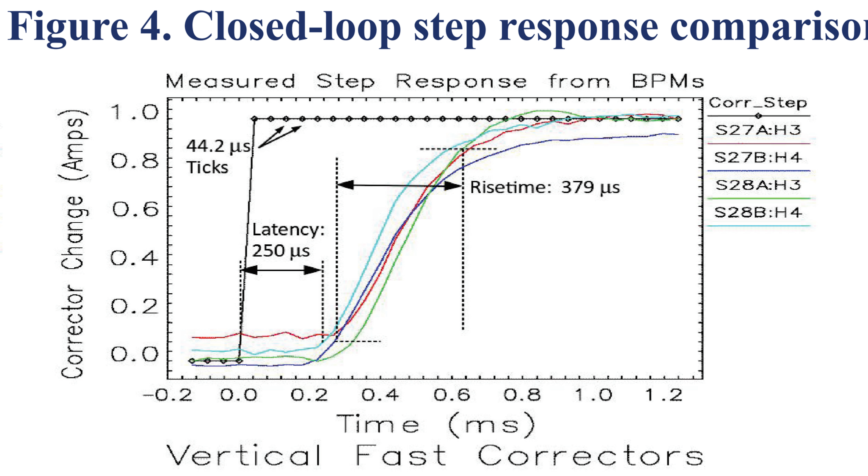

Figure 6. Open-loop vertical fast corrector step response

- 4x4 test sampling rate (corrector update rate) was 22.6 kHz or a factor of 15 above RTFB
- 4x4 test closed-loop bandwidth achieved was 464 Hz or a factor of 5 above RTFB (integral and proportional control used to maximize closed-loop bandwidth)
- 4x4 test closed-loop step response (integral control only) was 2.5 times faster than RTFB
- Limiting factor for increased closed-loop bandwidth is latency/risetime of existing fast corrector power supplies

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References

[1] M. Borland etal. "Hybrid Seven-Bend-Achromat Lattice for the APS Upgrade," IPAC (2015).