

FIRST BEAM TESTS OF THE APS MBA UPGRADE ORBIT FEEDBACK CONTROLLER*

N. S. Sereno[†], N. Arnold, A. Brill, H. Bui, J. Carwardine, G. Decker, B. Deriy, L. Emery, R. Farnsworth, T. Fors, R. Keane, F. Lenkszus, R. Lill, D. Paskvan, A. Pietryla, H. Shang, S. Shoaf, S. Veseli, J. Wang, S. Xu, B. X. Yang,
ANL, Argonne, IL, USA 60439

Abstract

The new orbit feedback system required for the APS multi-bend acromat (MBA) ring must meet challenging beam stability requirements. The AC stability requirement is to correct rms beam motion to 10 % the rms beam size at the insertion device source points from 0.01 to 1000 Hz. The vertical plane represents the biggest challenge for AC stability which is required to be 400 nm rms for a 4 micron vertical beam size. In addition long term drift over a period of 7 days is required to be 1 micron or less at insertion device BPMs and 2 microns for arc bpm. We present test results of the MBA prototype orbit feedback controller (FBC) in the APS storage ring. In this test, four insertion device BPMs were configured to send data to the FBC for processing into four fast corrector setpoints. The configuration of four bpm and four fast correctors creates a 4-bump and the configuration of fast correctors is similar to what will be implemented in the MBA ring. We report on performance benefits of increasing the sampling rate by a factor of 15 to 22.6 kHz over the existing APS orbit feedback system, limitations due to existing storage ring hardware and extrapolation to the MBA orbit feedback design. FBC architecture, signal flow and processing design will also be discussed.

INTRODUCTION

Figure 1 shows the layout of the “4x4-test” in sectors 27 and 28 of the APS storage-ring (SR). In green are shown the new orbit feedback hardware including the new FBC to process bpm data and generate corrector setpoints. Four insertion device A:P0 and B:P0 bpm are connected to commercial Libera Brilliance+ (LB+) bpm electronics from Instrumentation Technologies, Solkan, Slovenia to obtain beam position for processing in the FBC. The FBC receives the turn-by-turn (TBT) or 271 kHz beam position data, decimates it by twelve to 22.6 kHz and processes it to obtain corrector setpoints. The corrector setpoints are then applied using an interface (CMPSI-2) between the FBC and the existing fast corrector power supply (PS) controls. The four horizontal and vertical fast correctors used are the A:HV3s and B:HV4s in sectors 27 and 28. In addition the FBC is able to send its bpm and corrector data to a data acquisition system (DAQ) which allows the data to be captured and provides a convenient interface to perform step response measurements (at the 22.6 kHz corrector update rate).

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[†] sereno@aps.anl.gov

Additional diagnostics shown in the figure include the mechanical motion system (MMS) system [1] and the next generation, grazing incidence insertion device (GRID) XBPM [2]. In these tests, we were most concerned with seeing what is required of the system to meet the AC stability specification so the MMS system data was not used by the FBC to correct for long term drift of the bpm. The GRID, also was not used but is presently used in the APS operations orbit feedback system. Table 1 lists the AC and long term beam stability requirements for the MBA ring.

To begin each study, the SR was filled to 102 mA in 324 equally spaced single bunches. Use of this bunch pattern is twofold: first, the LB+ bpm will have a clean, nearly CW signal at their rf inputs and hence all ADC samples in one turn can be used to compute the average beam position; second, this fill pattern has the longest lifetime (60 h) and there is no need for top-up. During top-up injection transients were expected to corrupt some of the data. Every so often, usually when the beam current dropped below 90-95 mA, we would do a fill-on-fill to 102 mA in the 324 bunch fill pattern.

We used the LB+ with its switching feature off so as to not corrupt the fast data stream (at TBT rates as sent to the FBC) with switching noise. The LB+ was operated in its time-domain processing (TDP) mode so as to reduce the latency as much as possible for data processing and transmission through the device (latency is 2 turns in this mode compared to its digital down-conversion (DDC) processing mode where the latency is 4 turns). Toward the end of the testing program reported here, we also implemented notch filtering to eliminate LB+ switching noise and a low-pass (LP) anti-alias filter in the LB+ to remove switching transients and prevent aliasing of signals above 11.3 kHz. The experiments reported in this note were all performed in the horizontal plane since the vertical plane response matrix was ill-conditioned when using all four singular values (SVs) to construct the inverse response matrix (irm).

FEEDBACK CONTROLLER SIGNAL FLOW, PROCESSING, CONTROL AND HARDWARE

Figure 2 shows the signal flow from bpm data to processed and applied fast corrector setpoints. After forming the bpm error by subtracting the orbit setpoint, the bpm data is multiplied by an irm calculated using standard SR high level software tools. The corrector errors can then be filtered and sent through a PID regulator to produce corrector

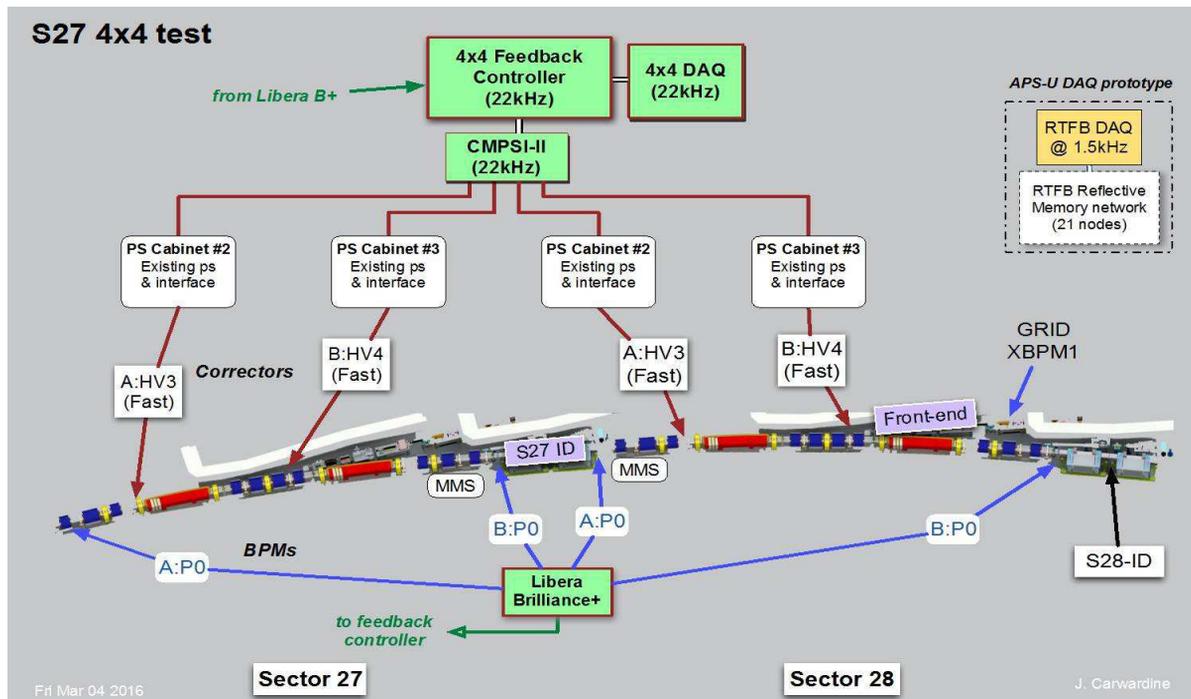


Figure 1: Four corrector, four BPM “4x4-test” layout in sectors 27 and 28 of the APS storage ring. New signal processing hardware is indicated in green.

Table 1: Beam Stability Requirements for the MBA Ring

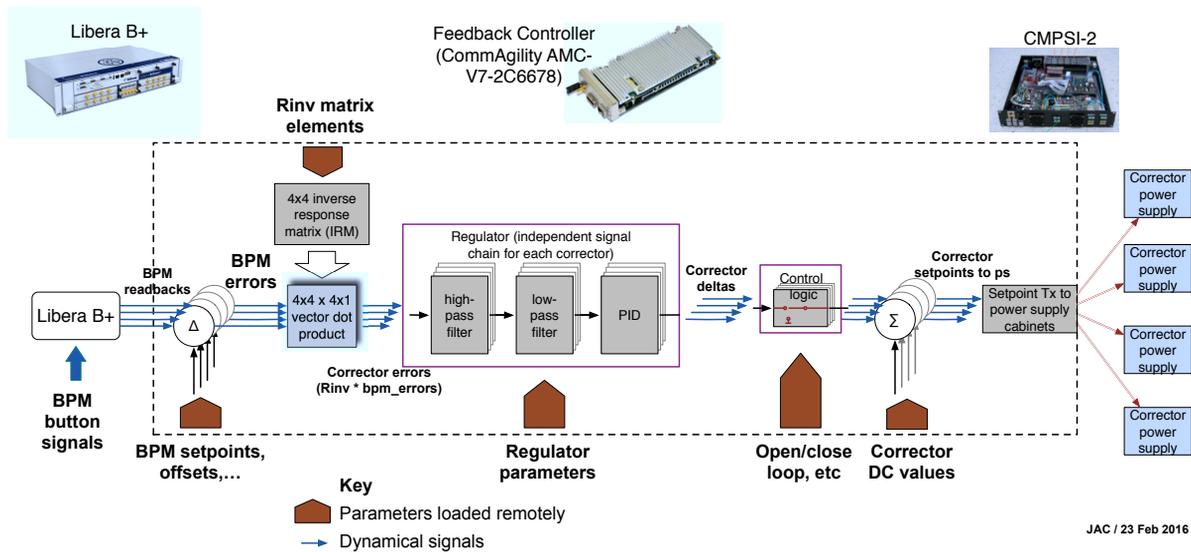
Plane	AC Motion	AC Motion	Long-term Drift	Long-term Drift
	(0.01-1000 Hz) Position (rms)	(0.01-1000 Hz) Angle (rms)	(>100 s) Position (rms)	(>100 s) Angle (rms)
Horizontal	1.7 μm	0.26 μrad	1.0 μm	0.6 μrad
Vertical	0.4 μm	0.17 μrad	1.0 μm	0.5 μrad

delta values which are then added to the corrector DC set-point and applied to the corrector CMPSI-2 interface. Main goals for the test are to demonstrate all hardware functioning together, increase the sampling rate by a factor of 15 over the existing real time feedback system (RTFB) to 22.6 kHz from 1.5 kHz, and demonstrate closed-loop bandwidth increase at the four P0 bpms in the loop above the 80-100 Hz closed-loop bandwidth of the present RTFB system. Initial testing reported here used no filtering of the bpm TBT data for closed-loop testing (only decimation by a factor of 12 to 22.6 kHz).

Figure 2 also shows pictures of the hardware used in the test. We used a microTCA-based CommAgility AMC-V7-2C6678 as the FBC which uses a Xilinx Virtex 7 FPGA to route data to two TMS320C6678 DSPs each with eight cores. We implemented the feedback algorithm shown in the figure on one core on one of the DSPs. This offered the flexibility of implementing the feedback algorithm in C code and allowed easy reuse of code from our existing RTFB system which is presently running a previous generation TMS320 DSP. Additional flexibility is afforded by the DSP hardware since additional processing of the same bpm

and corrector data can be done on the other 15 remaining DSP cores. The FPGA is used to receive TBT LB+ BPM data and send it to the DSP and receive processed corrector setpoints at 22.6 kHz (every 12 turns) from the DSP and send to the CMPSI-2. The CMPSI-2 consists of a Xilinx Zynq FPGA and is used to convert DSP corrector setpoints to the format used by the existing APS fast corrector interface. The DSP can also generate a step input using the bpm or corrector setpoints. In this way, step response measurements can easily be done. We measured step responses using this functionality to assess the latency in the existing fast corrector system and identify where latency reductions should be made in the future full integrated test in sectors 27 and 28 planned in fall of 2016.

A long term plan for the MBA ring is to implement the FBC system using a modular approach in a microTCA crate (the existing RTFB system uses VME). We anticipate using the present double-sector feedback architecture where each FBC has access to two sectors worth of bpms and correctors. The FBCs communicate via fast fiber links to adjacent FBCs. TBT bpm data will allow flexibility to test different feedback algorithms such as the ability to perform local



JAC / 23 Feb 2016

Figure 2: FBC signal flow diagram starting with bpm data on the left to fast corrector setpoints on the right. Shown at the top of the figure are pictures of the new hardware including: commercial BPM electronics (LB+) available from Instrumentation Technologies, the FBC CommAgility AMC-V7-2C6678 microTCA board and the CMPSI-2 which uses a Xilinx Zinq FPGA used to convert corrector setpoints at 22.6 kHz to the existing CMPSI interface for the APS fast corrector power supplies.

fast correction (using only local TBT bpm data is used to compute local fast corrector setpoints) before the full bpm vector is available to each FBC for full correction of the orbit. Other FBC star-type architectures for the system are also being considered where TBT bpm data transfer latency reduction is a primary goal.

CLOSED-LOOP BANDWIDTH AND RMS MOTION MEASUREMENTS

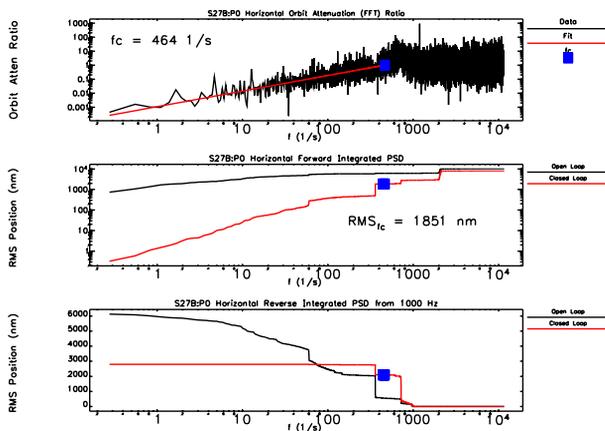


Figure 3: Orbit attenuation and closed-loop bandwidth plot for S27B:P0 (upstream ID P0 bpm). Top plot: Orbit attenuation showing closed-loop bandwidth cutoff frequency of 464 Hz. Middle plot: forward integrated PSD. Bottom plot: reverse integrated PSD starting at 1000 Hz. The closed-loop bandwidth shown in the figure did not change when we tested notch filtering and anti-alias LP filtering in the LB+.

Figure 3 shows the results of the closed-loop bandwidth test as measured at the S27B:P0 bpm (the bpm upstream of the sector 27 ID). The top plot shows the orbit attenuation as a function of frequency as the ratio of the FFT of the data closed-loop vs open-loop (approximately 5 seconds of data at 22.6 kHz sampling rate was taken to generate the plots). One clearly sees that near DC three orders of magnitude of attenuation (60 dB) is achieved. The curve crosses unity at a cutoff frequency of approximately $f_c = 464$ Hz indicating the closed-loop bandwidth. This closed-loop bandwidth is a factor of 5 above that achieved by RTFB in the present machine. The middle plot shows the total rms (square-root of the forward-integrated PSD) motion of 1851 nm at the cutoff frequency compared to closed-loop. The bottom plot shows the square-root of the reverse-integrated PSD starting from 1000 Hz showing amplification of the line at 720 Hz and attenuation at 360 Hz. The data shown in fig. 3 were obtained using only proportional and integral control and no filtering. Frequency domain data closed-loop at the other three P0 bpm's was similar to that shown in fig. 3.

FAST CORRECTOR STEP RESPONSE MEASUREMENTS

The FBC was used to perform both closed and open-loop step response measurements by changing bpm or corrector setpoints in a single 22.6 kHz clock tick of $44.2 \mu s$. Comparing closed-loop step response for the 4x4-test and a similar configuration of 4 bpm's and 4 fast correctors configured for use by the operations RTFB system showed an increase in speed by a factor of 2.5 when using integral control only for each system. In addition, open-loop step response measurements of the fast correctors were obtained by using an

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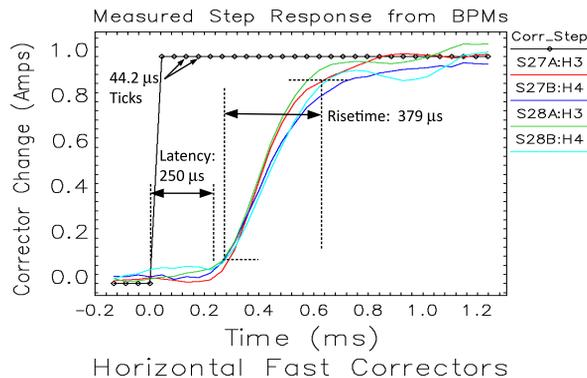


Figure 4: Open-loop horizontal fast corrector step response measurements inferred from P0 bpm step response data and the inverse response matrix.

inverse response matrix on bpm data when each fast corrector was stepped in turn. Figure 4 shows the results for the horizontal correctors. Vertical corrector step responses were similar. Note the plot shows the measured total latency in the system. The plot shows large $250 \mu\text{s}$ latency where no output from the fast corrector is observed. After this initial latency, the risetime from 10 to 90 % full value is $379 \mu\text{s}$.

Due to the large corrector latency, one would not expect to be able to achieve 1000 Hz closed-loop bandwidth since alone, $250 \mu\text{s}$ implies 90 degrees of the total phase margin at 1000 Hz. Other latencies in the system were tabulated and found to be mostly due to the fast corrector PS including setpoint data transmission, DAC and regulator delay and the 22.6 kHz clock tick. The LB+ was found to have negligible latency of $7 \mu\text{s}$ in its time-domain processing (TDC) mode (with no filtering) by comparison. We expect the large corrector latency to be much reduced for the MBA ring by careful design of PS controllers, fast corrector power supplies and magnets and vacuum chambers.

CONCLUSION

We have demonstrated first closed-loop test of new orbit feedback hardware at a 22.6 kHz update rate using four bpm's and four correctors configured as a "4x4" bump. We have demonstrated closed-loop orbit attenuation at the bpm's up to 464 Hz and step response improvement of a factor of 2.5 over the existing orbit feedback system. These

results will be used to optimize the system for the full integrated test this fall. In the integrated test, latencies in the PS will be minimized by using MBA upgrade PS hardware including a new PS corrector setpoint switch, controllers and fast corrector power supplies. In addition, a fully unified fast and slow corrector feedback algorithm will be used [3,4]. It is expected that ultimately the limiting factor to achieving the 1000 Hz closed-loop bandwidth will be the fast corrector magnet and vacuum chamber which has been measured to have a 3dB bandwidth of approximately 750 Hz. In addition, notch filtering for LB+ switching transients and anti-alias filtering will be added to the TBT data to eliminate aliased and switching transient signals. Additional closed-loop bandwidth testing will be done to assess the impact of additional latency due to filtering in the LB+ (or when as planned this filtering is moved to the FBC). Additional filtering latency will be offset to a large degree by using MBA upgrade fast corrector power supplies, controllers and setpoint transfer switch which should save at least $\approx 200 \mu\text{s}$.

Finally MMS and GRID diagnostics will be brought to bear on assessing how well the prototype FBC can meet the demanding long-term beam stability goals in table 1. The 4x4-test was an important stepping stone that was used to develop and test the first version of the prototype FBC and bpm hardware. In addition, software tools were developed for control room evaluation of FBC performance which will be upgraded and modified going forward into integrated feedback system testing in the fall of 2016.

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REFERENCES

- [1] R. Lill, N. Sereno and B. X. Yang, "BPM Stability Studies for the APSMBA Upgrade," proceedings of IBIC16.
- [2] B. X. Yang, et al. "Performance Test of the Next Generation X-Ray Beam Position Monitor System for the APS Upgrade," proceedings of IBIC16.
- [3] J. Carwardine, APS Upgrade Feedback Workshop, May, (2013).
- [4] N. S. Sereno, et al. "Beam Stability R&D for the APS MBA Upgrade," IPAC15, Richmond, Va. (2015).