DATA ACQUISITION SYSTEM FOR SUPERKEKB BEAM LOSS MONITORS

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Abstract

The monitoring of the beam loss distribution along the accelerator is important to prevent damage do delicate detectors around the collision point and to vacuum components such as collimators, and also to suppress the unnecessary irradiation of the accelerator elements. As it is not convenient to construct the readout system synchronized to fast timing such as beam injection, a new 64-ch ADC system which samples the output of the loss monitor signal integrator at a fairly fast rate and automatically keep the peak, mean, and minimum data has been developed. The performance of the ADC system is shown. The control system configuration which reads and resets the hardware interlock signal from the loss monitor integrator for the machine protection system (MPS) is also shown.

INTRODUCTION

The KEKB collider is now being upgraded to the SuperKEKB collider to obtain 40 times higher luminosity than that of KEKB. To realize such high luminosity, the beam energy is re-optimized to 7 GeV for KEKB-HER (HER, electron) and to 4 GeV for KEKB-LER (LER, positron). The maximum beam currents will be roughly doubled to 2.6A for HER, and to 3.6A for LER with much reduced beam emittances and x-y couplings. The beam size at the collision point will be further squeezed with a larger crossing angle. The first commissioning of the HER and the LER without BelleII detector installed (Phase-I operation) is planned to start early 2016. The main beam parameters of the SuperKEKB rings are shown in Table 1.

With the increase of the beam currents and reduction of the beam sizes, the stable beam loss rate along the rings is anticipated to increase greatly. The simulated beam loss rates with designed luminosity are 10 mA/s and 7.2 mA/s for LER and HER, respectively [1]. Those rates are 50 times higher than that of KEKB. In addition, the much smaller vertical beam size could easily cause disastrous damage to the vacuum components due to higher charge density. It is important to monitor the beam loss and to take necessary actions, such as stopping injection or requesting a beam abort before causing disastrous accidents.

For the main rings (HER and LER), we will use a similar configuration for the beam loss monitor system to that used at the KEKB accelerator [2, 3]. It consists of air ion chambers (ICs) and PIN photo-diodes (PINs) [4]. The lengths of the ICs are 5 m and they are distributed roughly every 30 m around the ring, typically near the focusing sextupole magnets (SFs). They are fixed on the cable rack near the outer wall of the accelerator tunnel where the direct distance from the nearest ring is about 2 m, and about 1 m above the medium plane of the rings. For the new positron damping ring (DR) [5] which will start beam commissioning around late FY2016, we plan to install ICs with lengths of 9 m around the ring.

Table1: Main Parameters of SuperKEKB Rings

	HER/LER	DR
Energy (GeV)	7/4	1.1
Circumference(m)	3016	135.5
Max. Beam current (A)	2.6/3.6	0.07
Number of bunches	2500	4
Single bunch current (mA)	1.04/1.44	18
Bunch separation (ns)	4	>98
Bunch length (mm)	5/6	6
RF frequency (MHz)	508.887	
Harmonic number (h)	5120	230
T. rad. damping time (ms)	58/43	11
L. rad. damping time (ms)	29/22	5.4
x-y coupling (%)	0.27/0.28	5
Natural emittance (nm)	3.2/4.6	42.5
Crossing Angle (mrad)	83	
Horiz. beam size at IP(μm)	10.2/7.75	
Vert. beam size at IP(nm)	59/59	
Beam-Beam Parameter	0.90/0.875	
Peak Luminosity ($cm^{-2}s^{-1}$)	8×10^{35}	
Max. injection rate (Hz)	50/50	50
Number of ICs	105	40
Number of PINs	101	optional

The PIN photo-diodes (PINs) are mainly placed near special vacuum components, such as beam collimators, to directly detect large and fast beam loss. Though the number of ICs is almost the same as that of KEKB, we

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will reinforce the PINs to observe fine, fast beam loss distributions.

Signals from the ICs and PINs are brought to five local control rooms around the rings. The outputs of the ICs are integrated and amplified using NIM 2W-size integrators which handle 8-channels of IC signals. The gain and the integration time constant can be selected from 1X, 10X or 100X, and 0.1 s, 0.3 s and 1 s, respectively. If a loss level exceeds a common pre-defined threshold, it initiates a beam abort request signal which is connected to the machine protection system (MPS).

The outputs from PINs are first integrated with a short time constant of 1 μs, then amplified with the selected gain (1X, 10X, 100X). One output of the amplifier is held with a peak hold circuit with the fixed time constant of 1 s. Other output is directly compared with the pre-defined threshold to initiate beam abort. The size of the module is NIM-2W, and it handles 8 channels of PIN signals. Typical beam abort levels at KEKB were 10 mA/ms and 10 mA/μs for ICs and PINs, respectively [4].

We have developed a 64-ch ADC system which samples the output of the loss monitor signal integrator modules at a fairly fast rate and automatically holds the peak, mean, minimum data. The details and the performance of the system are shown. The control system which reads and resets the hardware interlock signal from loss monitor integrators for the MPS are also shown.

READOUT SYSTEM

Original ADC used at KEKB.

In the original KEKB MR loss monitor systems, we used 16 bit, differential-input, 32-channel scanning VME ADC boards (Internix PVME-332) to read the individual output of the integrators. The original plan was to trigger the ADC synchronized to the injection timing with a reduced integration time constant of the integrator during beam injection, and then to trigger it at 1 Hz with a much longer integration time constant during storage. We prepared an external injection trigger module which mixed the injection timing of both LER and HER, and the control hardware and software to change the integration time constant automatically. Unfortunately, the system did not work so effectively due mainly to insufficient network resources (10Mbps) and a slow user interface due to computing power constraints at the time. Note that it is still not practical to directly handle the data at a high repetition rate such as 50 Hz because no one can utilize the data within 20 ms. We therefore gave up on changing the mode between injection and storage, and fixed the integration time constant to 1 s for the ICs.

New ADC Boards 18K14

There are several unsolved difficulties with the multi-board operation of the PVME-332s. Moreover, the boards have been discontinued and the company that fabricated the board have given up any kinds of support. We therefore have decided to develop a new VME-based ADC board which fulfils following specifications:

- 64-channel single-ended inputs compatible with PVME-332 (bipolar input, with the input range of ±10 V, and the signal input connectors).
- More than 14-bit resolution ADC with simultaneous sampling for all 64 channels.
- On board mathematic function which calculates the peak, the minimum and the mean of the data at a higher sampling frequency, such as 1 kSPS.
- Board to board synchronization function to synchronize the peak, minimum and mean calculation period.

Figure 1 shows the block diagram of the developed ADC board (Digitex 18K14A). It consists of 8, 16-bit, simultaneous sampling, analog-to-digital data acquisition systems (Analog Devices, AD7606) [6] with eight single-ended input channels. The maximum throughput rate of the AD7606 is 200 kSPS. It also includes oversampling function from 1 (no oversampling) to 64 times the timing clock with built-in antialiasing filter (a second-order Butterworth with -3dB frequency of 23 kHz when used with the input range of ±10 V). The SNR and THD is typically 95.5dB and -107dB, respectively. The DC accuracy is ±8 LSB, typically.

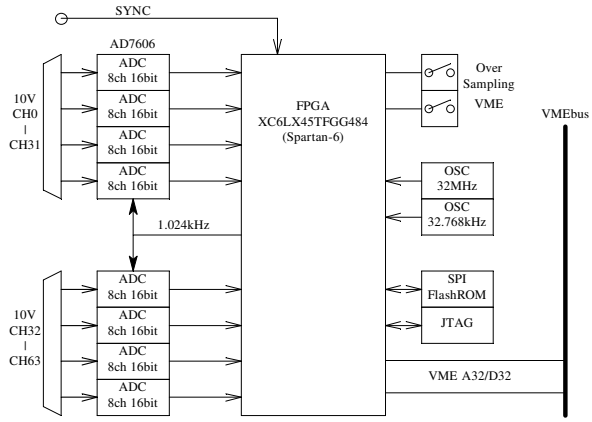

Figure 1: Block diagram of 16bit 64-ch., high-sampling rate ADC (Digitex 18k14A).

The board contains an FPGA (Spartan6 XC6SLX45) to read the AD7606s and to communicate with the VMEbus. It boots up from a SPI flash ROM during initialization of the VMEbus. The boot-up time is very short, typically less than 1 second, much shorter than the boot up time of VxWorks on the VMEbus controller. A J-TAG connector on the board is prepared to update the SPI flash ROM if needed. Timing clock for AD7606 is designed to be 1.024 kHz which is supplied from the FPGA (32.768 kHz / 32) to all AD7606s.

Data from AD7606s are captured and processed by the FPGA using a high speed serial interface. The average (simple average), peak-hold and minimum-hold function is done within the defined time period (1 s: 1024 samples, 0.5 s: 512 samples, 0.25 s: 256 samples). For monitor use, it also can report the raw AD data at the VME access

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which updates once per 1024 samples. The oversampling function of the AD7606s is also usable by setting a DIP switch on the board. We have no plan to use the oversampling function in normal operation, though.

The board supports A32 D32 supervisor (AM=0x0D) and non-supervisor (AM=0x09) access, and occupies 1024 bytes of memory space per board. The interrupter function after finishing mathematical calculations is also supported by the setting of the DIP switch on the board. As simple scan should be enough for most cases, we will not use the interrupter function, however. Figure 2 shows a photo of the 18K14A board installed in the VME64x bus at a test stand. On the front panel, it has two D-sub 37 connectors for analog input, one QLA input for synchronization between boards, three LEDs to show the FPGA status (program done or not), VME access and A/D status (busy, calculation done or standby). On the board ADC chips (AD7606s) are electrically shielded to suppress the noise around the VME. The lengths of the shielded signal cables from the loss monitor integrator to the ADC depends on the configuration of the system rack, typically around 5 m. We have developed EPICS [7] (R314.12.3) device support for VxWorks 6.8.3 on MVME5500 CPU.

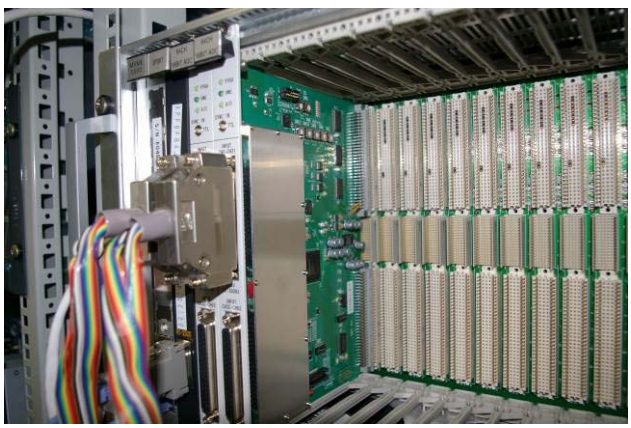

Figure 2: Picture of 18K14A 64-ch 16-bit VME ADC on the test stand.

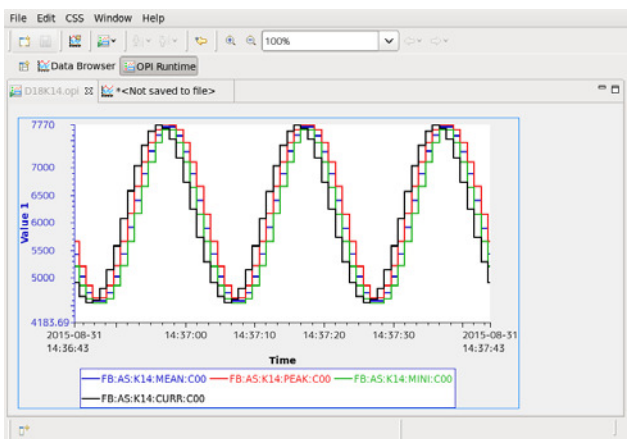

Figure 3: Digitized sinusoidal signal of 0.05 Hz. Mean (blue), Peak (red), Minimum (green) with monitor (black) shows expected behaviours.

The mathematical functions on the FPGA have been evaluated by injecting the known fast signals to 18K14A and checking the ADC outputs (peak, mean, minimum). Figure 3 shows an example of ADC outputs with 0.05Hz sinusoidal input. The scanning of the ADC output is 1 Hz and the calculation period is 1 s (1024 samples). The peak always stays on top and the minimum always stays on the bottom, while the mean stays between the peak and minimum. Note the monitor output shows a different phase from the calculated ones, because it bypasses the mathematical functions, roughly 1 second earlier than those signals.

By injecting a much higher frequency than 1 Hz, for example, a 991 Hz sinusoidal signal, the output shows completely different curves as shown in Fig. 4. All the curves (Peak, Mean and Minimum) show constant lines. The monitor curve shows the aliased remainder from 991 Hz of the function generator to 1 Hz of the 18K14A ADC clock. They also show good frequency response up to 1 kHz.

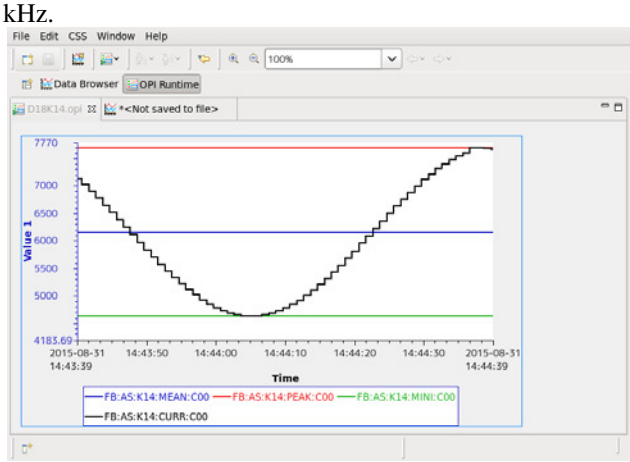

Figure 4: Digitized sinusoidal signal of 991 Hz. The monitor output (black) shows aliased curve to 1 Hz ADC clock.

Synchronization Between the ADC Boards

The ADC boards will be installed in the local control rooms around the rings. They boot up completely independently and process the data following their own system clock. Therefore, the beam loss data obtained with the EPICS scanning period of 1 Hz might be placed into earlier or later scanned data slots depending on the calculation period of the ADC boards. As the precise behaviour of a beam loss which triggers a beam abort is recorded directly using a multi-channel data logger with other useful information such as beam current, RF phase, RF voltage, a one second difference with the slow beam loss data is not a big problem. Nevertheless, the inconsistency might introduce unnecessary confusion during beam tuning especially during the injection tuning with a slow injection rate such as less than 1 Hz. We have implemented two synchronization mechanism among the distributed installed boards to reset the calculation period.

The first method is to inject a hardware synchronization signal to the board to reset the calculation period. On the front panel, we have prepared a timing

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injection port (TTL, rising edge). As in most local control rooms around the ring it is provided an event receiver which could transfer event timing with the timing accuracy of less than one revolution of the ring, 10 μs [8]. Unfortunately it has only four ports on the event receiver and most of the ports are already occupied with other needs.

Another method is to reset the calculation period with a software based signal. On the VME register, we have prepared reset command input which initiates the calculation timing to reset. This could be caused by the EPICS channel access command or by the EPICS sequencer initiated by the interrupt caused by the event system. Though the event system induced software timing might have been expected to have similar timing accuracy among the local control rooms, the arrival time of the EPICS channel access command should have much worse timing jitter.

Nevertheless we will at first evaluate the software timing synchronization scheme based on the EPICS channel access during the phase I operation of SuperKEKB. By observing the calculation time by the flashing timing of LED of 18K14As installed in one VME crate, the phase of the calculation period spread around 45 degree at peak to peak difference per day after the synchronization. It might be needed to re-synchronize the timing twice or more times per day. One such chance might be the period after beam abort—we anticipate having more than one beam abort per day even with normal, stable beam operation.

INTERLOCK MONITOR AND RESET SYSTEM

If the beam loss exceeds a pre-defined threshold, the integrator unit triggers the hardware beam abort request signal to the MPS [9]. The interlock status is latched on the integrator module until receiving signal reset (TTL, falling edge). When the beam abort due to loss monitor has happened, the operator will need to check the place where the loss exceed the threshold as soon as possible, then try to reset all the interlock status to restart beam operation soon. If recovery has been made without difficulty, the detailed beam and beam loss behaviour around the beam abort timing might be investigated during the injection time using data from fast loss logger, RF system data logger and oscilloscopes, and the Bunch Oscillation Recorder (BOR) [10].

During KEKB operation, we used an 80-bit VME-based general purpose I/O (Internix PVME-501) with open collector type 40-inputs/40-outputs daughter card. As in the case of original ADC boards, the board is also discontinued and no support is available now.

To replace and expand the I/O system for the loss monitor, we have selected Yokogawa FA-M3 systems [11] which contain two 32-bit TTL input units (F3XD32-5F) and one 32-bit TTL output unit (F3YD32-1T) with F3PU20-0S power unit on a 5-slot base unit (F3BU05-0D). Those TTL input and output modules are optically isolated. On the Linux-base CPU module (e-RT3), built-in EPICS system is working which enable us fairly easy access to the I/O modules by only defining the EPICS database parameter [12]. Figure 5 shows the installed FA-M3 system at KEKB-D7 local control room. As the signal connectors of those modules are not compatible with existing modules, and as the TTL output unit F3YD32-1T needs external +5V power to be injected to the collector of the photo-couplers, we have prepared a connector box of NIM-2W size. It translates the Dsub-25 connectors from interlock status output of loss monitor modules to Yokogawa A1451JD connectors for F3XD32-5Fs, an A1451JD connector from F3YD32-1T to 8-channels of QLA connectors to reset the interlock status. Driving power for the photo-coupler of the TTL output module is also supplied by the module.

Figure 5: Yokogawa FA-M3 system to read interlock status and to reset the latched interlock. From left, power supply unit, CPU unit, two 32-bit TLL input unit and 32-bit TTL output unit.

Installation of the new ADCs and FA-M3 I/O control system is now in progress. Operation testing of the system has been done at KEKB-D7 local control room and no difficulties have been found, as shown in Fig. 6.

Figure 6: Loss monitor station at KEKB-D7 under installation work.

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The graphical user interface (GUI) must be rewritten almost from scratch due to the addition of many new data (Peak, Mean, Minimum) and the addition of the new monitors. It will be prepared by the end of this year. The complete system test will be done by the end of this year, before the start of the Phase I operation of the SuperKEKB rings.

SUMMARY

We have designed and tested a new 64-ch VME ADC with intrinsic peak, minimum and mean calculation functions for SuperKEKB beam loss monitor systems. Data obtained in the test stand shows excellent performance as expected. The I/O control system to read and reset the interlock status of the loss monitors are also designed and tested and confirmed to be working as expected.

Though the current analog amplifier and integrator unit has long integration or peak-holding functions, the high speed sampling of the developed ADC board might not be so significant. Nevertheless, it might be possible to omit the analog integration circuit which will be installed in the future.

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