Institute of Modern Physics (IMP), Chinese Academy of Sciences

The Digital Controller for Power Supplies in HIAF

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Abstract

HIAF[1] (High Intensity heavy ion Accelerator Facili-ty) is a project proposed by IMP (Institute of Modern Physics, Chinese Academy of Sciences). This paper de-signs a digital controller for Bring in HIAF dipole power supplies system, which is several circuit boards consist of high precision ADC, optical fiber module, DDR3 SDRAM, Gigabit Ethernet module. It uses Cyclone V SX SoC FPGA, which integrated with dual-core ARM Cor-tex-A9 MP Core processor. This paper explains the hard-ware and software architecture of the controller and how can it improve power supplies performances. The FPGA finishes the PI regulating and PWM modulation. The ARM is responsible for data pre-setting, web service, database, and power supplies detection and protection management. At the end, this paper gives the output measurements when the controller is used in the proto-type, which verifies the rationality and reliability of the design.

Table. 1The Difference Between FPGAS

item	Cyclone Ⅴ	Cyclone Ⅱ
LE	68,416	110,000
Pins	499	422
Memory bits	5,662,720	1,152,000
DSP Blocks	112	/
Multiplier	224	150
Total PLL	15	4

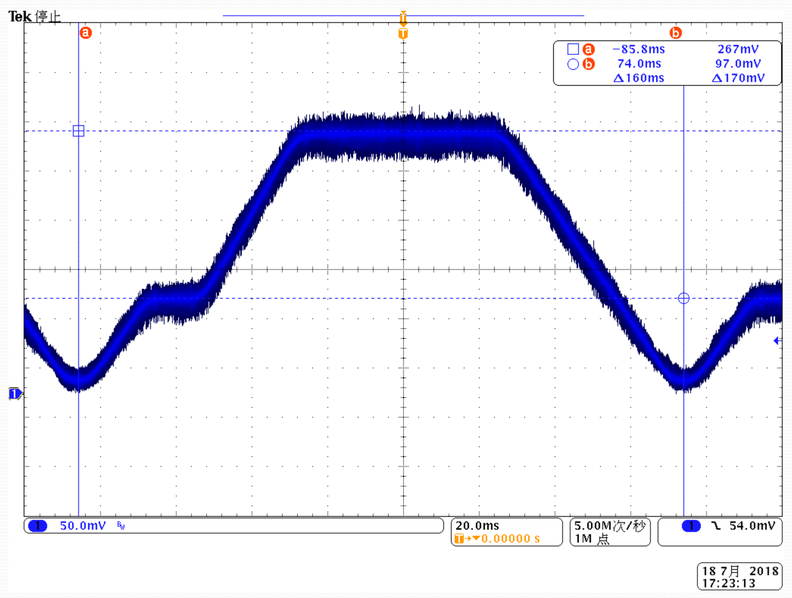

Figure. 4. Oscilloscope screenshots (Pulse Current output Direct Current output, Maximum current 20A).

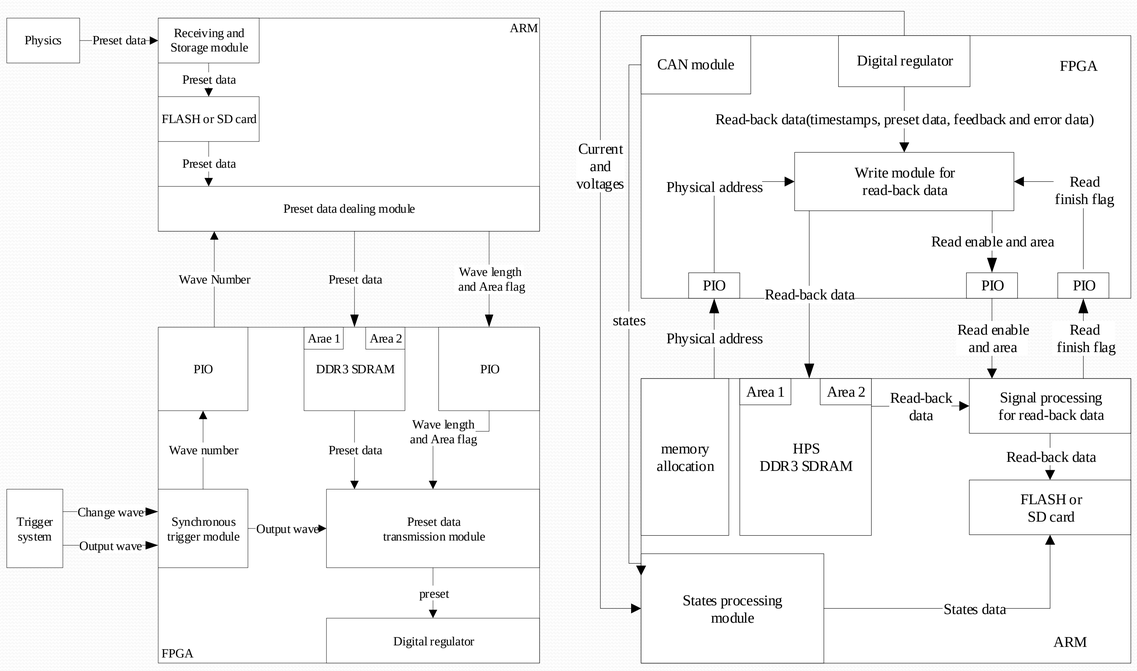

Figure. 1. Pre-set data transmission flow.

Figure. 2. Read-back data transmission flow.

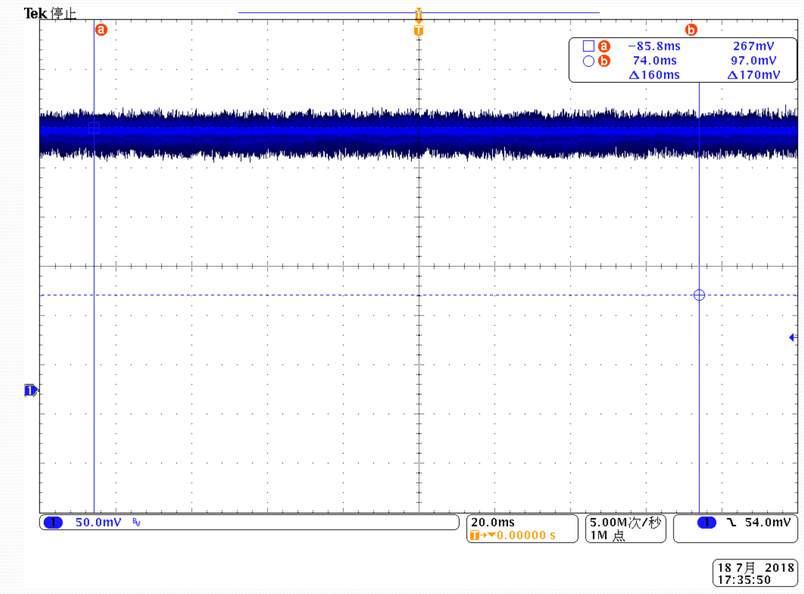

Figure. 5. Oscilloscope screenshots (Direct Current output 5A).

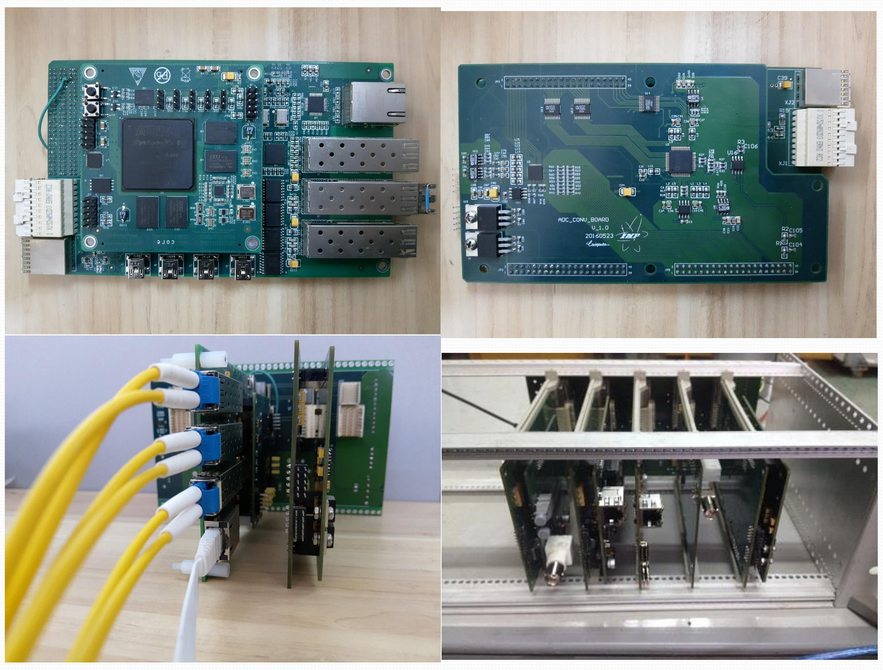

Figure. 3. The photos of the controllers.

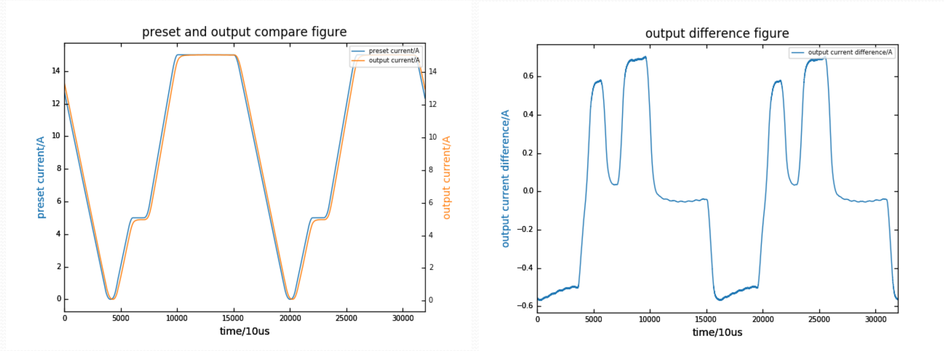

Figure. 6. The given and output current (the left one) and the error between given and output (the right one).

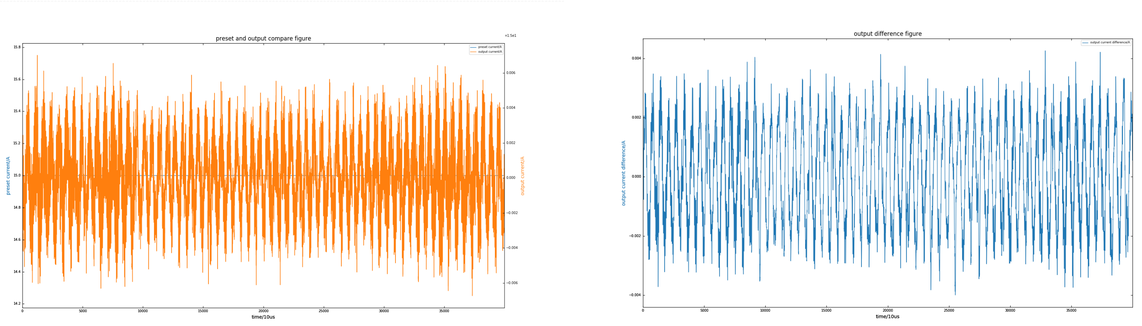

Figure. 7. The given and output current (the left one) and the error between given and output (the right one).

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