# DESIGN OF FAST PULSE GENERATOR FOR KICKER POWER SUPPLY IN HIAF*

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## ABSTRACT

Kicker power Supply is one of the key components in the injection and extraction system of HIAF (High Intensity Heavy Ion Accelerator Facility, the 12th five-year national big science project). The PFN-Marx generator technology based on solid-state switch IGBT will be applied to HIAF-Kicker power supply. Hundreds of controllable fast pulse signals are required for these IGBTs' control. The PFN-Marx generator has many requirements for their control signals, such as adjustable pulse-widths and time-delay. The maximum value of adjustment accuracy of the pulse-widths and delay among multiple control signals need to be 10ns. In this paper, a fast pulse generator circuit with adjustable pulse-widths and time-delay is designed for HIAF-Kicker power supply. This design is based on an emerging ARM-embedded FPGA. And the test results shown that the design can meet the required performance.

## THE SOLID-STATE PFN-MARX GENERATOR

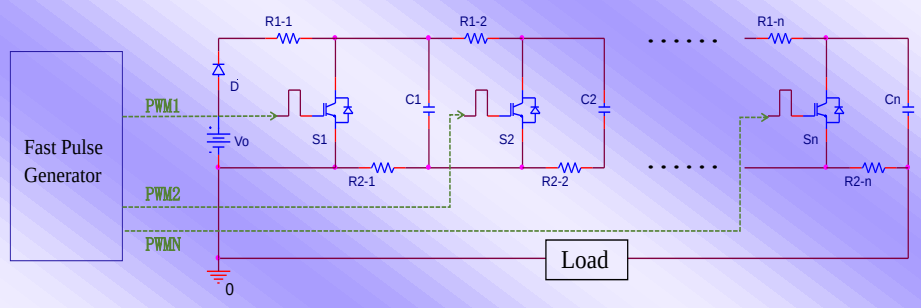


Figure 1 The schematic of the solid-state PFN-Marx generator.

HIAF-Kicker power supply will use a solid-state PFN-Marx structure as an energy storage system. Since the limited withstand voltage and current capability of a single solid-state switch IGBT, the quantity of IGBTs in solid-state FPN-Marx generator is very large. The control accuracy of FPN-Marx generator directly affects the beam injection efficiency. Therefore, the synchronous driving of multi-channel IGBT has become a technical difficulty problem that must be solved for HIAF-Kicker power supplies.

To reduce the time-delay caused by the dispersion of circuit parameters on FPN-Marx generator, people used to adjust switches on and off manually. This method is time consuming and laborious. The switches cannot to be debugged online while the power supply is in operating. To solve these problems, we designed a fast pulse generator based on Cyclone V chip, which integrates FPGA and a dual-core ARM Cortex-A9 MP core processor. In this design, ARM is mainly used to upload and download the control data. The fast pulse generator circuit is designed to generate hundreds of fast pulse control signals. For such signals，the time-delay and pulse-widths are adjustable and the adjustment accuracy is 10 ns. The high-accuracy digital control design provide synchronous drive signals for multi-channel IGBT of FPN-Marx generator, which has a significant advantage over manual adjustment.

## THE CONTROL SYSTEM STRUCTURE

The entire control system of HIAF is a network-based distributed control system. The information such as voltage parameters and pulse-widths need to be quickly sent to Kicker power supply Controllers through the network [5]. In order to make communication between the upper control system and the Kicker power supply controllers easier, we use the Cyclone V SX FPGA, which integrated with dual-core ARM Cortex-A9 MP Core processor.

The control system structure is showed in Figure 2. In this control structure, the delay and pulse-widths data are sent by the user interface via Ethernet. The ARM stores this information and distributes them to different registers on the FPGA side through the AXI bus bridge. After receiving these data, fast pulse generator circuit on FPGA generate hundreds of fast pulse control signals. Then we convert these output pulse signals into multi-channel optical signals. These optical signals are transmitted through the optical fiber and then converted into current signals by optical transceiver to the PFN-Marx generator.

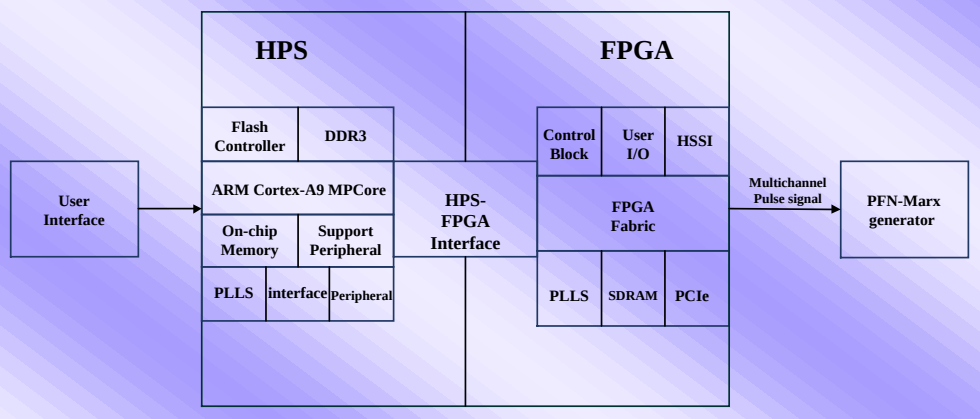


Figure 1: The control system structure.

## FPGA-BASED FAST PULSE GENERATOR

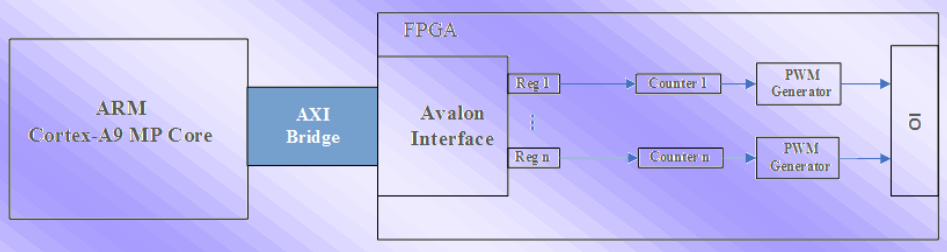


Figure 3: The fast pulse generation circuit hardware.

As shown in Figure 3, the programming contents on FPGA include: the fast pulse generation module and Avalon bus interface module. The fast pulse generation module contains multiple 16-bit counters. These counters read the delay and pulse-widths data for counting. These data are written in some 32-bit registers on FPGA by ARM through the AXI bus bridge. Among this data the upper 16 bits data represent the delay information and the lower 16 bits data represent the pulse-widths information. After counting process is completed the fast pulse generation circuit outputs the fast pulse.

For general external address space access, the CPU requires a user-defined interface control module. The Avalon bus interface module is designed according to the CPU read /write timing. Then the two modules are attached to the AXI bus bridge via the Qsys component. We use the PLL cores of FPGA to multiply the clocks to 100MHz respectively, so that the adjustment accuracy of the pulse-widths and delay to be 10ns.

## THE FAST PULSE OUTPUT SIGNALS

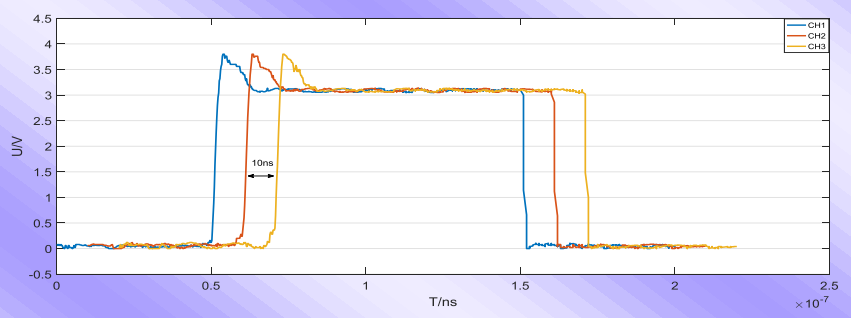


Figure 4 The multi-channel fast pulse output signals.

The design of fast pulse generator was used successfully to driving multi-channel IGBTs of PFN-Marx generator synchronously in HIAF. In this paper, we take three fast output pulses as an example. As shown in Figure 4, the delay among each channel signals is adjustable with a precision of 10 ns. The pulse-widths can also be adjusted according to the Kicker power supply's requirements with the same precision of 10 ns. All pulse-widths and delay information are sent through the network. The synchronization experiment show this controllable fast pulse output signals can meet the synchronous drive requirements of solid-state FPN-Marx generator in HIAF.

## REFERENCES

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