ISBN: 978-3-95450-203-5 doi:10.18429/JACoW-HIAT2018-MOPB04

DESIGN OF FAST PULSE GENERATOR FOR KICKER POWER SUPPLY IN HIAF

Y. Liu†[1], J. Gao[1], D.Q. Gao, J.B. Shang-guan, J. Zhao
Institute of Modern Physics, Chinese Academy of Sciences, 730000 Lanzhou, China
[1]also at University of Chinese Academy of Sciences, Beijing 100049, China

Abstract

Kicker power Supply is one of the key components in the injection and extraction system of HIAF (High Intensity Heavy Ion Accelerator Facility, the 12th five-year national big science project). The PFN-Marx generator technology based on solid-state switch IGBT will be applied to HIAF-Kicker power supply. Hundreds of fast pulse signals are required for these IGBTs' control. The PFN-Marx generator has many requirements for their control signals, such as adjustable pulse-widths and time-delay. The maximum value of adjustment accuracy of the pulse-widths and delay among multiple control signals need to be 10ns. In this paper, a fast pulse generator circuit with adjustable pulse-widths and time-delay is designed for HIAF-Kicker power supply. This design is based on an emerging ARM-embedded FPGA. And the test results shown that the design can meet the required performance.

INTRODUCTION

The High Intensity Heavy Ion Accelerator Facility (HIAF) is a new accelerator facility under design at the Institute of Modern Physics (IMP), Chinese Academy of Sciences [1]. The Kicker power supply is a device that provides excitation current for the pulsed magnet in the injection and extraction system of HIAF. HIAF-Kicker power supply will use a solid-state PFN-Marx structure as an energy storage system. Since the limited withstand voltage and current capability of a single solid-state switch IGBT, the quantity of IGBTs in solid-state FPN-Marx generator is very large. The control accuracy of FPN-Marx generator directly affects the beam injection efficiency. Therefore, the synchronous driving of multi-channel IGBT has become a technical difficulty problem that must be solved for HIAF-Kicker power supplies.

To reduce the time-delay caused by the dispersion of circuit parameters on FPN-Marx generator, people used to adjust switches on and off manually. This method is time consuming and laborious. The switches cannot to be debugged online while the power supply is in operating. To solve these problems, we designed a fast pulse generator based on Cyclone V chip, which integrates FPGA and a dual-core ARM Cortex-A9 MP core processor. In this design, ARM is mainly used to upload and download the control data. The fast pulse generator circuit is designed to generate hundreds of fast pulse control signals. For such signals, the time-delay and pulse-widths are adjustable and the adjustment accuracy is 10 ns. The high-accuracy digital control design provide synchronous drive signals for multi-channel IGBT of FPN-Marx generator, which has a significant advantage over manual adjustment.

THE SOLID-STATE PFN-MARX GENERATOR ON HIAF-KICKER

Compared with FPN (Pulse-Forming Network) and PFL (Pulse-Forming Line), PFN-Marx generator is based on solid-state switch IGBT, which has advantages of smaller size, easy to repair and more flexible to adjust pulse-widths and delay. After the energy storage process has been completed in PFN-Marx circuit, the square wave excitation current can be generated by the solid-state switch IGBT for the magnet load [2].

The work principle of the solid-state PFN-Marx generator is: the charging power supply charges the PFN in parallel through the charging resistor. After the charging process has been completed, the solid-state switches are turned on at the same time. The charging resistor acts as an isolator，and the PFNs in each stage are discharged serially. Each level of PFN modulates the waveform and finally the approximate square wave pulse waveform is obtained on the load. The schematic of the solid-state PFN-Marx generator is shown in Fig. 1.

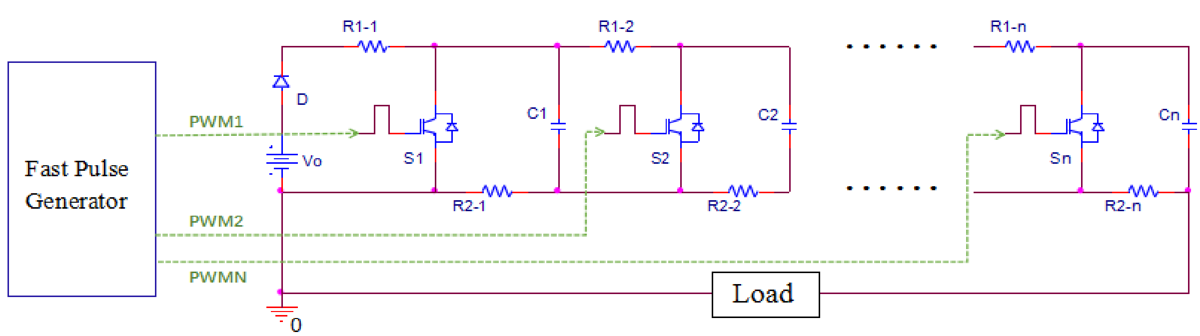

Figure 1: The schematic of the solid-state PFN-Marx generator.

† yanliu@impcas.ac.cn

ISBN: 978-3-95450-203-5 doi:10.18429/JACoW-HIAT2018-MOPB04

THE CONTROL SYSTEM STRUCTURE

The entire control system of HIAF is an Ethernet-based distributed control system. The information such as voltage parameters and pulse-widths need to be quickly sent to Kicker power supply controllers through the Ethernet [3]. In order to make communication easier between the upper control system and the Kicker power supply controllers, we use the Cyclone V SX FPGA, which integrated with dual-core ARM Cortex-A9 MP Core processor.

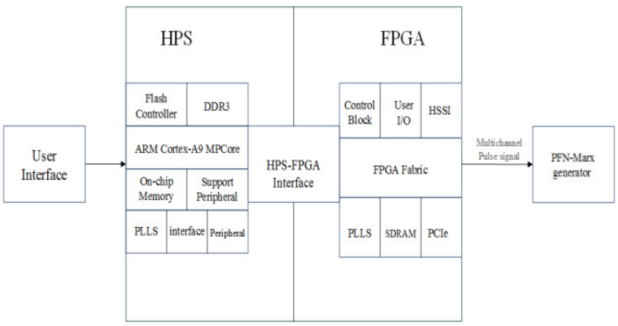

Figure 2: The control system structure.

The control system structure is showed in Fig. 2. In this control structure, the delay and pulse-widths data are sent by the user interface via Ethernet. The ARM stores this information and distributes them to different registers on the FPGA side through the AXI bus bridge. After receiving these data, fast pulse generator circuit on FPGA generate hundreds of fast pulse control signals. Then we convert these output pulse signals into multi-channel optical signals. These optical signals are transmitted through the optical fiber and then converted into current signals by optical transceiver to the PFN-Marx generator.

FPGA-BASED FAST PULSE GENERATOR

As shown in Fig. 3, the programming contents on FPGA include: the fast pulse generation module and Avalon bus interface module. The fast pulse generation module contains multiple 16-bit counters. These counters read the delay and pulse-widths data for counting. These data are written in some 32-bit registers on FPGA by ARM through the AXI bus bridge. Among this data the upper 16 bits data represent the delay information and the lower 16 bits data represent the pulse-widths information. After counting process is completed the fast pulse generation circuit outputs the fast pulse.

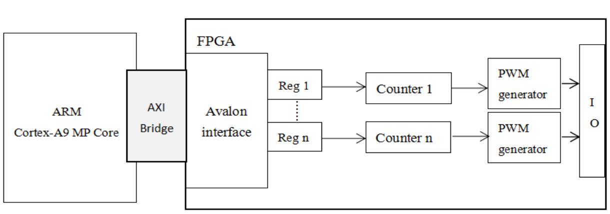

Figure 3: The fast pulse generator hardware structure.

For general external address space access, the CPU requires a user-defined interface control module. The Avalon bus interface module is designed according to the CPU read/write timing. Then the two modules are attached to the AXI bus bridge via the Qsys component. We use the PLL cores in FPGA to multiply the clocks to 100MHz, so that the adjustment accuracy of the pulse-widths and delay reaches 10ns.

THE FAST PULSE OUTPUT SIGNALS

The design of fast pulse generator was used successfully to driving multi-channel IGBTs of PFN-Marx generator synchronously for HIAF. In this paper, we take three fast output pulses as an example. As shown in Fig. 4, the delay among each channel signals is adjustable with a time precision of 10 ns. The pulse-widths can also be adjusted according to the Kicker power supply's requirements with the same precision of 10 ns. All pulse-widths and delay information are sent through the Ethernet. The synchronization experiment show this design can meet the synchronous drive requirements of solid-state FPN-Marx generator for HIAF.

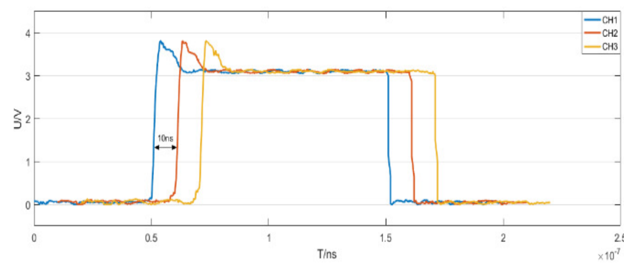

Figure 4: The multi-channel fast pulse output signals.

CONCLUSIONS

In this paper, a fast pulse generation circuit based on an ARM-embedded FPGA structure is designed to realize the synchronous driving for multi-channel IGBT of PFN-Marx generator for HIAF-Kicker. We use digital technology to accurately adjust the delay and pulse-widths of the drive pulses, effectively avoiding the shortage of manual adjustment. Moreover, the digital driving technology can improve the stability and synchronization of the injection and extraction system in HIAF. The following work will focus on integrating the fiber interfaces for hundreds of fast pulses into the controller of Kicker power supply systems and giving an optimized fan out scheme to reduce budget.

REFERENCES

[1] J.C. Yang, J.W. Xia, G.Q. Xiao, et al., "High Intensity heavy ion Accelerator Facility (HIAF) in China", Nuclear Instruments & Methods in Physics Research, 2013, 317(5), pp. 263-265.

[2] H. Li, H.J. Ryoo, J.S. Kim, et al., "Development of Rectangle-Pulse Marx Generator Based on PFN", IEEE Trans Plasma Sci, 2009, 37(1), pp. 190-194.

[3] Yu. Guo, Yan Wang, D. Zhou, W.F. Liu, et al. "Design of Control System for Kicker Magnet Power Supply", Atomic Energy Science and Technology, 2013, 47(6), pp. 1070-1073.