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DESIGN AND IMPLEMENTATION OF FAST MACHINE PROTECTION SYSTEM FOR CSNS

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Abstract

According to the design concept of high availability, high reliability and high maintainability, CSNS accelerator fast machine protection system (FPS) adopts the distributed architecture based on "high-performance chip (FPGA) + high-speed transmission link (Rocket I/O) + VME". We self-developed the main logic board with the function of reading and writing via VME, and which is the core and real-time to summary each interlocking signals, then determine and send out the protection action with accurately and stably. Simultaneously, in order to achieve interaction with each device flexible, we also self-customized a variety of interface boards. The permanent and instantaneous protection strategy was researched independently to meet the requirements of improving the efficiency of beam supply under the premise of ensuring operational safety. CSNS accelerator FPS has been put into operation for nearly six years stable and reliable until it is strict and systemic to test the function and performance on line, especially time-consuming, which is one of the important basic conditions for the efficient operation of CSNS accelerator.

INTRODUCTION

The Chinese Spallation Neutron Source (CSNS) is a large-scale scientific facility, which is mainly composed of an 80 MeV LINAC accelerator (LINAC), a 1.6 GeV Rapid Cycling Synchrotron (RCS), a target station, LINAC to Ring beam transport line (LRBT), RCS to target beam transport line (RTBT), multiple neutron scattering spectrometers and corresponding supporting facilities [1]. CSNS is the first pulsed neutron source facility in developing countries. It is expected to have positive effects in promoting the development of fundamental sciences and technology.

CSNS is based on accelerated high-energy protons, so if equipment failure or other reasons cause the high-energy protons to deviate from the normal orbit, the equipment along the beam, such as Drift Tube LINAC (DTL), may be suffered from graze or permanent damage by continuous beam bombardment because of the strong destructiveness protons. Therefore, it is essential to establish machine protection system to cut off the beam with high reliability in the shortest possible time, and execute the relevant progress in order time accurately. The CSNS accelerator fast machine protection system (FPS) is crucial to be need to meet the special functional requirements, which must have the characteristics of high stability, high reliability, and high speed under long-term operation. This article will introduce the requirements of system function, the design of architecture and protection strategy, and also the operation status.

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REQUIREMENT

According to the simulations and calculations carefully, if beam abnormality occurs during LINAC accelerator operation, the entire protection action should be completed within 10 µs to cut off the beam promptly [2], as shown in Figure 1. Generally, the response time of PLC-based slow protection system (SPS) is on the level of milli-seconds [3], which cannot meet the requirements of the CSNS LINNAC accelerator. In view of the overall the urgent and actual requirements of the CSNS accelerator, we decided to design and develop a fast machine protection system (FPS) based on the current high-speed digital electronic technology, and the key purpose of design is to achieve the response time of less than 10 µs.

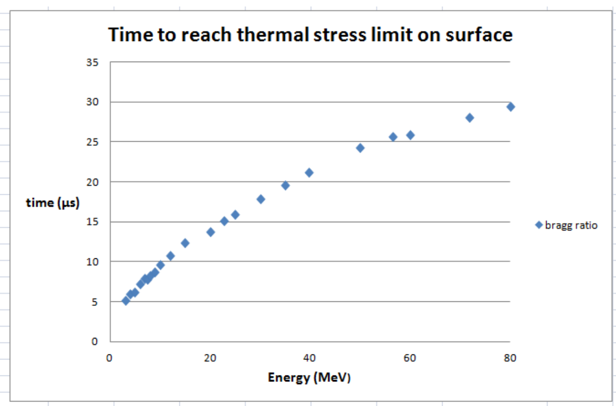

Figure 1: The relationship between the thermal stress limit in the material (copper) and the cumulative beam loss time. ① I=15 mA, $\sigma_x = \sigma_y = 0.2$ cm, J=62 J/gm (energy density); ② Un-chopped beam, 15 mA; ③ Beam size: 0.2 cm ×0.1 cm RMS; ④ Hitting the components directly.

ARCHITECTURE

According to CSNS accelerator physical design and beam research requirements, CSNS accelerator currently has a total of 6 beam targets [4], including: Ion Source (IS), LRBT Beam Dump (L-DUMP), LR Beam Dump (LRDUMP), Injection Beam Dump (I-DUMP), RTBT Beam Dump (R-DUMP) and target station, each beam target corresponds to the beam along the line and related equipment. Therefore, CSNS machine protection system needs to be able to timely

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and accurately update the connected machines and equipment when the beam target is switched. In addition, in order to protect the personal safety of the staff, CSNS accelerator has set up a total of 3 independent radiation protection areas, including: LINAC area, RCS area and target area, as shown in Figure 2.

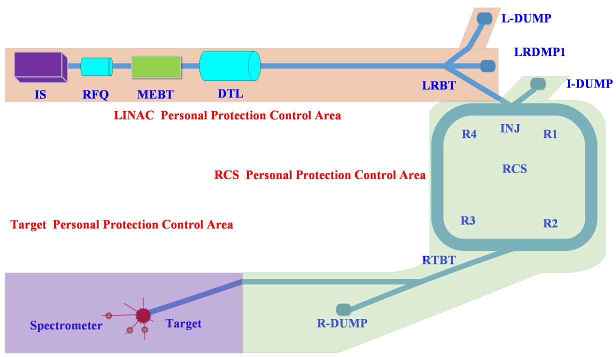

Figure 2: The schematic diagram of signal link.

In order to ensure the safe operation of the CSNS accelerator, we adopted the distributed architecture based on "Run Management System (RMS) + two slow machine protection systems based on PLC (SPS) + fast machine protection systems speed based on high-speed digital technology (FPS)" [5], the interaction of each system is shown in Figure 3, Both SPS and FPS are not only independently responsible for interacting with their respective devices signals, but also interlocking or unlocking with each other by the global reset signal from RMS, which hold a concurrent post that it is responsible for soft interlock, such as that the current beam of radiation frequency quadrupole (RFQ) is lower than pass rate. According to the characteristics of each interlocking signal and in-depth study, CSNS accelerator machine protection has the characteristics of high availability, high scalability and easy maintenance based on both mature commercial technology and the latest high-speed digital technology.

According to the above analysis, the main object of FPS is the DTLs with a small aperture in a vacuum along the beam line. In order to cut off the beam safely and reliably, the most effective method is to control in the early stage of beam rapidly. Therefore, the CSNS FPS mainly involves three systems: the ion source control system, the timing of the ion source extraction power supply and the power of RFQ. Table 1 is the table of input equipment and its distribution, including RFQ, DTL power, global beam loss, SPS and global reset and timing signals. Table 2 is the table of output equipment and its distribution, including the timing of the ion source extraction power supply, the power of RFQ, the beam gate of LINAC LLRF and SPS.

According to the equipment and distribution characteristics, and considering the actual needs of system installation, maintenance and expansion, FPS adopts the distributed architecture "high-performance FPGA chip + high-speed Rocket I/O transmission + VME", as shown Figure 4. "FPGA +

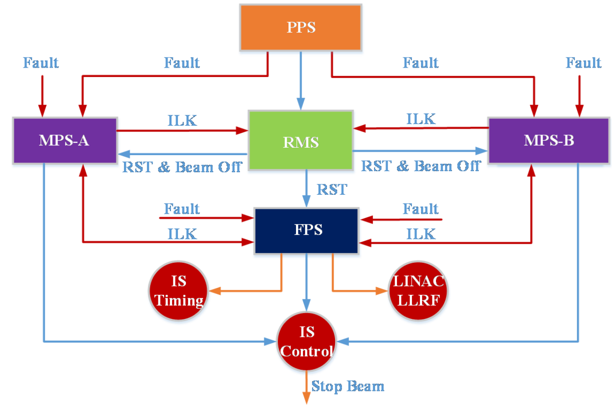

Figure 3: Layout of MPS.

Table 1: Input Signals for FPS

System Station	RF	PI	BI	MPS	RMS	Total
LINAC	8	120	12	4	2	146
LRBT	0	0	28	0	0	28
RCS	0	0	83	0	0	83
RTBT	0	0	50	0	0	50
Total	8	120	173	4	0	307

Rocket I/O" is responsible for signal aggregation, logic processing, signal fan-out, etc. VME is responsible for data readout, line OR for backplane signal, etc., which is designed though user-defined bus. In the light of the functional design, the architecture of FPS is divided into the third layers: collection, summary and preliminary processing, processing and execution. The layers are corresponding to the access substation, the summary sub-station and the executive master station respectively. Based on the principle of "minimizing the transmission delay and transmission quality of key inter-locking signals as much as possible", the executive master station and each summary sub-station are connected by multi-mode optical cables based on high-speed Rocket I/O transmission, and the same as each summary sub-station and each access sub-station.

There, the summary sub-station is illustrated as an example. The summary sub-station is responsible to summary and deal with interlocking signals preliminary and then sent interlock signals to executive master station. Figures 5a, 5b show the architecture of "multiple main logic boards + Rocket I/O + standard 21-slot VME chassis". The functions of the main logic boards are following: the main logic board of slot 1 is used for reading and writing the self-definition registers by standard VME bus; the main logic boards of other slots except slot 4 are used for receiving the data sent by the collection station based on high-performance FPGA and Rocket I/O. In order to achieving the purpose of " the main logic board can share interlock signals and reduce transmission delay", it is creative to design that the connection between each main logic board and the VME Backplane is bidirectional, so all main logic boards sent or get the in-

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Table 2: Output Signals for FPS

System Station	IS Control	IS Timing	RFQ Power	RF Beam Gate	MPS	Total
LINAC	2	1	1	8	4	16

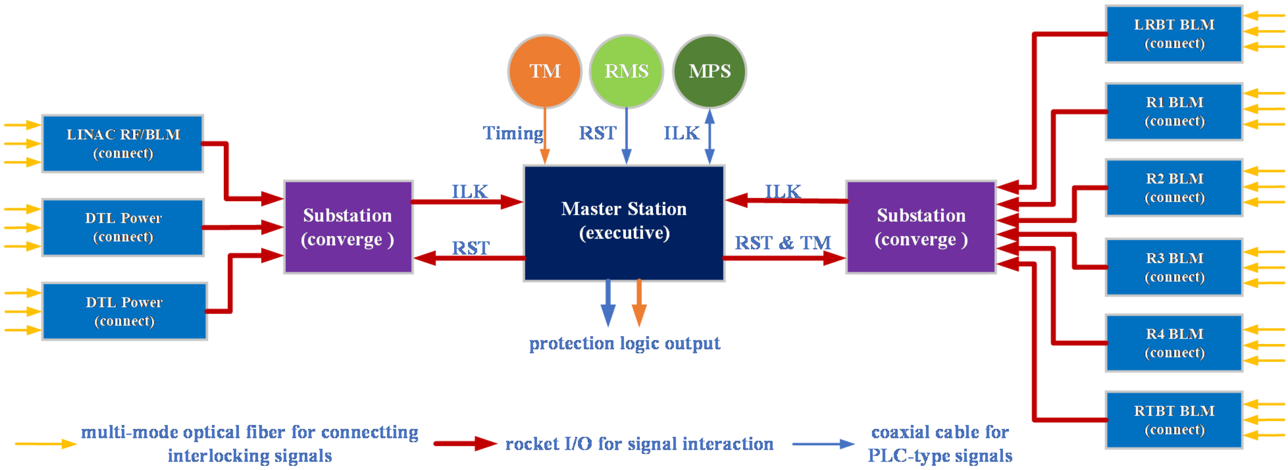

Figure 4: The schematic diagram of signal link.

terlock signals via VME Backplane respectively, which is used the open-collectors to realize the "wire-OR" logic, as shown in Figure 6. the main logic board of slot 4 is used to collect the real-time signals from VME Backplane and send to execution master.

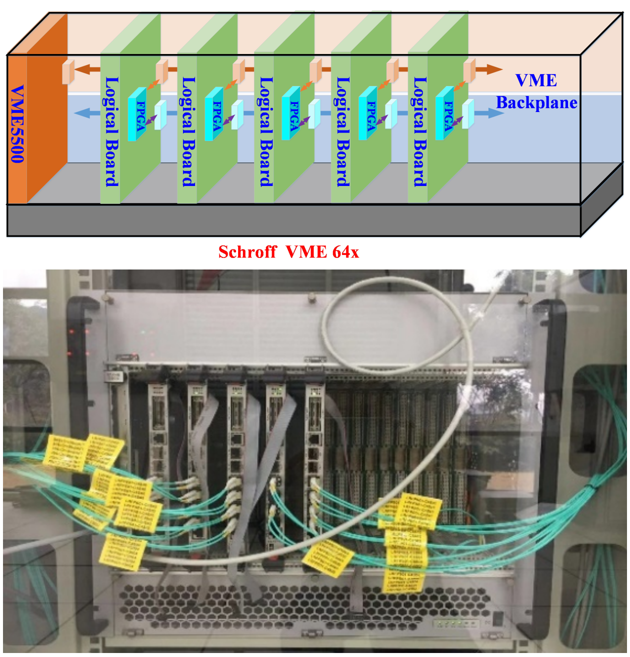

Figure 5: (Top) The schematic diagram of the summary sub-station, (Bottom) The physical map of the summary sub-station.

In order to ensure that the whole transmission link of each node is normal, a heartbeat signal, a width of 100 ns with 1 Hz, is generated at every sending terminal of the transmission link, and each link is used to transmit the heartbeat signal and real-time status signal simultaneously; the heartbeat signal is detected at the receiving terminal in real time, as shown is Figure 7. It is need to stop the beam immediately if an abnormal heartbeat signal is checked.

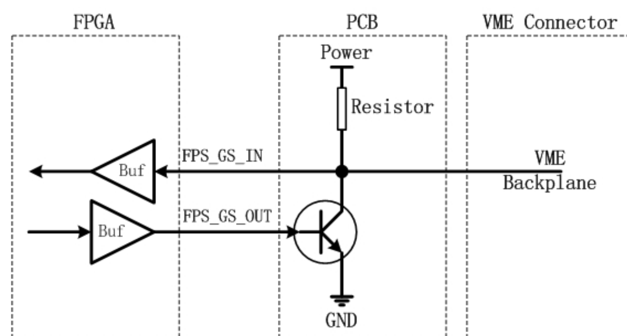

Figure 6: The schematic diagram of logic "OR".

PROTECTION STRATEGY

In order to formulate protection strategies, the characteristics of each interlocking signal should be in-depth recognized and analysed.

The signal of CSNS LINAC accelerator DTL power supply system during operation will be unique state, normal or abnormal. Therefore, if the FPS receives the ab-normal signal from DTL power supply or SPS, the faults is locked whatever the duration is short or long. Figure 8 is a schematic diagram of the signal processing for DTL power supply.

The signal of beam loss detector can be normal or abnormal, and the duration of the abnormal state is one beam cycle. Therefore, the FPS receives the abnormal signal from

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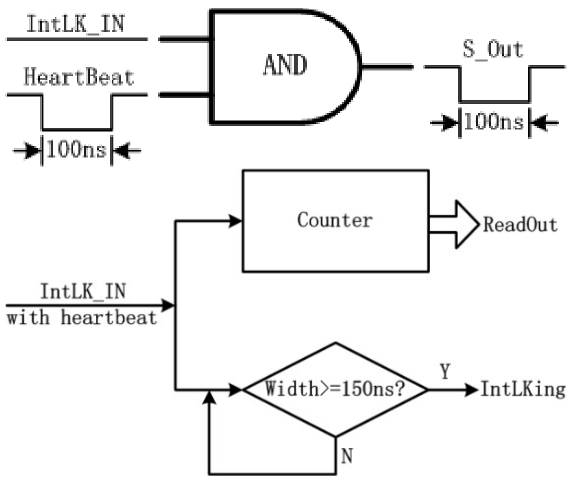

Figure 7: The logic function of heartbeat.

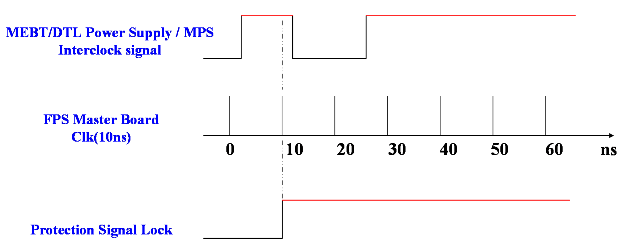

Figure 8: The schematic diagram of the signal processing for DTL power supply.

beam loss detector, it is instantaneous to stop beam. However, it is unacceptable if the abnormal signal is occurrence frequently. According to physics discussion, it is permanent if the number of instantaneous times within 10 seconds is six in LINAC or the number of in-stantaneous times within 5 seconds is two in RCS. Figure 9 is the schematic diagram of the signal processing for RCS BLM.

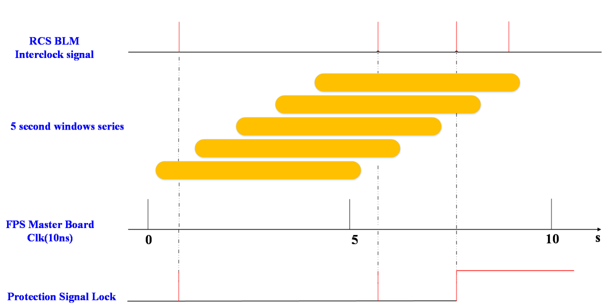

Figure 9: The schematic diagram for RCS BLM signal processing.

According to the characteristics of the interlock signals, the whole faults caused by equipment failures are divided into two categories: transient faults or permanent faults. In order to improve the operation efficiency of the CSNS accelerator, protection strategy is in-depth studied based on ensuring the safe operation. If the fault is transient, the beam should be cut off immediately, and the beam will be sync recovery automatically after the fault has passed, as shown in Figure 10; on the contrary, the beam should be cut off immediately, and the beam should be recovery manually because of the locked fault. It is indeed that the protection strategy can significantly improve the operation efficiency under ensuring equipment safety. Figure 11 shows the schematic diagram for implementing permanent protection function.

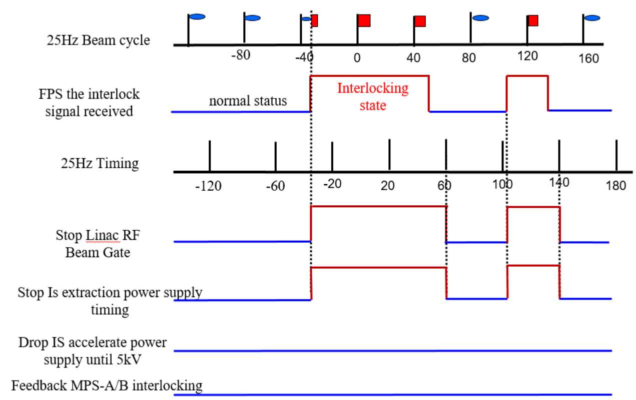

Figure 10: The schematic diagram for instantaneous protection logic.

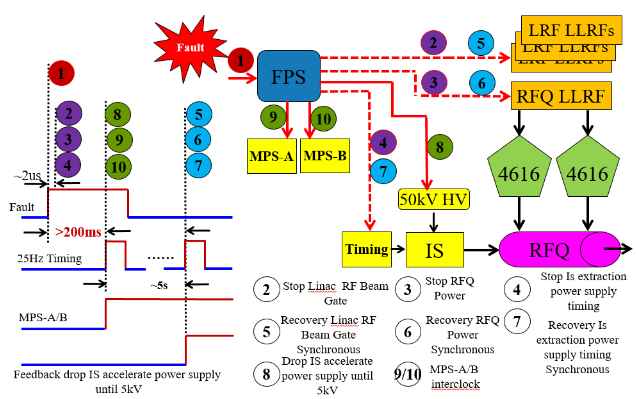

Figure 11: The schematic diagram for implementing permanent protection function.

TIME CONSUMING

FPS can not put into operation guaranty until the internal and joint testing with related equipment have been carried. The transmission delay of each node in the system has been tested rigorously, as shown in Figure 12; the time consumption for two fast execution shutdown targets is also carried out, as shown in Figure 13. The results of all tests show that the CSNS fast machine protection system can meet the current and subsequent upgrade needs of the accelerator.

- Figure 13 (Top): The progressing is that "get fault signal->judgment->sent out interlock signal->stop the timing of ion source extraction power supply", the total time is about 1.3 μs, which includes the delay 1.1 μs due to transmission.

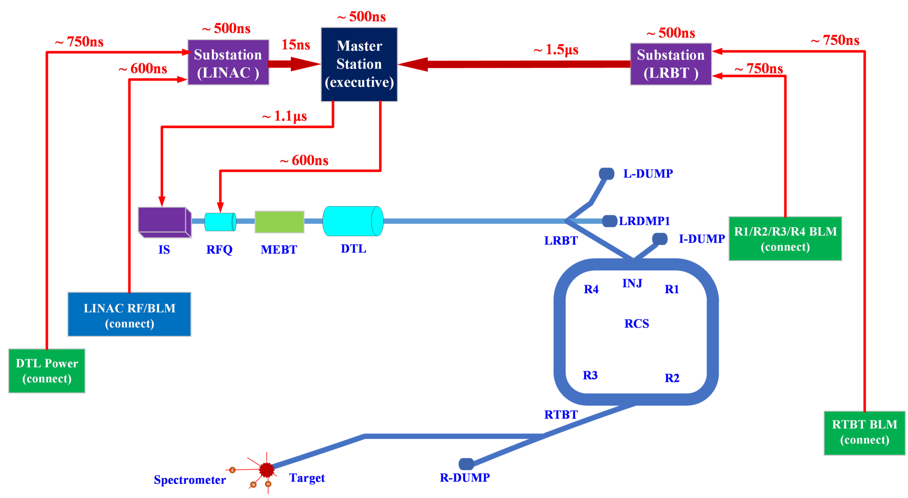

Figure 12: The response time of critical link.

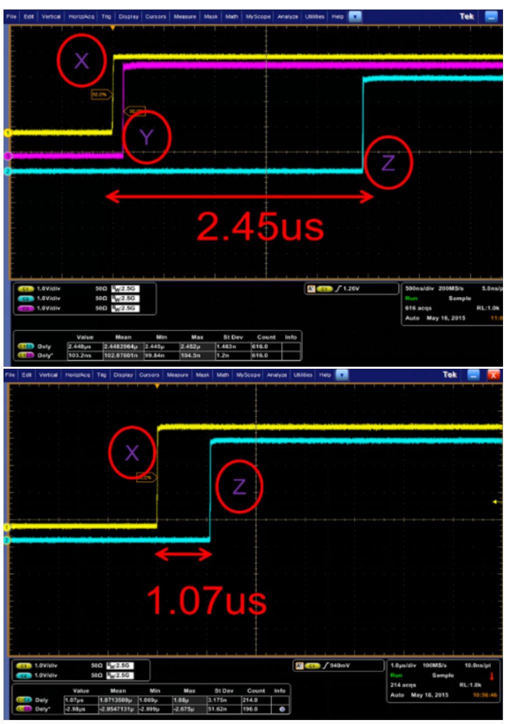

Figure 13: (Top) stop the timing of ion source extraction power supply, (Bottom) cut off the power of RFQ.

- Figure 13 (Bottom): The progressing is that “get fault signal->judgment->sent out interlock signal->cut off the power of RFQ”, the total time is about 1.3 μs, which includes the delay 600 ns due to transmission.

CONCLUSION

In order to cut off the beam with high reliability in the shortest possible time, and to maintain the relevant state in time to meet the operational safety, we the self-developed FPS for CSNS accelerator, which has under-gone detailed response time-consuming tests and careful traversal testing.

Since the beginning of installation, commissioning and gradual use in 2015, the FPS of CSNS has been operating stably for nearly six years, safe and reliable, and has been continuously optimized during adjustment and operation, such as adding the beam gate for each BLM and improving the design that all the beam loss signals of RCS are connect to FPS, whose enhance the robustness and high availability. It has been put into operation for nearly six years with stable and reliable, which is one of the important basic conditions for the efficient operation of CSNS accelerator.

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