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PROGRESS AND PLAN OF THE FAST PROTECTION SYSTEM IN THE RAON ACCELERATOR

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Abstract

In the RAON accelerator, beams generated by ion sources like ECR-IS or ISOL are accelerated to an energy of up to 200 MeV/u before reaching the laboratory target, and the beam power reaches up to about 400 kW at that moment. During transportation of such a beam, if beam loss occurs due to a device malfunction or a sudden change in beam condition, the accelerator can be severely damaged. Therefore, we have developed a machine protection system to protect the devices by minimizing the damage and to operate the accelerator in safe. As part of the RAON machine protection system, a FPGA-based fast protection system (FPS) that can protect devices within a few tens of microseconds after detecting the moment of beam loss has been developed since 2016. The development and test of the FPS prototype was successfully completed last year, and we are now preparing for mass production of the FPS. Here we will present the progress of the FPS development and the future plan for the FPS in the RAON accelerator.

INTRODUCTION

RAON accelerator produces beams with high energy and high power for a variety of scientific experiments [1]. However, unexpected factors can cause beam loss during delivery of these beams to the laboratories, which can lead to severe damage to the accelerator equipment. To minimize the damage, we has been developing a machine protection system (MPS). As shown in Fig. 1, the RAON MPS protects the accelerator by stopping the beam after collecting interlock signals from each device. This MPS consists of a fast protection system (FPS) and a slow interlock system (SIS) depending on the response time of the interlock signal. The field-programmable gate array (FPGA) based FPS responds to interlock signals within a few tens of microseconds and the programmable logic controller (PLC) based SIS within a few tens of milliseconds. There are also the run permit system (RPS) and the post-mortem system (PMS) for more stable and efficient operation of the MPS. The RPS is operated based on EPICS, and it is a system to determine the beam operation by checking information corresponding to machine mode and beam mode before starting the accelerator operation. The PMS is a system which identifies and analyzes the reason of the beam loss.

In the next chapters, we are going to explain the development status and the plan of the FPS, which plays the most important role in the MPS. To achieve faster processing speed, the FPS requires the FPGA based fabrication, and thus the prototype development was started from 2016 and completed by early 2017. After testing with individual devices, the beam test was successfully finished in fall of 2017, and the FPS product is currently being developed based on the prototype. The FPS product, which will be completed at the end of 2018, will be installed in the accelerator gallery after 2019, and the commissioning will be continued.

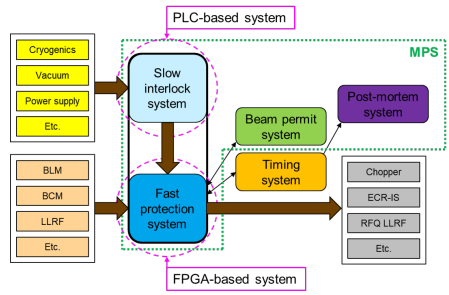

Figure 1: Layout of the RAON machine protection system, which consists of the fast protection system, the slow interlock system, the run permit system, and the post-mortem system.

FAST PROTECTION SYSTEM PROTOTYPE

The FPS prototype was made by using five ZC706 evaluation boards and consists of one mitigation node, three acquisition nodes, and one event generator as shown in Fig. 2. The acquisition node acts as a slave that collects interlock signals from each accelerator equipment and sends an interlock information to the mitigation node. The mitigation node acts as a master to send signals to the devices that stop the beam when it detects an interlock signal. In the prototype, the EPICS IOC is run on an external PC and the collected information from the mitigation node can be monitored and controlled with the CS-Studio (CSS).

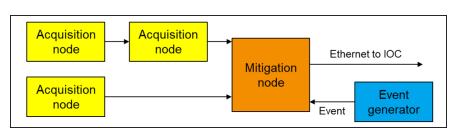

Figure 2: Block diagram of the fast protection system prototype. It consists of one mitigation node, three acquisition nodes, and one event generator.

The prototype was individually tested with the the SIS prototype, the AC current transformer, and so on. After that, the beam test was successfully carried out at the RISP SCL demo [2] by generating an interlock signal during actual beam operation and stopping the beam with the LEBT chop-

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per. Figure 3 shows the beam current before and after the FPS activation at the SCL demo. With several tests, the FPS prototype performance was verified. The details of the FPS prototype was presented at the ICABU 2017 workshop [3]. Based on the prototype results, we have been developing the FPS product using Xilinx zynq chip.

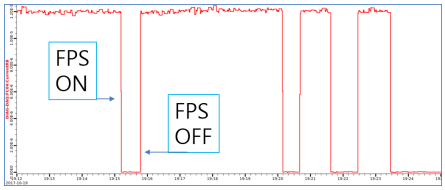

Figure 3: Beam test result of the fast protection system prototype at the RISP SCL demo.

DEVELOPMENT OF FAST PROTECTION SYSTEM

Prior to the mass production of the FPS, one chain consisting of one mitigation node and seven acquisition nodes as shown in Fig 4 are under developing. Each acquisition node can collect 64 interlock signals, and the collected information is finally transmitted to the mitigation node. The FPS based on the zynq chip can expect the fast signal processing by using a programmable logic (PL), and a processing system (PS) can drive an EPICS IOC with the petalinux system.

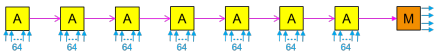

Figure 4: Layout of one chain in the FPS. It is composed of one mitigation node and seven acquisition nodes.

The configuration of the mitigation node is shown in Fig 5. The mitigation node is designed to transmit information from the acquisition nodes through the optical cable of 5 Gbps speed and send the signal to the chopper, RFQ LLRF etc. to stop the beam when an interlock signal is generated. Eight SFP+ transceivers are installed for the optical communication with acquisition nodes and an event generator, and a zynq XCZU9EG chip is used to implement the FPS function. Also Ethernet, USB, UART, and JTAG ports are supported for external interfaces. Twenty four SMA connectors are installed to transmit signals to the beam stopping devices.

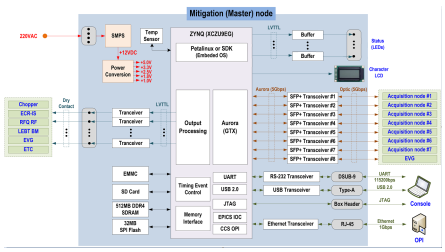

Figure 5: Configuration of the FPS mitigation node.

Unlike the mitigation node, the acquisition node does not require high specification, so the ZYNQ XC7Z100 chip is used. Four SFP+ transceivers are installed for the optical communications, and an interface terminal block is installed for collecting 64 signals from the accelerator equipment. It also supports Ethernet, USB, JTAG, and UART ports for external connections. The configuration of the acquisition node is shown in Fig 6.

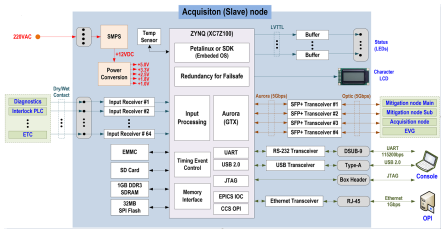

Figure 6: Configuration of the FPS acquisition node.

Along with the printed circuit board (PCB) fabrication of the FPS, the external hardware shapes are also being produced. Figure 7 and 8 show the geometries of the mitigation node and acquisition node up to the present. On the front panel, devices for external interfaces such as SFP+ transceivers, Ethernet port, JTAG port, etc. are inserted in all nodes. On the rear side, the mitigation node has 24 SMA ports for sending signals to the beam stopping devices, and the acquisition node has 64 input connectors for collecting external interlock signals.

Figure 7: Hardware shape of the FPS mitigation node.

Figure 8: Hardware shape of the FPS acquisition node.

Information for monitoring and managing the FPS can be found at the CSS operator interface (OPI) through the EPICS IOC running in the PL area. To to this, we are currently working on the production of the CSS OPIs. Figure 9 shows one of the FPS CSS OPIs. In addition to OPI for operating FPS, OPIs for operating RPS and PMS are also under development.

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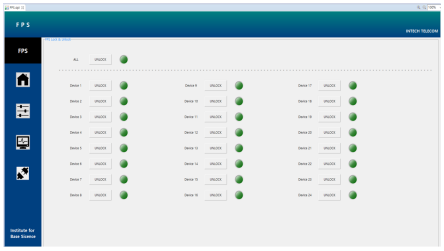

Figure 9: CSS OPI screen of the fast protection system.

PLAN OF FAST PROTECTION SYSTEM

The mitigation node and acquisition nodes under development will be installed in the control rack located in the accelerator gallery and will be operated together with other control devices such as a timing system and a SIS. As shown in Fig. 10, the mitigation node will be located in the injector section where the beam stopping devices are located, and the acquisition nodes will be installed along the long acceleration sections to collect interlock signals from peripheral devices. To support the beam operations of two low energy superconducting linac sections the mitigation nodes can be separately located and operated in each injector section.

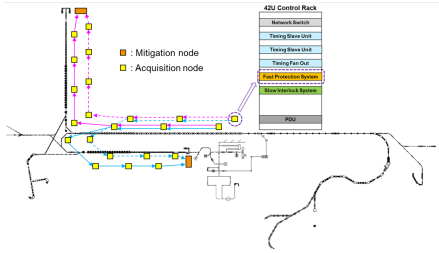

Figure 10: Layout of the RAON fast protection system.

For the beam operation from the low energy superconducting section (SCL3) to the high energy superconducting section (SCL2) in the RAON accelerator, the mitigation node consists of two units considering the backup. Also, the total of 49 acquisition nodes are installed, which are divided into 7 chains for efficient FPS operation, and more than 3,000 signals can be collected. Figure 11 shows the configuration of the FPS. The development of the one chain will be finished at the end of 2018, and then the remaining nodes will be made. The installation of the FPS in the accelerator gallery will be continued according to the beam commissioning schedule.

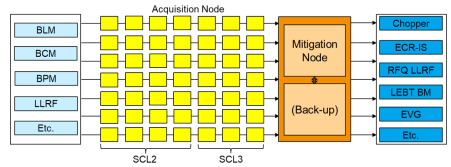

Figure 11: Architecture of the fast protection system from SCL3 to SCL2.

SUMMARY

We have described the development status of the FPS and its future plan. The FPS prototype had been developed, and the beam test was successfully carried out until the end of 2017. Based on this result, the Xilinx zynq based FPS products are under development. The hardware and software for the mitigation node and the acquisition node are under development, and this development is scheduled to be completed by the end of 2018. After the development, we are planning the commissioning of the FPS product after installing at the RAON accelerator based on the beam commissioning schedule.

ACKNOWLEDGEMENTS

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