Comparative Study of RF BPM Performance via Beam Measurements at NSLS-II

Advanced Beam Dynamics Workshop Future Light Source 2018

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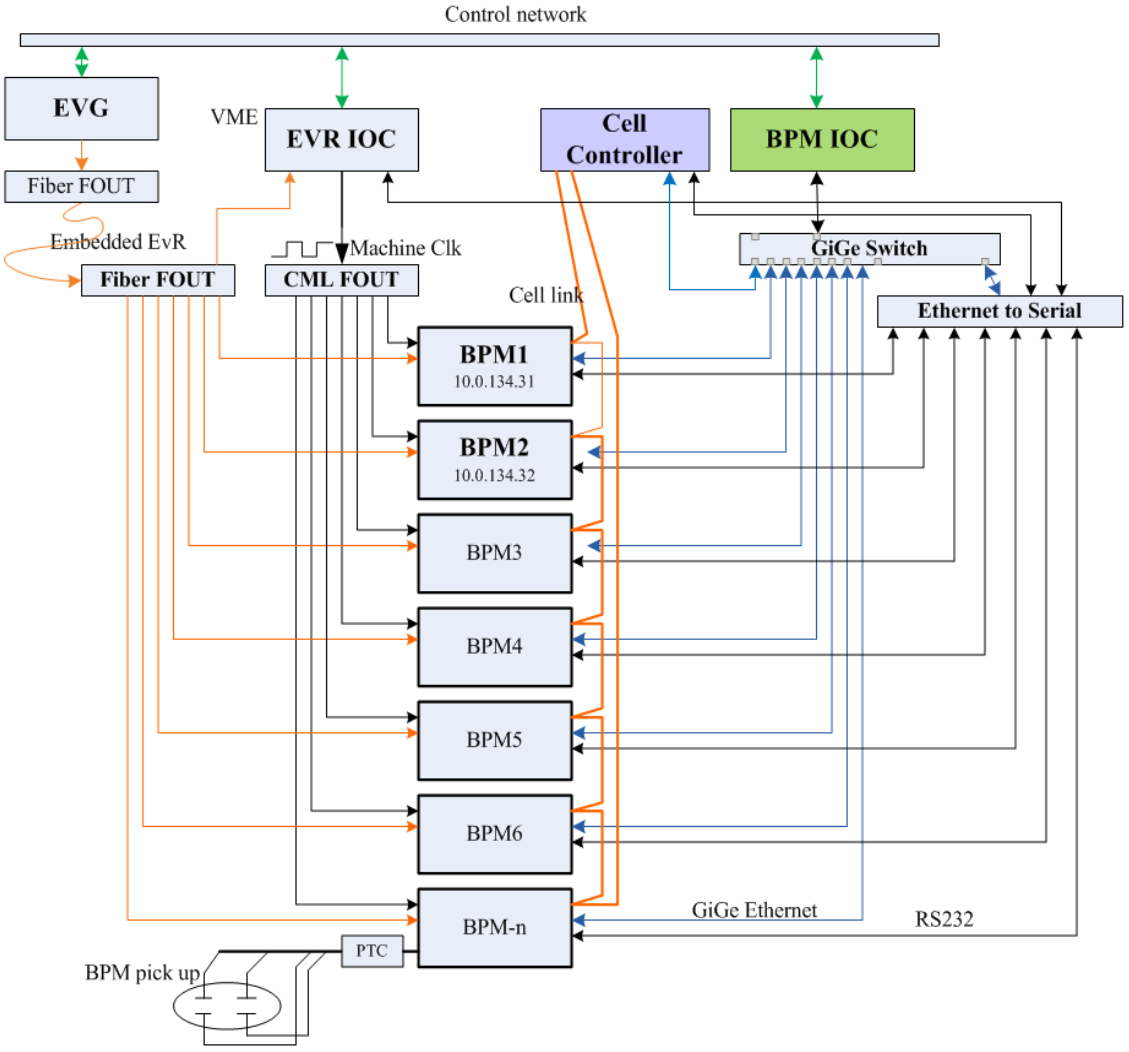
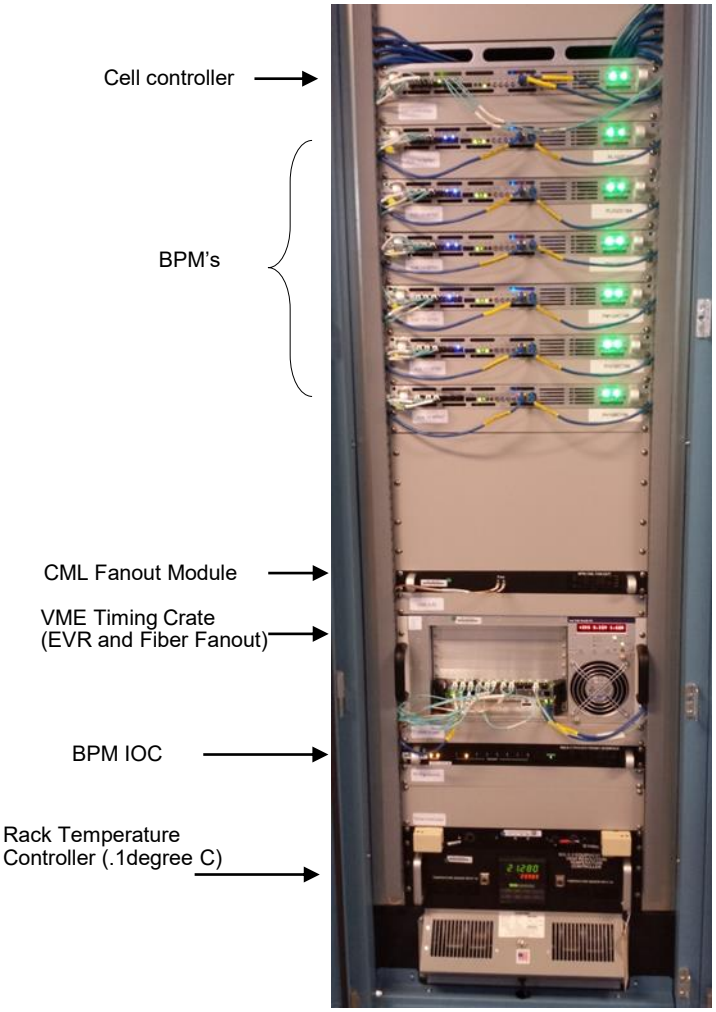
Outline

1. NSLS-II RFBPM overview
2. NSLS-II zBPM Specifications/Tests
3. iTech Libera Brilliance+ Specifications/Tests
4. zBPM / Brilliance+ Preliminary Performance Test
5. Performance Test Results Summary
6. Look Ahead: Next Generation AFE
7. X-BPM Specification/Tests

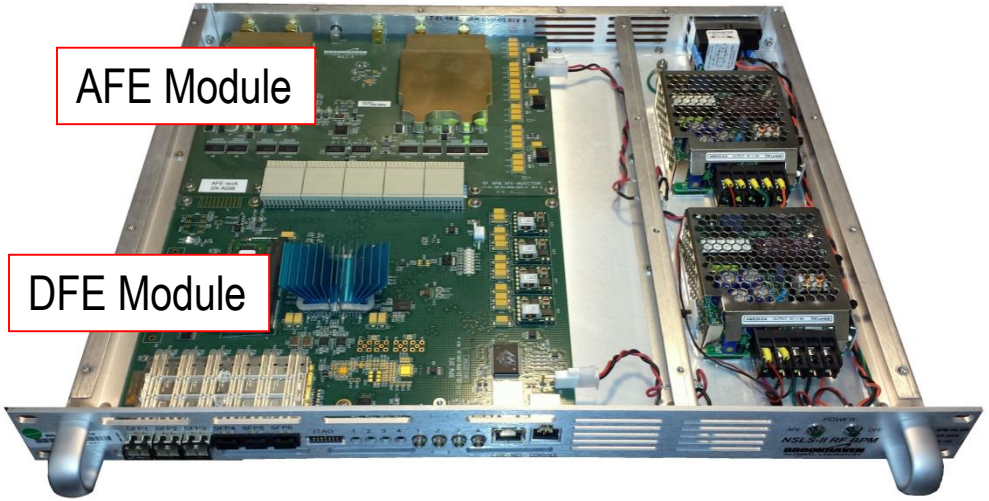
Typical BPM Cell Configuration





NSLS-II BPM Performance Specifications

- Original NSLS-II development
- Resolution specs:
  - ✓ 1 μm turn-by-turn (TbT)
  - ✓ 200 nm in 10 kHz (FA)
  - ✓ Long Term Stability 200nm/8hrs in 10Hz (SA)
  - ✓ Verified with beam
- TbT used for injection & kicked beam studies
- FA for fast orbit feedback & interlocks
- SA for orbit measurements, System Health
- No bunch-by-bunch capability (cannot resolve bunches within a turn)

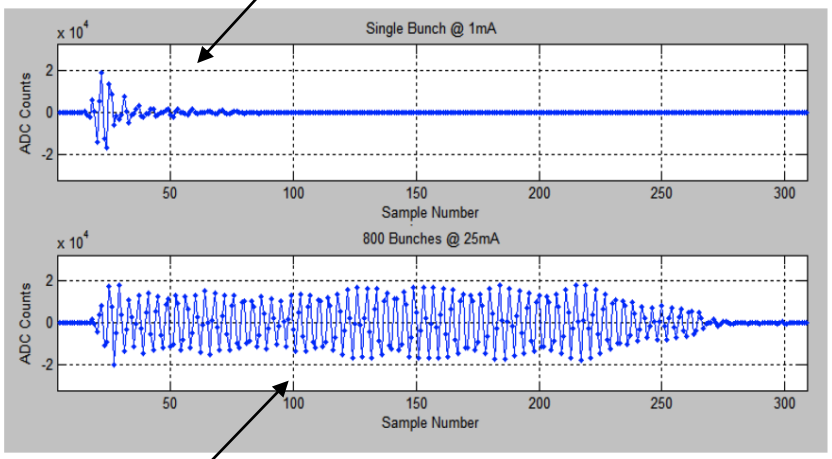


Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes or 32M samples raw ADC per channel simultaneously
TBT	On-demand	256Mbytes or 5M samples TbT (Frev=378KHz)
FOFB 10KHz	Streaming via SDI Link and On-demand	Streaming - X,Y,SUM ; For On-Demand: 256Mbytes or 5M samples FA (10KHz)
Slow Acquisition 10Hz	Streaming	DDR3 80hr Circular Buffer SA (10Hz)
System Health	Streaming 10Hz	DDR3 80hr circular buffer System Health; AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

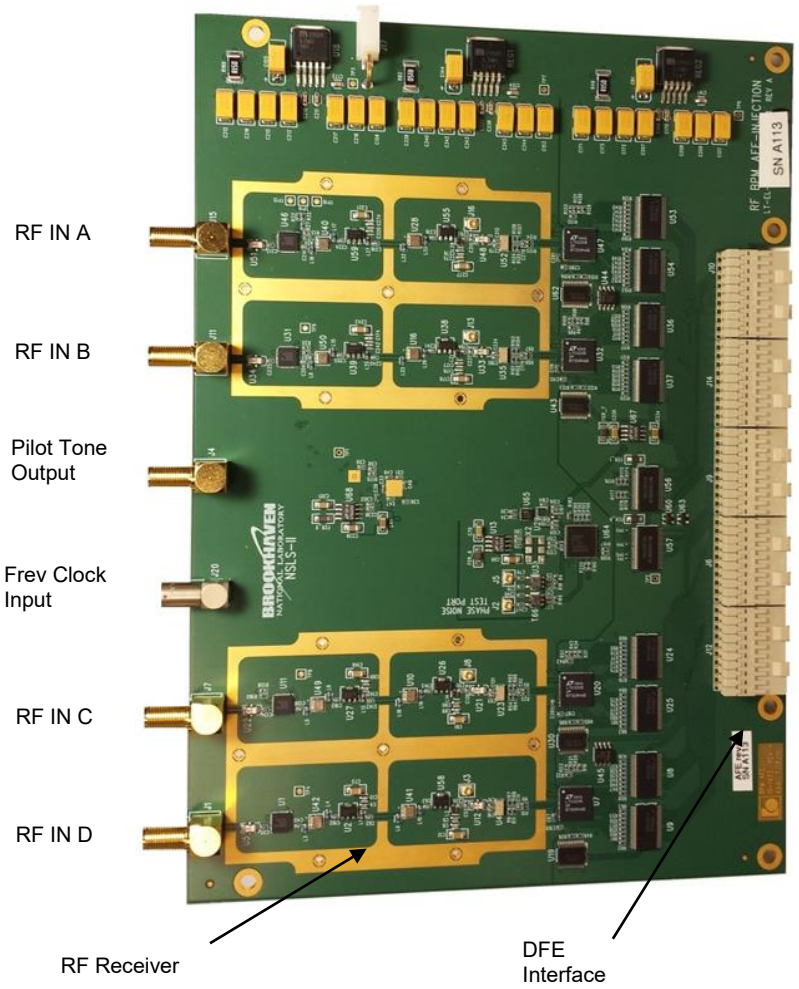
Analog Front End Board (AFE)

- Architecture is based on under-sampling the 500MHz impulse response of band-pass filter.
- Coherent signal processing – ADC clock is locked to Frev.
  - 310 ADC samples per turn

Single Bunch @ 1mA

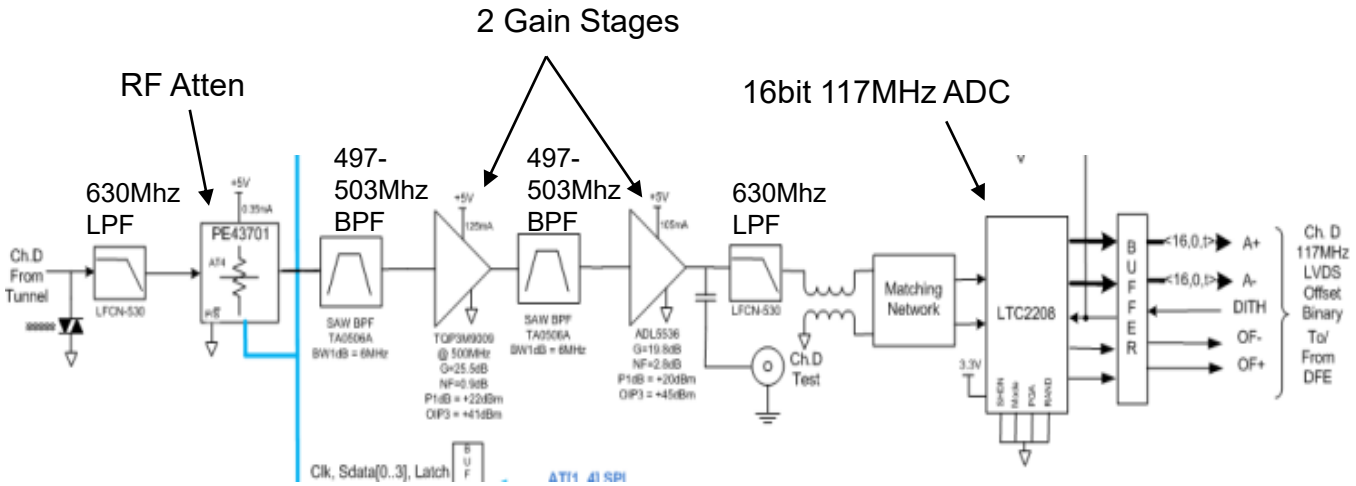


800 Bunches @ 25mA



AFE RF Channel Signal Chain

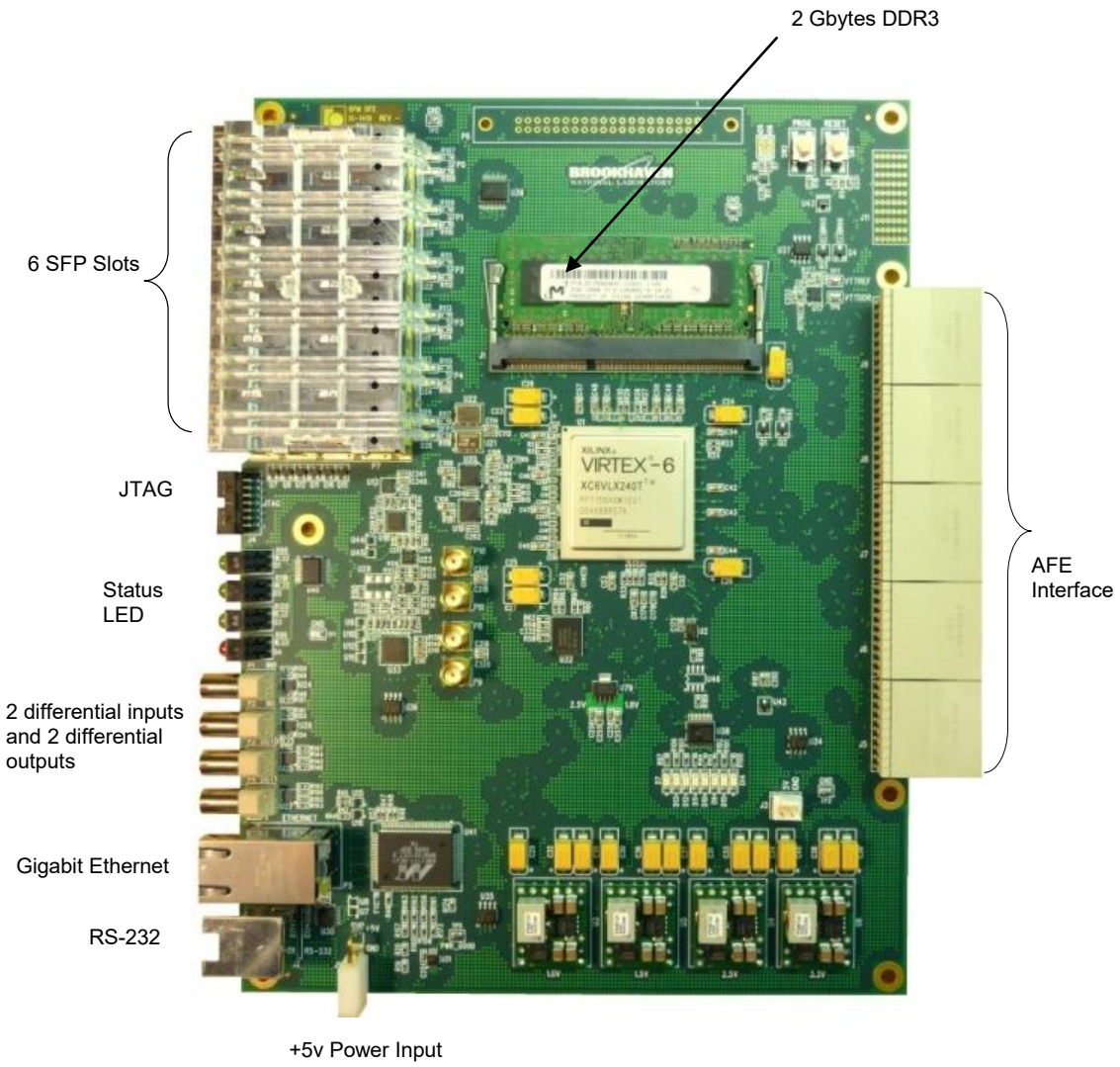
Single Channel Signal Chain



Digital Front End Board (DFE)

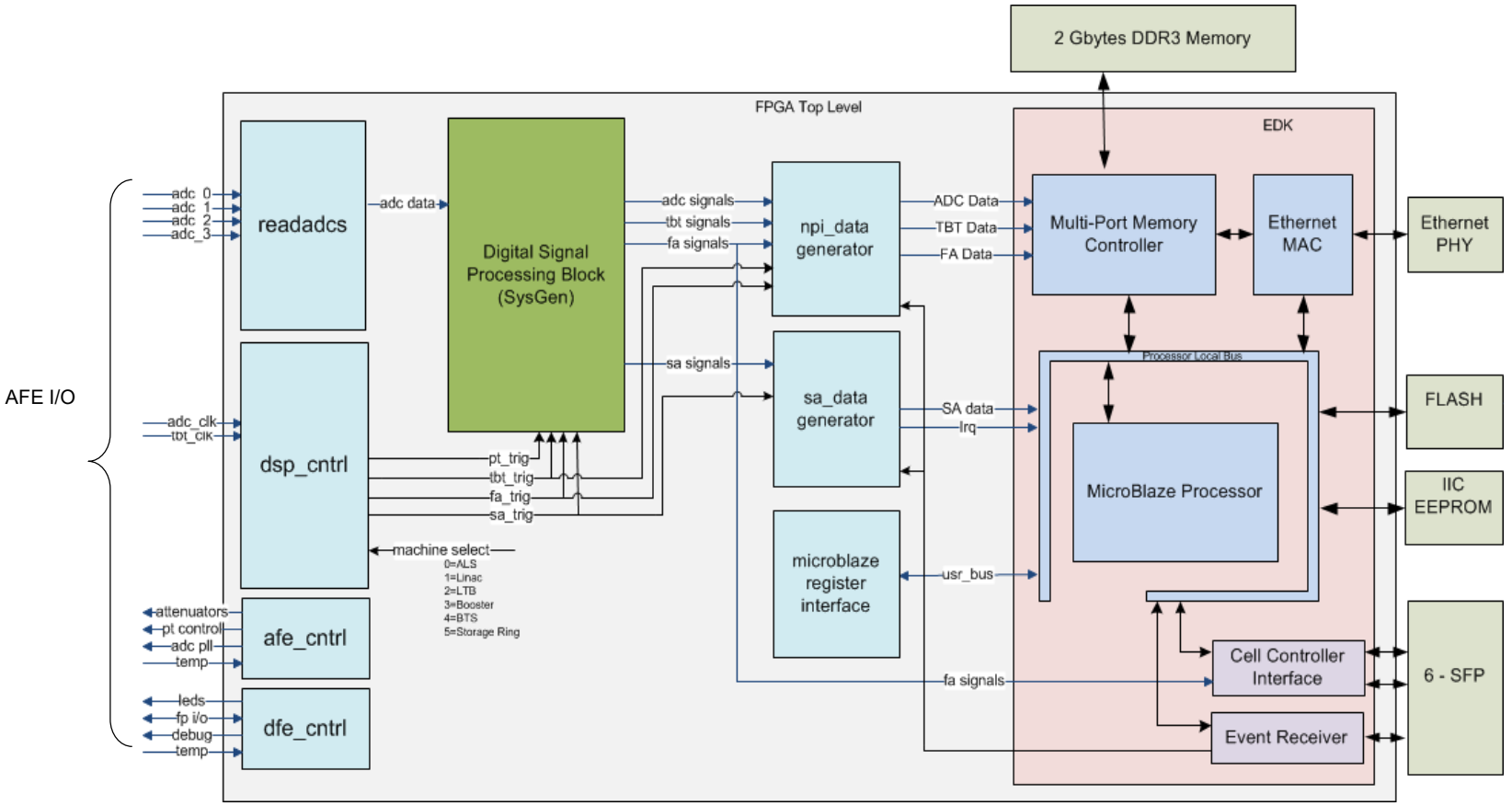
Features/Benefits:

- Xilinx Virtex-6 FPGA (LX240T)
- Embedded MicroBlaze soft core µP
  - Xilkernel OS and lwIP TCP/IP stack
- Gigabit Ethernet
- 2Gbyte DDR3 Memory (SO-DIMM Module)
  - Memory throughput = 6.4 GBytes/sec, which is fast enough to support streaming raw ADC data.
- Six 6.6Gbps SFP modules
  - Embedded Event Receiver
  - Fast Orbit Feedback
- 768 Hard Multipliers in FPGA fabric – Used for FIR filters, position calculations, etc.
- 1Gbit FLASH memory
- Also used as 'cell controller' processor for Fast Orbit Feedback



DFE FPGA Block

- FPGA implemented using a combination of VHDL, Verilog, System Generator (for DSP Block) and EDK for MicroBlaze processor
- 2 main data paths
  - Non Deterministic : ADC, TbT, FA, SA data to DDR memory and then to IOC via Microblaze ProcessorFPGA (Ethernet)
  - Deterministic : FA data to Cell Controller for FOFB and Active Interlock (Fiber Optic)



Motivation for BPM Upgrade to zDFE

Deficiencies of existing RF BPM DFE

- The soft-core MicroBlaze processor has limited performance and poor network performance (<20Mbit/sec).
- Xilkernel OS is a non-standard, Xilinx specific, bare-metal operating system with limited support.
- LwIP TCP/IP stack has some reliability issues.
- Software development requires special knowledge of Xilkernel OS features and therefore steep learning curve and difficult to maintain as opposed to standard OS such as Linux.

zDFE Improvements vs. Existing RFBPM DFE

- Hard dual-core ARM A9 processor provides >500Mbit/sec throughput. This is a 25x improvement over the existing RFBPM DFE performance.
- Runs standard Debian based Linux Operating System.
- Embedded IOC
- Software development is now standard user space applications similar to software development on a standard linux server.
- Programs compiled using standard gcc compiler.
- Long term maintainability and standard software development provide quick learning curve and allow developers easier access to maintain and upgrade software and features.
- Added FPGA resources.

zDFE BPM Performance Specifications

- zBPM Prototype
- Resolution specs:
  - ✓ 1 µm turn-by-turn (TbT)
  - ✓ 200 nm in 10 kHz (FA)
  - ✓ 200nm Long Term Stability /8hrs in 10Hz (SA)
  - ✓ Verified with beam
- TbT used for injection & kicked beam studies
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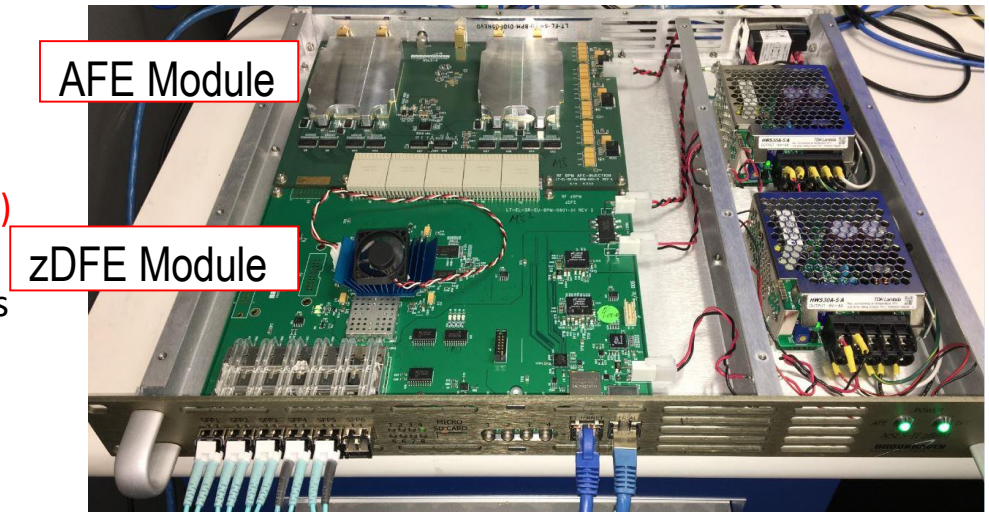
- SA for orbit measurements, System Health

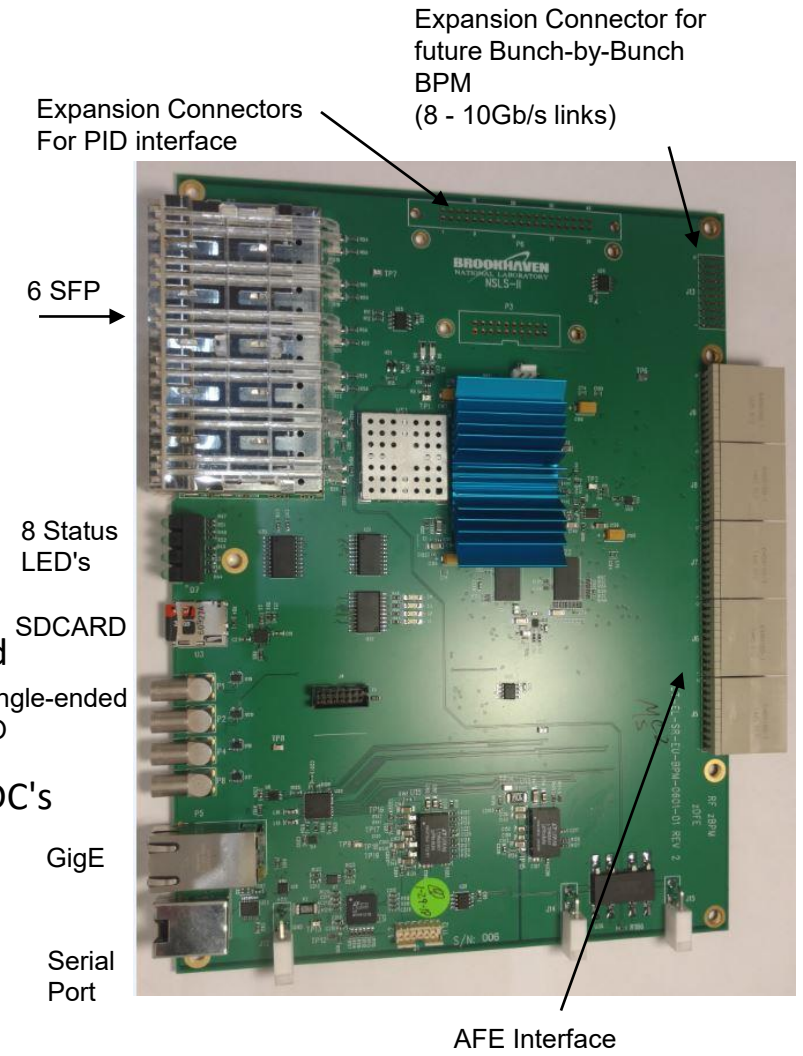


Data Type	Mode	Max Length
ADC Data	On-demand	100Mbytes or 12M samples raw ADC per channel simultaneously
TBT	On-demand	100Mbytes or 2M samples TbT (Frev=378KHz)
FOFB 10KHz	Streaming via SDI Link and On-demand	100Mbytes or 2M samples FA (10KHz)Streaming - X,Y,SUM ; On-Demand:
Slow Acquisition 10Hz	Streaming and On-demand	SD Card based 80hr circular buffer SA (10Hz)
System Health	Streaming	SD Card based 80hr circular buffer System Health; AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

Digital Front End Board (zDFE)

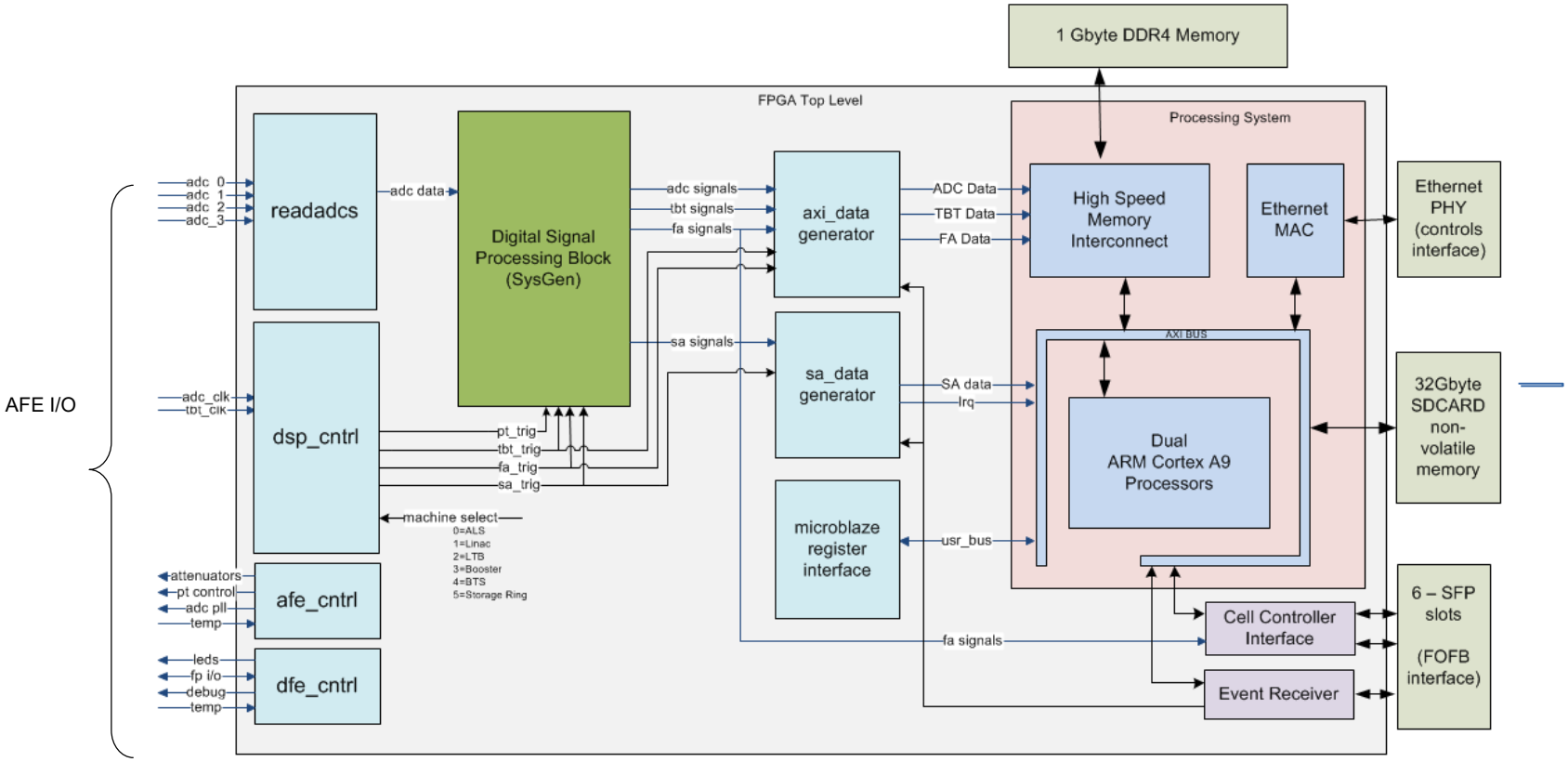
Features/Benefits:

- Faster processing and networking, 500Mbit/sec vs. 10Mbit/sec
- Hardware is backward compatible, use existing AFE and enclosure to minimize upgrade effort and cost
- Standardize to common DFE platform, supporting multiple sub-systems including: RFBPM, BbB-BPM, X-Ray BPM, Cell Controller for Fast Orbit Feed-Back
- Runs standard Debian based Linux Operating System.
- Software development is now standard user space applications similar to software development on a standard linux server.
- Support for Bunch-by-Bunch position calculation
- Integrated 10Gbps transceivers to interface to 500MSPS ADC's



zDFE FPGA Block

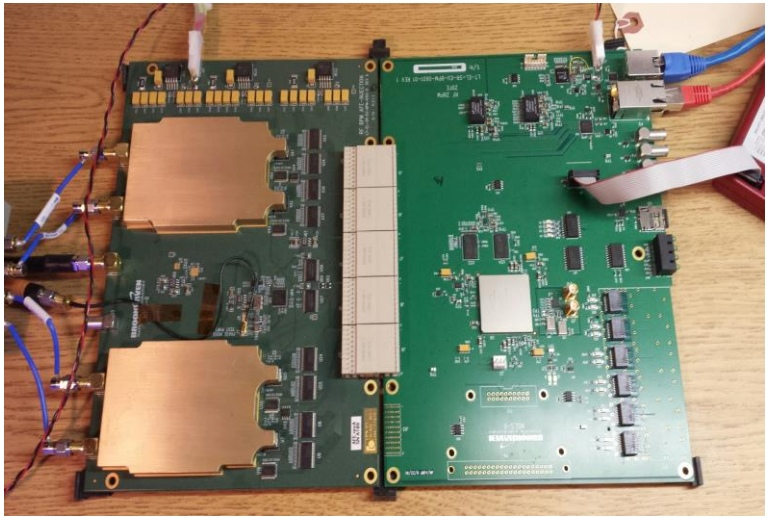
- FPGA implemented using a combination of VHDL, Verilog, System Generator (for DSP Block)
- 2 main data paths
  - Non Deterministic : ADC, TbT, FA, SA data to DDR memory and then to IOC via ARM A9 ProcessorFPGA (Ethernet)
  - Deterministic : FA data to Cell Controller for FOFB and Active Interlock (Fiber Optic)



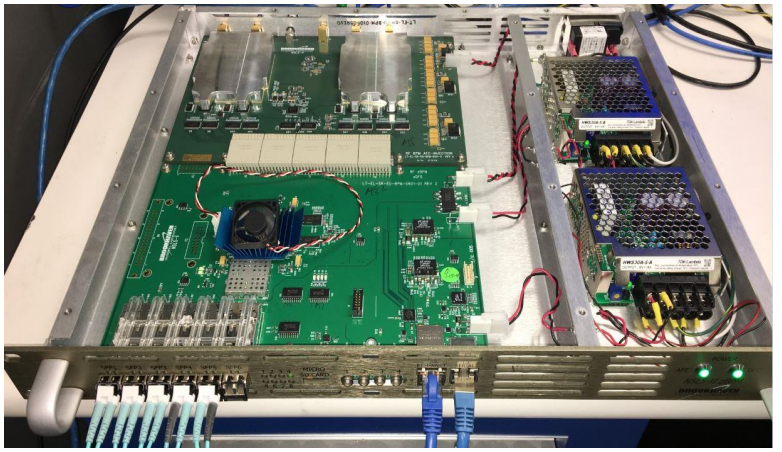
zDFE/AFE Functional Bench Test Status

- Main Functional blocks of zDFE are operational
  - ✓ Power Management, DC/DC converters
  - ✓ DDR Memory
  - ✓ Gigabit Ethernet
  - ✓ Serial Port
  - ✓ SD card : FPGA boots up and runs Linux
  - ✓ Embedded Event Receiver
  - ✓ Interface to Si5338 PLL
  - ✓ SDI Interface
  - ✓ Interface to AFE board complete
  - ✓ Pilot Tone Synthesizer chip working
  - ✓ RF / PT Attenuator working
  - ✓ AD9510 PLL programmed
- Firmware / Software / IOC / CSS Operational
  - ✓ ADC Raw
  - ✓ SA at 10 Hz
  - ✓ FA at 10kHz
  - ✓ TbT at 378kHz
- Integration Test with Beam (Sept ’17-Mar ’18)
  - Ongoing

Prototype Bench Configuration

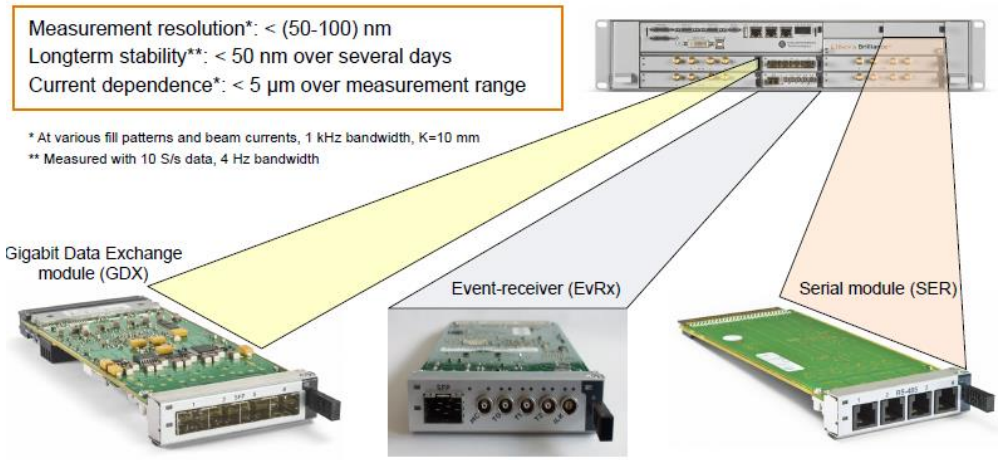


Prototype Chassis Configuration



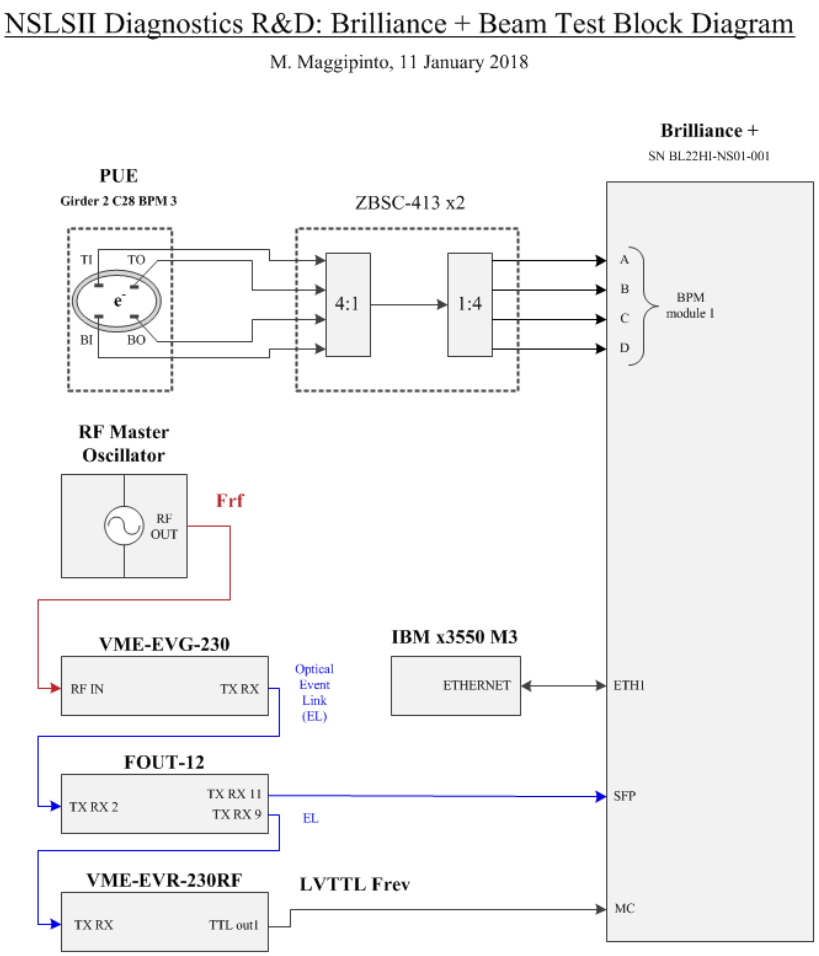
Libera Brilliance+ Performance Specifications

- Libera Platform B
- Compare (FA) in 10kHz <(50-100)nm
- Compare Long Term Stability over 8hrs in 10Hz (SA) <50 nm
- Verify with Beam

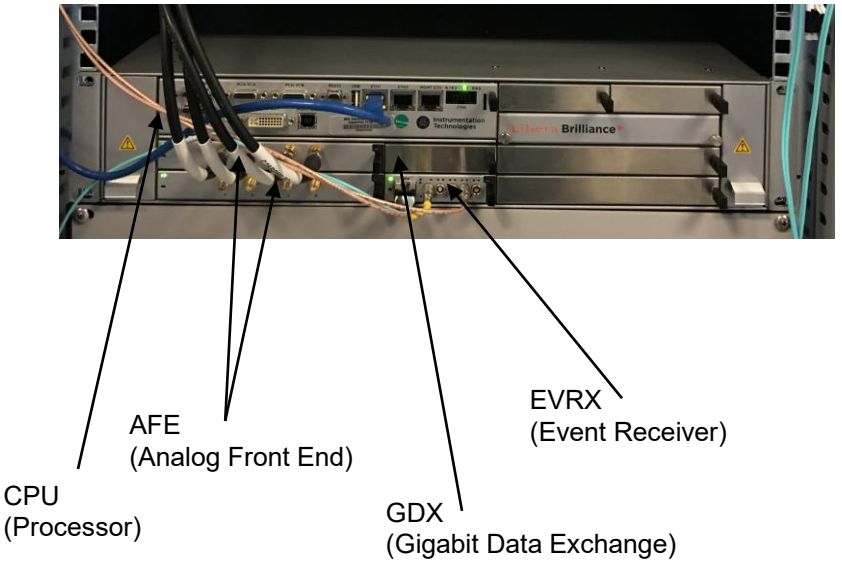


Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes Total
TBT	On-demand	256Mbytes Total
FOFB 10KHz	Streaming via GDX Link	(10kHz) Streaming X,Y,SUM
Slow Acquisition 10Hz	Streaming	(10Hz) Streaming X,Y,SUM
System Health	Streaming	(10Hz) Streaming Temp, FPGA Die temp, PLL lock status, etc.

Libera Brilliance+ Beam Test Configuration



- 4 U modified uTCA platform
- **Libera ADC Fs = 116.9705 MHz**
- zBPM ADC Fs = 117.3491 MHz



zBPM/Brilliance+ System Integration Test Config

➢ MC28RG-G1 BPM Development Rack

- Stand-alone Temperature Controlled to .1 degC
- Standard NSLS-II Timing System
- Dedicated PUE for testing
- Dedicated NSLS-II Cell Controllers

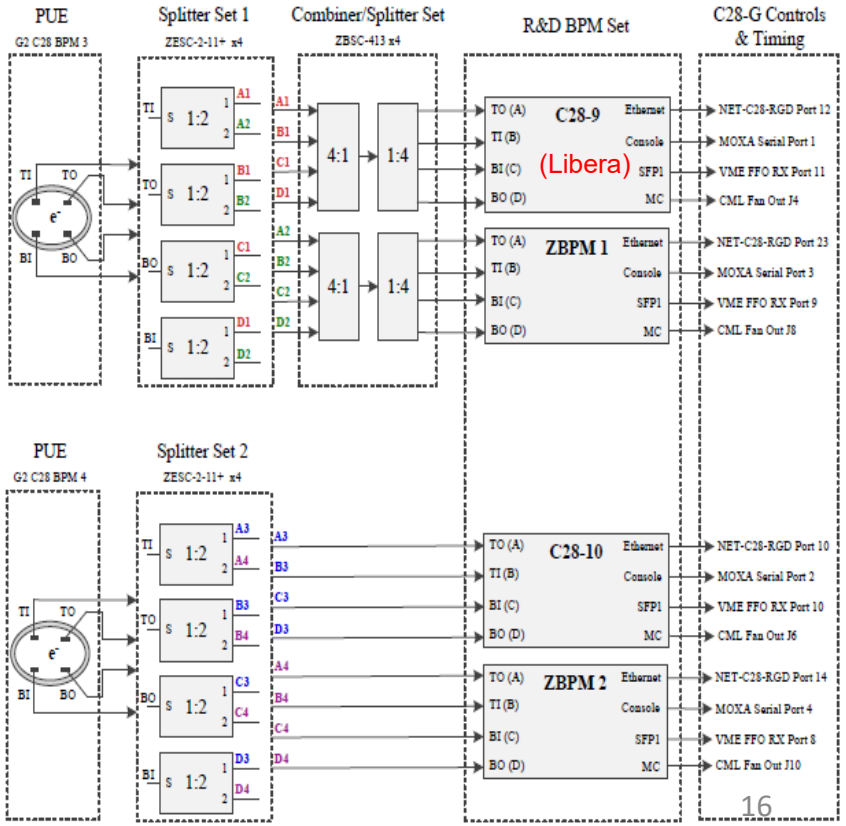
Diagnostics R&D Rack **MC28-RG-G1** Block Diagram

Version 2, M. Maggipinto, 01/09/2017

Device	IP Address	MOXA Port
28-9	10.0.142.196	4001
28-10	10.0.142.197	4002
ZBPM 1	10.0.153.29	4003
ZBPM 2	10.0.153.38	4004

MOXA IP = 10.0.132.42

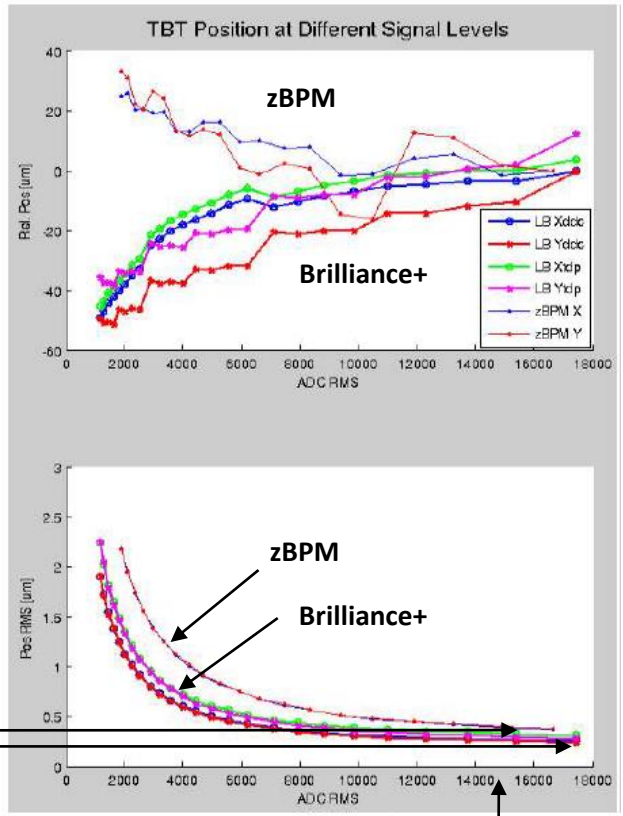
➢ zBPM 1, 2 installed and configured in Rack, fully integrated to PUE 1, 2



(Test 1) zBPM / Libera Brilliance+ TbT Resolution

- ➢ **Test Conditions 1:**
- ✓ *RF Attenuator scanned with fixed beam current and fill pattern* 350mA top-off, 1000 bunches
- ✓ Data collected zBPM/Brilliance+ in TbT Mode
- ✓ Each unit connected to same 4-button PUE w/splitter/combiner
- ✓ zBPM PT off
- ✓ Brilliance+ Crossbar switch off
- ✓ TbT data of the DDC and TDP recorded
- ✓ No Spike Removal

- Absolute position changed by ~10 microns



- zBPM meets NSLS-II Requirements
- Plans to change FIR filtering to limit BW and improve TbT, FA resolution.

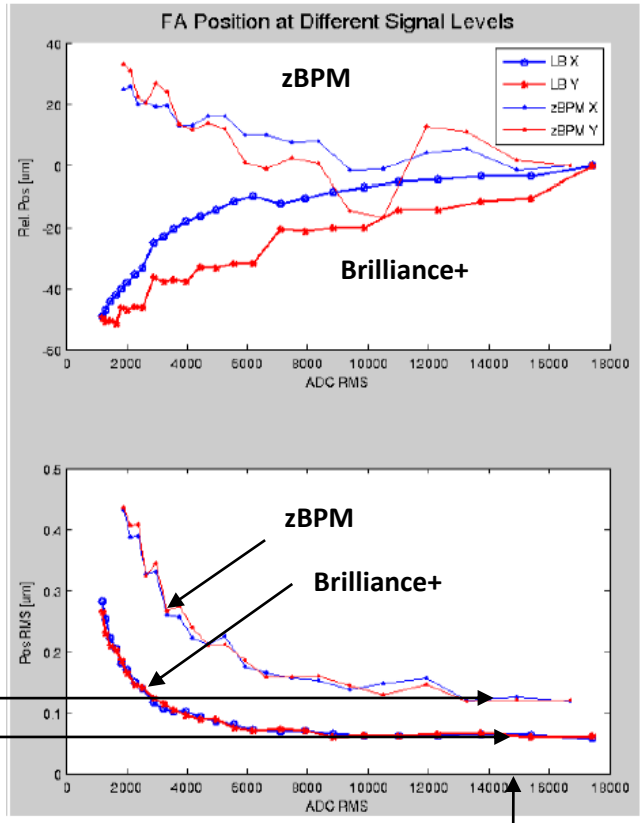
Brilliance +(250nm)

zBPM(400nm)

(Test 1) zBPM / Libera Brilliance+ FA Resolution

- ➢ **Test Conditions 1:**
- ✓ *RF Attenuator scanned with fixed Beam Current and Fill Pattern*
- ✓ 350mA top-off, 1000 bunches
- ✓ Data collected zBPM/Brilliance+ in FA Mode
- ✓ Each unit connected to same 4-button PUE w/splitter/combiner
- ✓ zBPM PT off
- ✓ Brillianc+ Crossbar switch off
- ✓ FA data derived from TbT DDC data
- ✓ No Spike Removal

- Absolute position changed by ~10 microns



- zBPM meets NSLS-II Requirements
- Plans to change FIR filtering to limit BW and improve TbT, FA resolution.

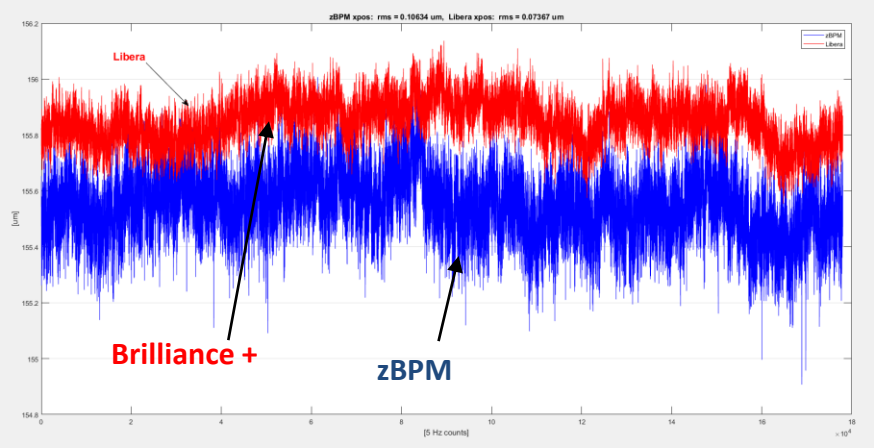
zBPM(125nm)

Brilliance +(75nm)

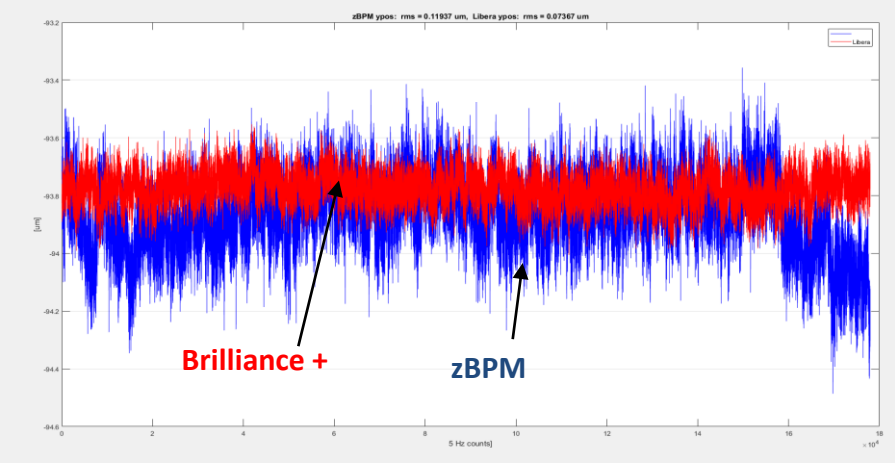
(Test 1) zBPM / Brilliance+ SA Long Term Stability

Data Type	Beam Conditions	RF Attenuator	zBPM σx,σy (RMS)	Brilliance+ (w/o Crossbar switch) σx,σy (RMS)
Slow Acquisition (SA), 10Hz Long Term Stability (9hrs)	300mA, 1000Bunches	11db 15db	n/a 106nm, 119nm	73.6nm, 73.6nm n/a

zBPM / Brilliance+ x position



zBPM / Brilliance+ y position

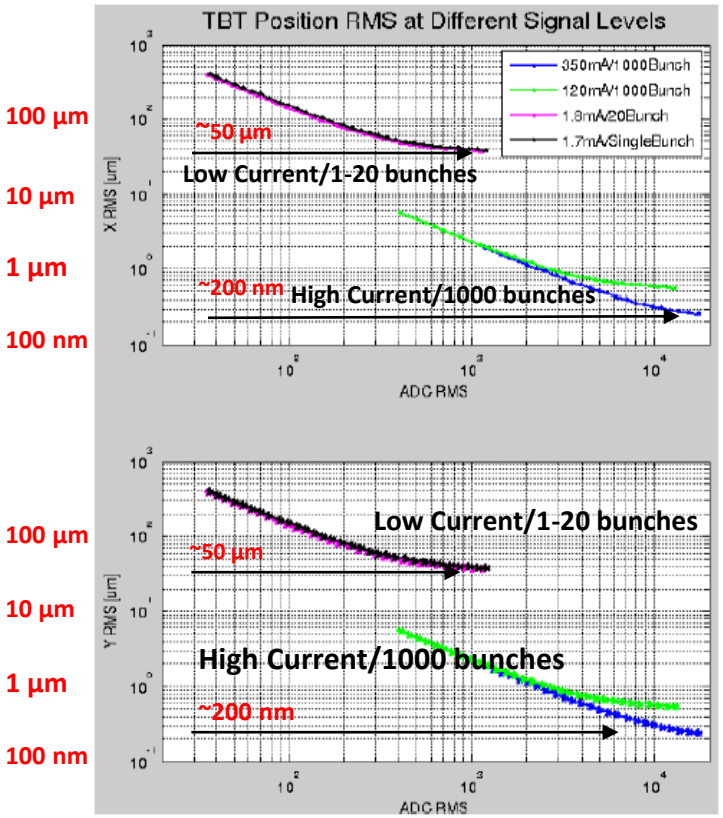


(Test 2) Libera Brilliance+ TbT Resolution

- ➢ **Test Conditions 2:**
- ✓ *RF Attenuator Scan for 4 different Beam Current/Fill patterns*
  - 350mA/1000 Bunches
  - 120mA/1000 Bunches
  - 1.8mA/20 Bunches
  - 1.7ma/1 Bunch

- ✓ Brilliance+ Crossbar switch off
- ✓ TbT data of the DDC and TDP recorded

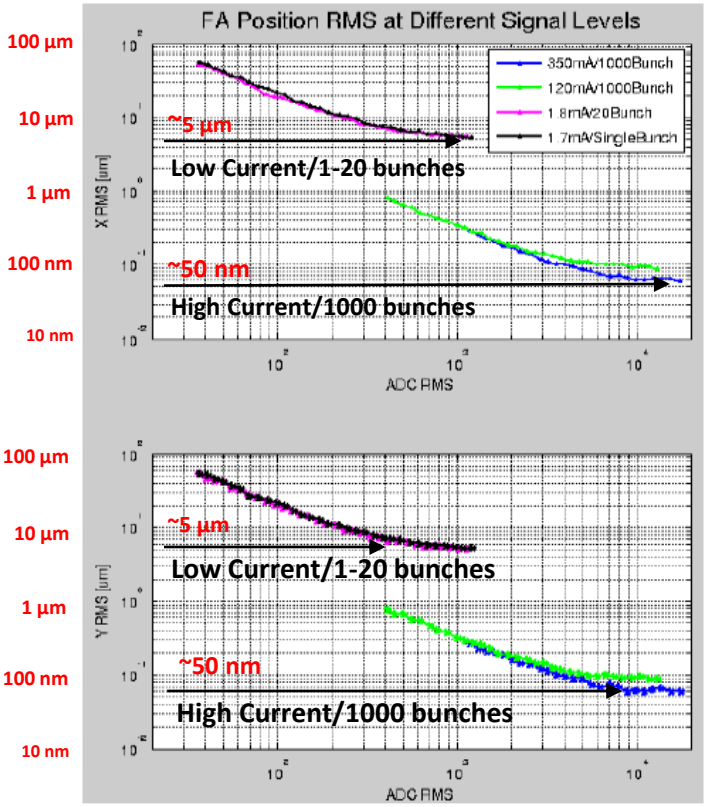
TBT POSITION



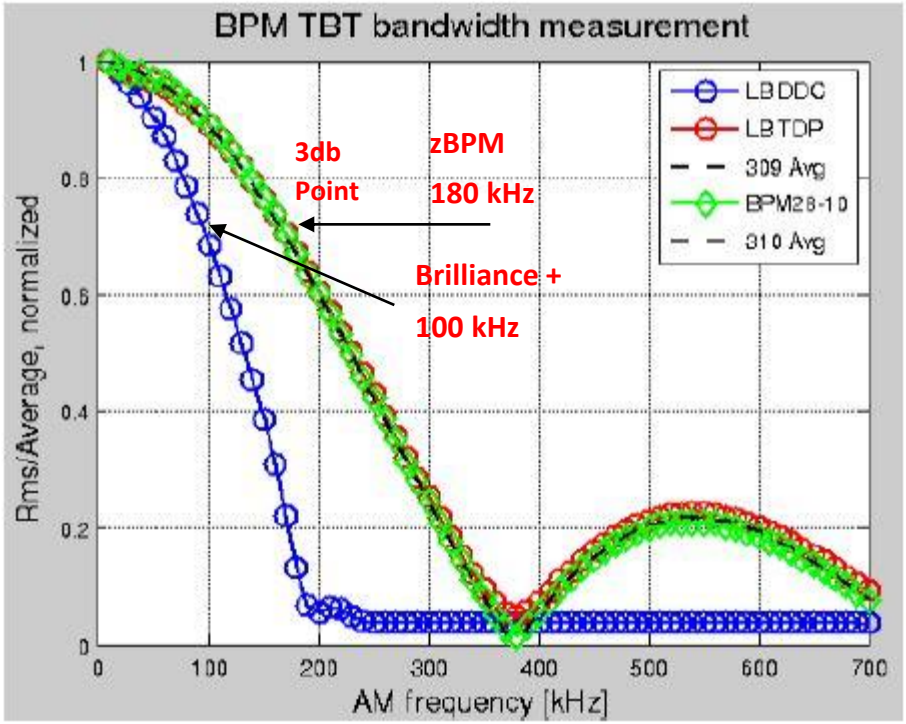
(Test 2) Libera Brilliance+ FA Resolution

- **Test Conditions 2:**
- ✓ RF Attenuator Scan for 4 different Beam Current/Fill patterns
  - 350mA/1000 Bunches
  - 120mA/1000 Bunches
  - 1.8mA/20 Bunches
  - 1.7ma/1 Bunch
- ✓ Brilliance+ Crossbar switch off
- ✓ FA data derived from TbT DDC

FA POSITION



(Test 3) zBPM/Brilliance + TbT Bandwidth

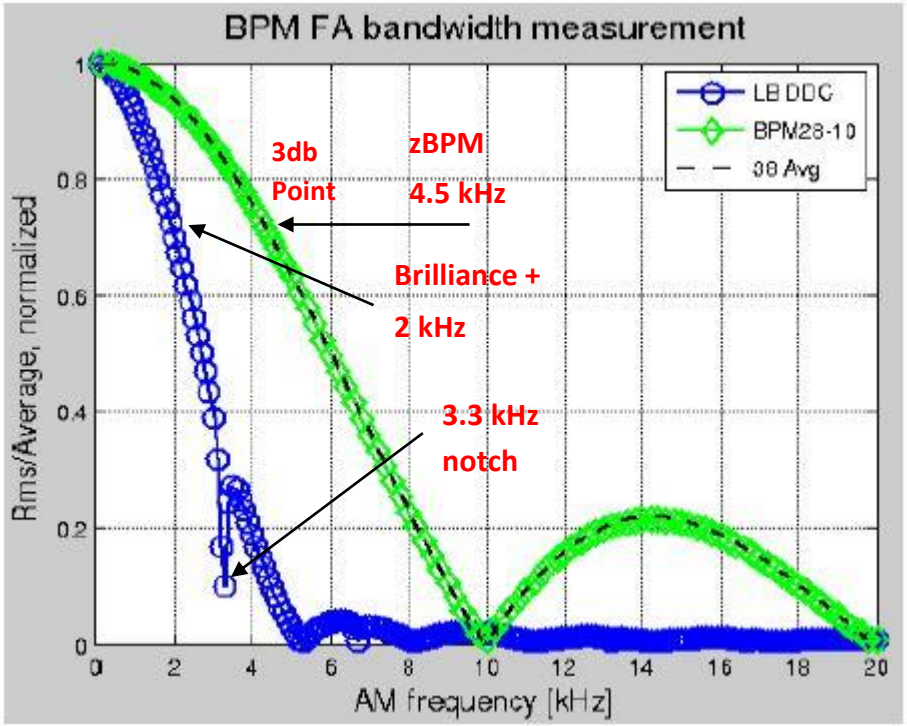


Bandwidth Measurement:

- The BPM electronics bandwidth was measured with AM modulated CW signal using a R&S SMA-100A signal generator.
- Modulation frequency was scanned to measure the button signal in TbT mode.

TBT data
NSLS2 BPM – 310 block average
Libera DDC – CIC + FIR
Libera TDP – 309 average

(Test 3) zBPM/Brilliance + FA Bandwidth



Bandwidth Measurement:

- The BPM electronics bandwidth was measured with AM modulated CW signal using a R&S SMA-100A signal generator.
- Modulation frequency was scanned to measure the button signal in FA mode.
- 3.3kHz notch is visible, and is intended to cut the crossbar switch aliasing.

FA data
NSLS2 BPM – 38 block average
Libera – 3-tap FIR + notch filter at 3.3kHz

Performance Summary Table

Comparative Performance Measurements and Features
NSLS-II RF BPM, Libera Brilliance Plus BPM 3-1-18

ITEM	METRIC	SPEC	zBPM	BRILLIANCE + (w/o crossbar)	zBPM (Target Performance)	DESCRIPTION
1	*Measurement Resolution*					*350ma Top-Off, 1000 Bunches*
1.1	ADC (117.35MHz)	N/A	N/A	N/A	500Mhz	ADC RAW
1.2	TbT (378.55kHz)	1µm	~400nm	~250nm	~150nm	Turn by Turn
1.3	FA (10kHz)	200nm	~125nm	~75nm	~50nm	Fast Acquisition
1.4	SA(10Hz)	200nm	~110nm	~75nm	~50nm	Slow Acquisition (Long Term Stability)
1.5	BW-TbT	N/A	~180kHz	~100kHz	TBD	Band Width in TbT
1.6	BW-FA	N/A	~4.5kHz	~2kHz	TBD	Band Width in FA
2	*Optical Fiber Interface*					
2.1	EVENT LINK	5Gb	10Gb	6.5Gb	N/A	Event Rcvr/Timing Data Rate
2.2	SDI LINK / GDX	5Gb	10Gb	6.5Gb	N/A	Fast Data for FOFB Data Rate
3	*RECORD LENGTHS*	**MODE**	**zBPM**	**BRILLIANCE +**		**DESCRIPTION**
3.1	ADC (117MHz)	On-Demand(wfm)	100Mbytes/ 12Msamples	256Mbytes/ 1Msamples	100Mbytes/ 12Msamples	RAW ADC per channel
3.2	TbT (378kHz	On-Demand(wfm)	100Mbytes/ 2Msamples	256Mbytes/ 2samples	100Mbytes/ 2Msamples	TbT (Frev=378kHz)
3.3	FA (10kHz)	Streaming & On Demand(wfm)	100Mbytes/ 2Msamples	10kHz streaming	100Mbytes/ 2Msamples	FA (10kHz) Streaming
3.4	SA(10Hz)	Streaming & On Demand(wfm)	SD Card Based	10Hz streaming	N/A	Long Term Stability
3.5	System Health	Streaming	SD Card Based	10Hz streaming	N/A	Temps, sys-status

Brilliance+ Summary/Observations

- At Typical Current/ Fill Pattern for NSLS-II operations(350ma/1000bunches): Brilliance + demonstrates very good performance.
- Significant SA (10Hz) performance improvement w/Crossbar switch.
- Configuration Issue: Int/Ext Trigger not synchronize w/ADC sample clock. Improve firmware?

zBPM Summary/Observations

- RFBPM zDFE board is completed, and fully functional for NSLS-II application
- 10 Gbps transcievers will support future development for the FA and FOFB.
- Achieved performance specification for NSLS-II (same DSP firmware)
- Use of Newer Xilinx/Vivado development environment
- Implementation of Embedded Debian Linux operating system for ARM dual core processor
- Implementation of Embedded EPICS IOC
- Developed the Linux DMA driver for DDR3 memory access (ADC, TBT, FA)
- Expanded support for Pilot Tone(PT) signal processing for active calibration.

Look Ahead: Next Generation AFE

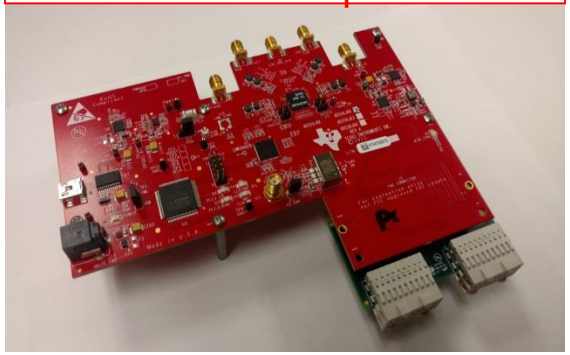
- RF BPM zAFE Development
- ✓ Support Active (PT Based) Calibration (Possible to Collaborate with ALS)
- ✓ New Pilot Tone Combiner (zPTC) Module
- ✓ Non-Dependence on Temperature controlled rack
- ✓ Improve Long Term Stability

- BbB zAFE Development
- ✓ 500Msps 14/16 Bit ADC(ADS54J66,ADS54J69) resolve bunches within a turn (BbB position data)

Next Gen ADC Considerations

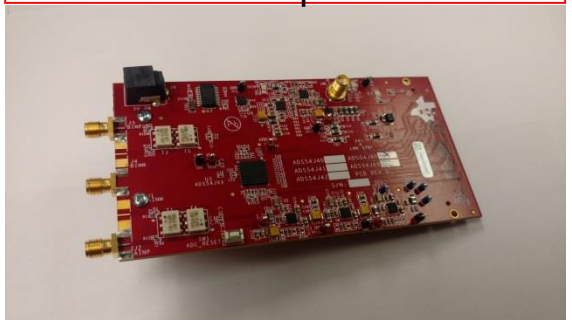
- 3 TI Evaluation Boards under test:
- ✓ ADS54J66 500Msps 14 Bit ADC (4 channel)
- ✓ ADS54J69 500Msps, 16 Bit ADC
- ✓ ADS54J60 1Gsps, 16 Bit ADC

ADS54J66-500Msps 14Bit



ADS54J68-500Msps 16Bit

ADS54J60-1Gbps 16Bit



Look Ahead: Next Generation FPGA (Zynq UltraScale)

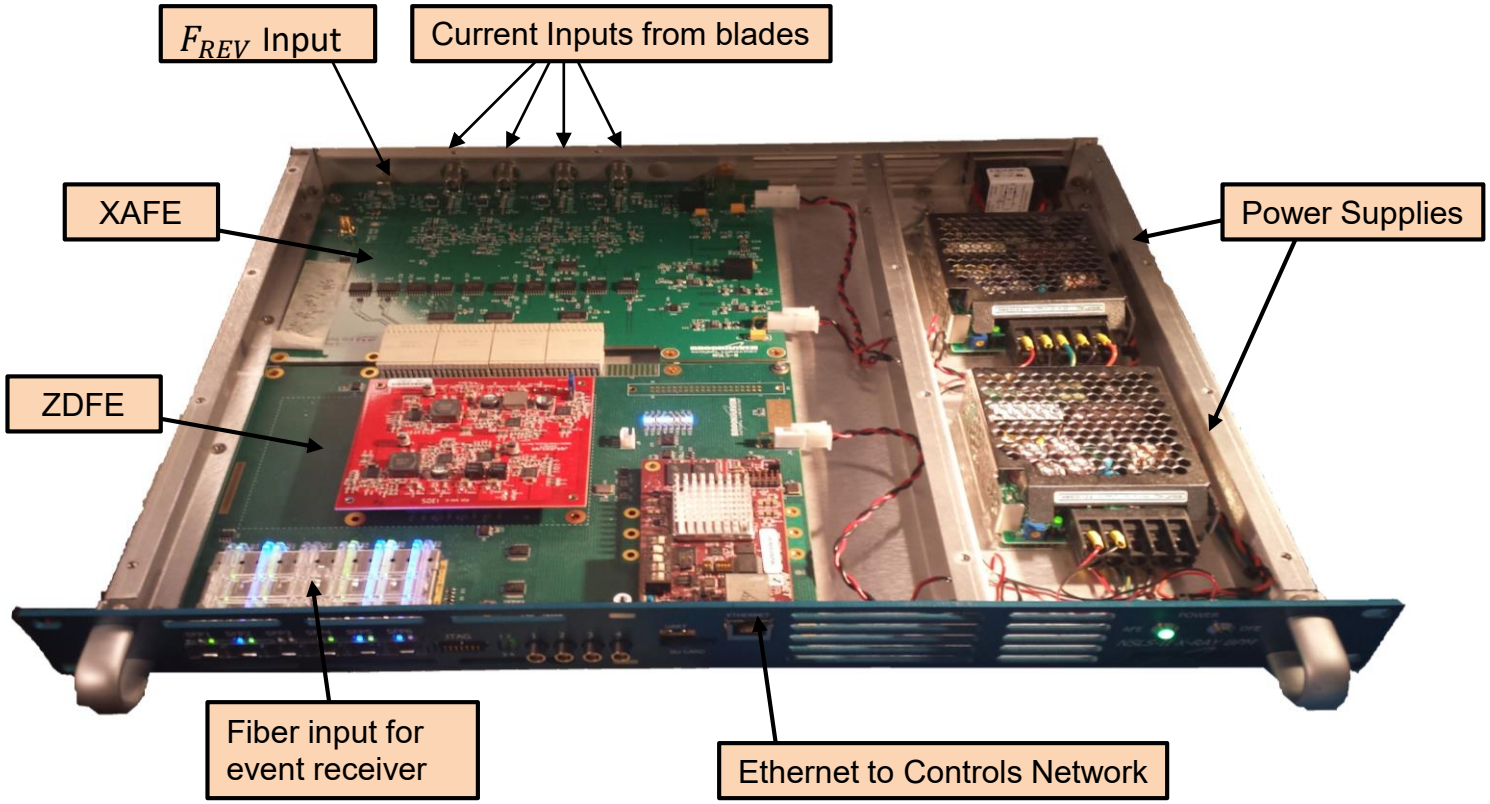
- Purchased Zynq UltraScale+ Evaluation board
  - 16nm technology as opposed to 28nm technology for Zynq
  - Quad-Core A53 Process @1.5GHz as opposed to Dual-Core A9 Processor at 700MHz for Zynq
  - Testing planned for 2018

Processing System (PS)

Features	All Devices
Application Processing Unit	Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5GHz
Real-Time Processing Unit	Dual-core ARM Cortex-R5 MPCore™ up to 600MHz
Graphics Processing Unit	ARM Mali™-400 MP2 up to 667MHz
Dynamic Memory Interface	DDR4, LPDDR4, DDR3, DDR3L, LPDDR3
High-Speed Peripherals	PCIe® Gen2, USB3.0, SATA 3.0, DisplayPort, Gigabit Ethernet
Maximum I/O Pins	214

Zynq UltraScale Processing System

X-Ray BPM Electonics

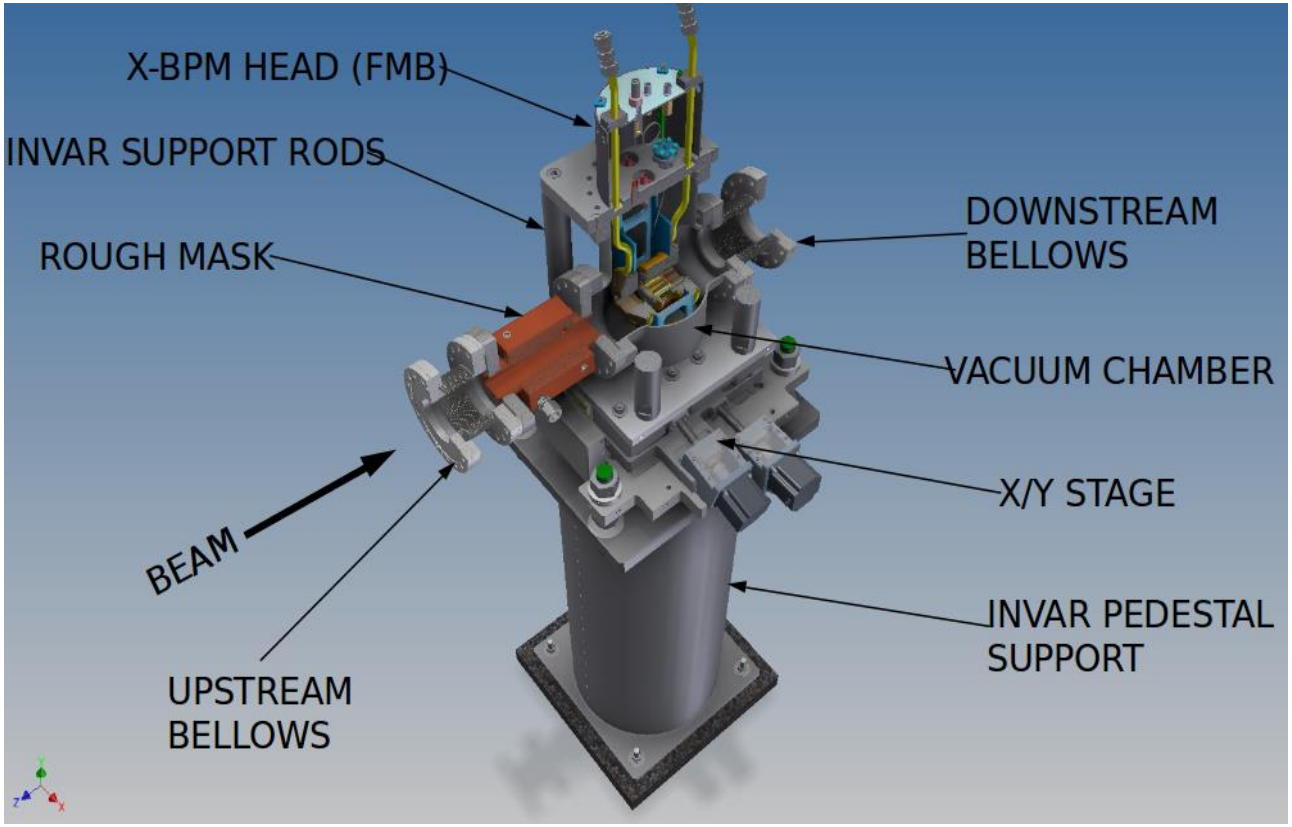


Features:

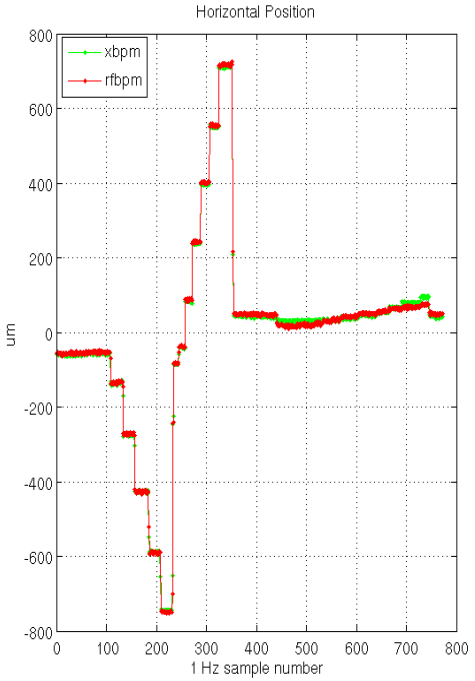
- Linux Operating System
- Embedded EPICS IOC and caClient Applications
- Python scripts for FFT calculations and other data processing
- Knowledgeable Users have access to all internal functions
- Very flexible, changes can usually be implemented within hours

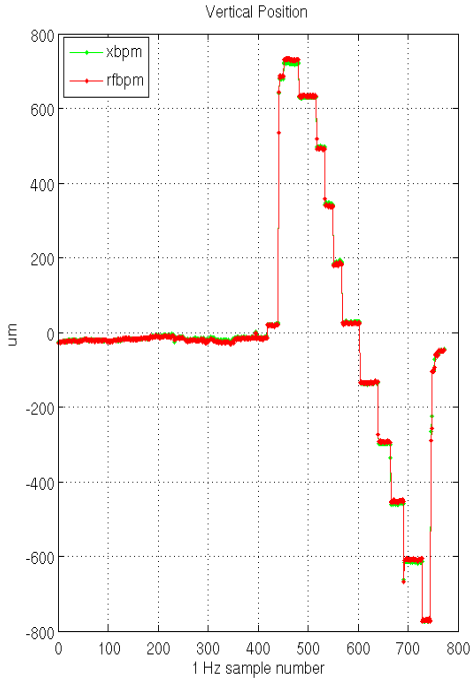
X-Ray BPM Blades and Chamber Assembly

XBPM Chamber Assembly



X-Ray BPM Resolution Measurement





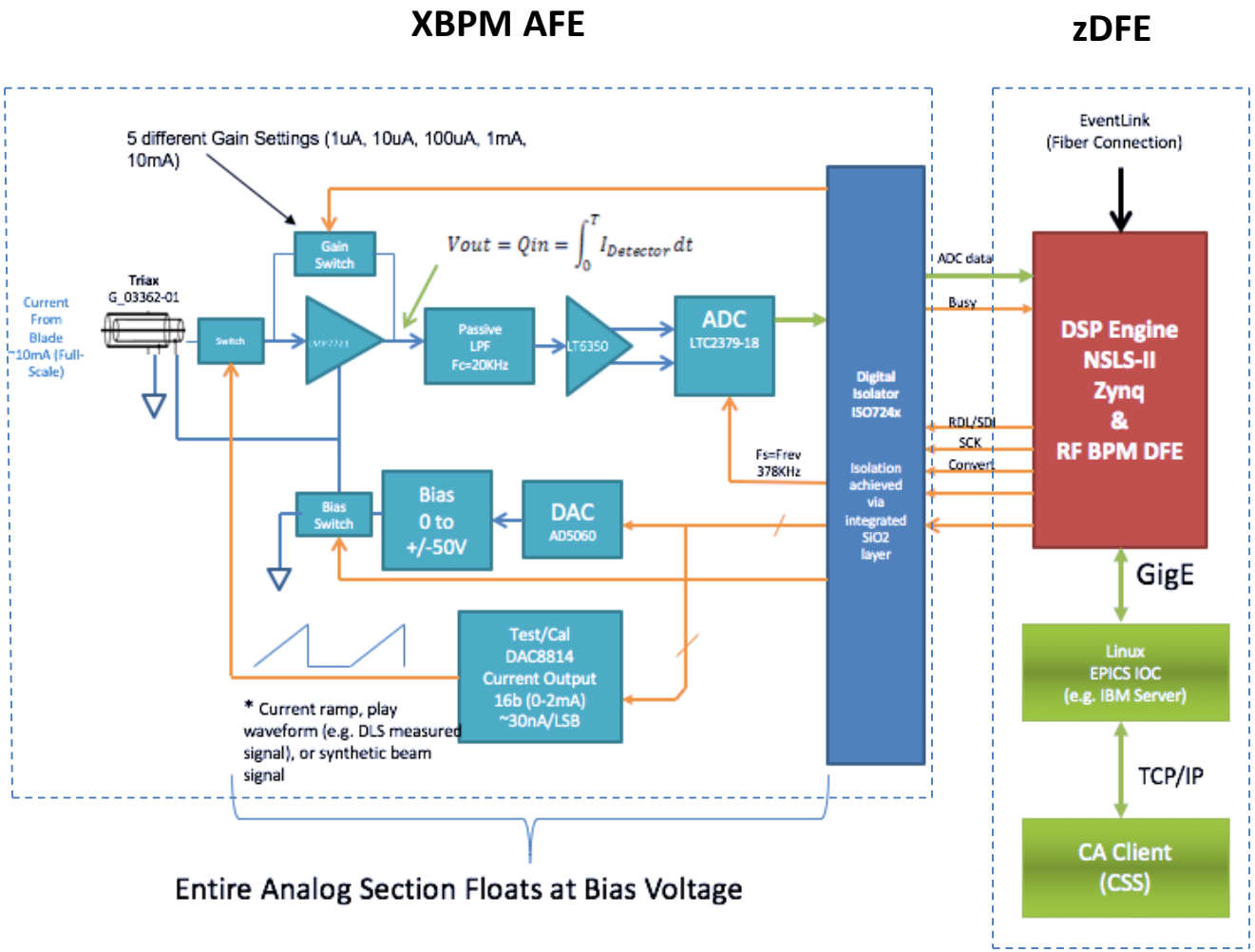
Test Condition:

- Manually swept local bump from -0.5mrad to +0.5mrad in Horizontal and Vertical planes
- XBPM position matches position calculated from 2 ID EBPMs

Resolution Measurement

# Samples	σx pos	σy pos	Data Type
3000	200nm	163nm	10Hz

X-Ray BPM Block Diagram



BPM Development Team

Dan Padrazo (Project Manager)
Weixing Cheng (Physics)
Kiman Ha (Embedded Controls, EPICS/IOC, FPGA)
Joe Mead (FPGA, DSP, DFE Board Design)
Tony Caracappa (Embedded Controls, EPICS/IOC, AFE)
Bel Bacha (RF)
Bernard Kosciuk (Mechanical, Thermal Analysis)
Marshall Maggipinto (Technical Support)
Chris Danneil (Technical Support)
John Bohenek (DFE Board Design)
John Kuczewski (Embedded Controls, Linux Kernel)
Om Singh (Retired)
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Contributions to this presentation:

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zDFE Configuration Test:

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zBPM/brilliance + Integration Testing:

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XBPM Performance Tests/Integration:

Petr Ilinski, Tony Caracappa, Joe Mead

Thank You for Your Attention!