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DEVELOPMENT OF THE RF SYSTEMS FOR THE PolFEL ACCELERATOR*

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Abstract

PolFEL stands for Polish Free Electron Laser, the first FEL research infrastructure in Poland. This facility is under development, and it will operate in three wavelength ranges: IR, THz and VUV, using different types of undulators. Machine will be driven by 200 MeV linear superconducting accelerator, which will operate in both, pulsed wave (PW) and continous wave (CW) modes. This contribution will describe the concept, current status and the first results of the RF systems development.

INTRODUCTION

PolFEL will be a 4-th generation light source, based on the 200 MeV superconducting linear accelerator [1]. It will generate coherent light in 3 ranges: THz, IR and VUV.

To deliver proper beam conditions, a stable RF field is required in the accelerator cavities, and to achieve this, a high-power and low-level RF systems are required. PolFEL accelerator will be driven by a solid state amplifiers, in the single cavity regulation mode where one cavity will be driven by one amplifier. For such control mode, vector sum calculation is not needed, which simplifies the the RF control system in comparison to such Free Electron Lasers such as X-FEL or FLASH.

To simplify the LLRF system even more, a direct sampling technique is planned to be implemented in PolFEL [2]. This technique reduces the need for the separate devices such as downconverters and LO generation modules. The key part of the direct sampling LLRF system will be the clocking solution for the ADCs, but since the whole clock tree will be integrated into the ADC board, it can be optimized for this particular application.

HIGH POWER RF SYSTEM OVERVIEW

The aim of the RF system is to deliver power to accelerating modules which is needed to accelerate the electron beam. The accelerating modules of in PolFEL accelerator will be made of TESLA-type, 9-cell RF Structures. Each criomodule will have two such RF structures, but each structure will be driven and controlled individually. RF power from solid state amplifiers to the criomodules will be delivered using WR650 waveguides. Solid state amplifiers will be placed in the hall next to the accelerator tunnel. Because construction of PolFEL accelerator will utilize existing buildings, the design of the waveguides distribution system is not straight-forward and requires significant effort.

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Table 1: SSA Key Parameters

Parameter	Value
Lower frequncy range (-3dB)	≤ 1270 MHz
Upper frequecy range (-3dB)	≥ 1310 MHz
Output power in pulsed mode	≥ 7kW
Maximal pulse duration	≥ 1 ms
Output power in continous mode	≥ 5kW
Maximal power of input signal	≥ 10 dBm
Amplifier gain	≥ 60 dB
Max. required power supply level	≤ 20 kW
Operational temerature range	5 °C - 40 °C

One of the features that helps in the wageguide design is single cavity regulation mode. Because of this, there is no need for splitting the RF power withing the waveguide distribution system. Each waveguide will deliver RF power directly from the solid state RF amplifier to the RF structure. In such configuration, circulators and loads does not have to be placed close to the criomodules and can be placed next to the RF amplifiers out of radiation impact area, which also helps in the design.

Solid State Amplifier

The RF power in the PolFEL accelerator will be generated by solid state amplifiers (SSA). Because of PolFEL will operate in continuous mode a dedicated RF power source is needed. Dedicated RF amplifier for PolFEL will be designed and delivered by the Kubara Lamina S.A. company [3]. The requirements for the RF amplifier are following show in Table 1.

By the time of writing this paper, the prototype of the SSA amplifier was under development (Fig. 1).

LOW-LEVEL RF SYSTEM OVERVIEW

High speed and high bandwidth ADCs makes possible to sample directly the RF signal of the frequency 1.3 GHz. Well known and also evaluated [4,5] for this purpose is Texas Instruments ADS5474, which input bandwidth covers range up to 1.4 GHz. Possibility of direct RF sampling allows to significantly simplify the LLRF hardware.

The components of the PolFEL LLRF system are similar to the ones used at X-FEL [6] because of the same fundamental frequency 1.3 GHz, but the layout of the system is more like the one used at ESS [7], because ESS operates also in single cavity regulation mode.

LLRF system scheme in the Fig. 2 show the configuration used at ESS. Configuration used at ESS for controlling

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Figure 1: Prototype of the solid state amplifier for PolFEL under development.

single cavity occupies 3 slots in the MTCA chassis, and results in total number of 6 devices (3xAMC + 3xRTM) for single cavity (Fig. 2). One slot is occupied by the main LLRF Controller, which uses both boards: AMC with FPGA and data converters, and RTM with the downconverters and vector modulator. Other two slots are occupied by the piezo controller, and LO clock signal generator.

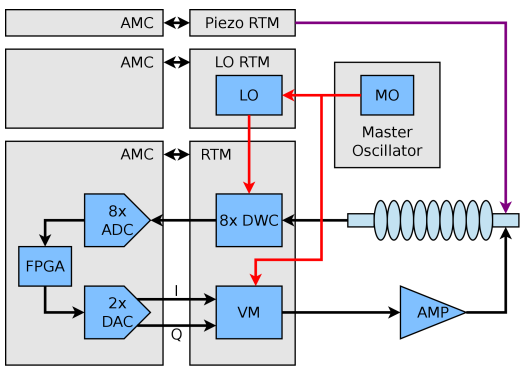

Figure 2: ESS LLRF System architecture.

The concept of the PolFEL LLRF controller (Fig. 3) is much simpler, for single cavity control single MTCA chassis slot is occupied. From the rear side of the slot the Piezo RTM will be placed, and from the front side an AMC FMC Carrier will be used. All LLRF specific infrastructure will be placed on the custom dual FMC board. With respect to the amount of connected I/O pins in the FMC connectors, any MTCA.4 FMC carrier can be used. This configuration does not require down-converters, so separate LO generation device is not required as well.

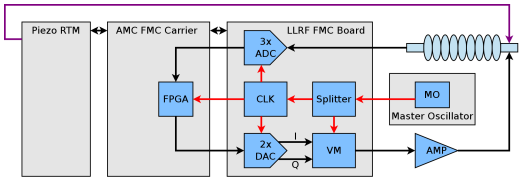

Figure 3: PolFEL LLRF System architecture.

The function of the LO generation is performed by proper circuitry integrated in the FMC board along with the ADCs and DACs. The ADC sampling clock is generated directly from the 1.3 RF signal, and the distance from RF input to the ADC or vector modulator is less than 10 cm. All clock distribution for a single LLRF system will be made on the single PCB.

Initial Tests of LLRF with the Copper Cavity

To evaluate described concept, a test setup has been assembled. To make tests as much similar to the final applucation, a 1.3 GHz, 3-cell, copper cavity has been used.

As a first step, the cavity has been measured and couplers tuned using Vector-Network Analyzer (Fig. 4). In the next step, the field in the cavity has been excited using the RF generator on one side, while the signal from the other coupler was connected to FPGA based system (Xilinx KC705 evaluation board) with ADS5474 ADC attached on the Curtiss-Wright ADC511 FMC mezzanine. Using digital I/Q detection, it was possible in the FPGA to restore the amplitude and phase of the cavity field.

In order to close the feedback loop, vector modulator was needed. For the purpose the FMC board with dual-channel DAC and vector-modulator has been designed, and manufactured (Fig. 5).

Having all components available, the complete setup has been assembled (Fig. 6). Signal from the RF generator has been split and delivered to vector modulator as source RF signal to be modulated, and to clock synthesizer, which generates frequencies suitable for ADCs and DACs. Clock synthesizer can additionally provide clock signal to the FPGA

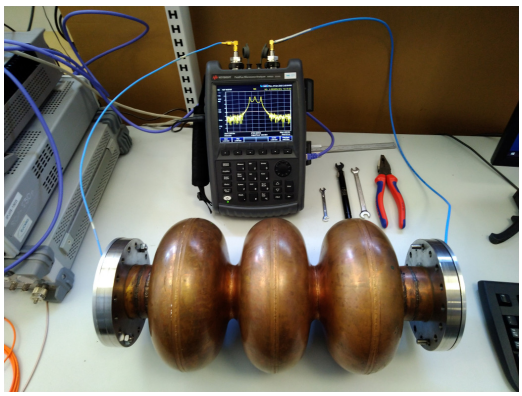

Figure 4: Cavity characterized using VNA.

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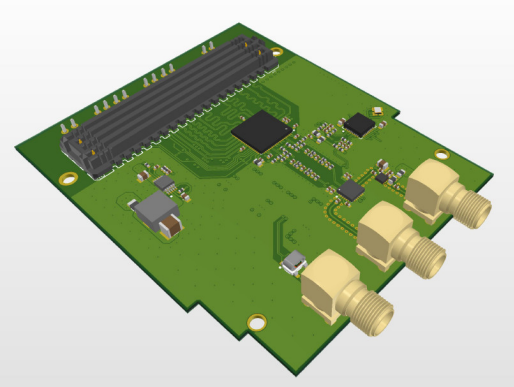

Figure 5: Vector modulator FMC board.

device using FMC_M2C signals, but this was not necessary because ADCs and DACs provides clock synchronized with their data.

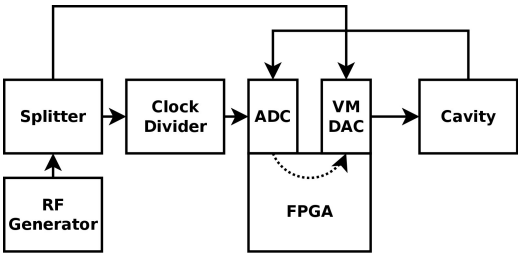

Figure 6: The scheme of the test setup.

Finally, using presented test setup, feedback loop on the copper cavity has been closed. Images below (Figs. 7, 8, 9) shows the single pulse of the input and output of the controller.

Figure 7 shows amplitude and phase the output signal from the controller on top of the feed-forward value (the ideal drive signal). The difference between feed-forward and output signal is caused by working closed loop feedback.

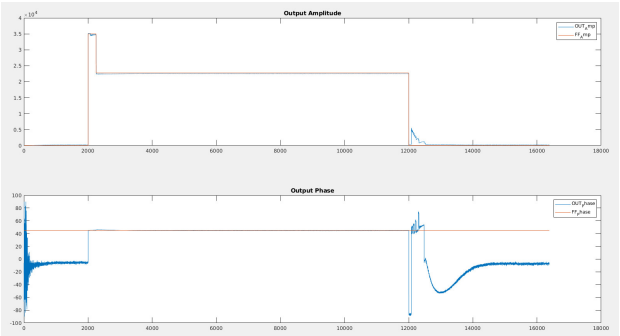

Figure 7: Controller output.

Figure 8 shows similar image like Fig. 7, but it shows the amplitude and phase of the controller input signal on top of the set-point value (expected cavity field).

To show better the input signal on top of the set-point Fig. 9 shows magnified amplitude and phase regions of the RF pulse.

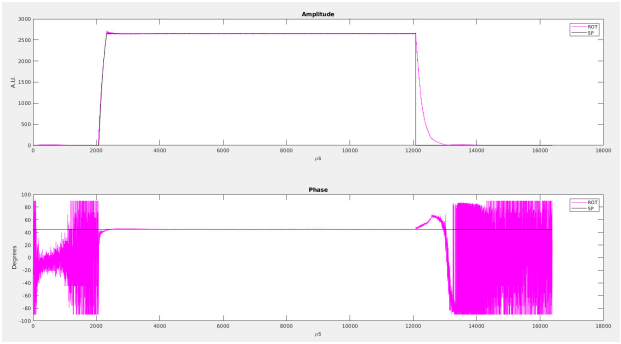

Figure 8: Controller input.

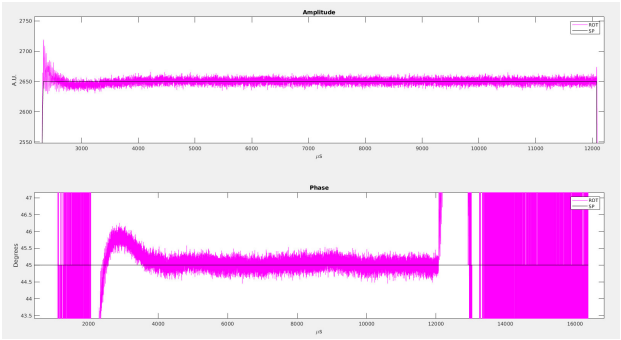

Figure 9: Controller input (magnified).

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