A Digital Synthesizer and Phase Control System for RF-Acceleration in COSY

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Abstract

The Cooler Synchrotron COSY is intended to operate its ferrite-loaded radio frequency (rf) acceleration station operating at fundamental (h=1) frequencies ranging from 0.4 to 1.6 MHz. A fully digital vector controller with high temporal and value resolution is under development to synthesize the low level acceleration rf voltage waveform. Its phase angle is set both externally, and from a beam-to-cavity phase locking loop (PLL). The PLL consists of only digital components, with analog-to-digital converters (ADC) at beam monitor and cavity, and a digital-to-analog converter (DAC) for output to the amplifier chain. Locking range and control bandwidth is a full 2π, and > 50kHz, respectively, to allow for programmed phase jumps at the γ-transition. Resolution of 12 to 16 Bit and oversampling at up to 25 MSPS are realized by recent video digital control and digital signal processing (DSP) technology. The synthesizer part, at first for use without beam-phase feedback, has been completed and used for first tests on the acceleration station. Major components for the PLL upgrade have so far been tested under operations conditions, and the corresponding circuitry is being finalized.

1. INTRODUCTION

Traditionally, frequency signals for rf acceleration in synchrotrons are generated by analog methods. Because of the large frequency swings in synchrotrons of up to a factor of ten, voltage controlled oscillators (VCO) are used without exception. They are tuned by the application of an adjustable analog voltage source. However, VCOs suffer from their main drawback of accuracy and stability limitations. Absolute frequency fidelity is crucial for accelerator systems with booster-to-main-ring particle transfer, requiring precise frequency alignment for all rings involved. Temperature drifts in VCOs are especially bothersome because of their frequency dependent power consumption and dissipation, leading to frequency hystereses from up- to down-ramping. Invariably, frequency signal generation must therefore rely on involved control circuitry to remedy these shortcomings.[1]

With the advent of very large system integration (VLSI) in circuit fabrication, fundamentally different methods based on numeric (digital) frequency synthesis, also referred to as numerically controlled oscillators (NCO), have emerged. In many cases, NCOs outperform conventional generators in typical characteristics, as accuracy, stability, tuning range/bandwidth, resolution, tuning speed, and signal modulation capability. As a matter of fact, the flexibility in some of these characteristics allows now, for the first time, to implement rf techniques thus far un-thought of.

NCOs render from an internal look-up table the values of a sine wave in time, which is then converted into an analog signal by a DAC. This process is timed by a *fixed-frequency* clock, whereby the NCO attains the clock's superior stability and phase noise properties, in spite of a large tuning range. Achievable *value resolution* (typically 8 to 16 bits) depends on the maximum clock rate of the NCO (typically 40 MHz to 1.5 GHz), see Fig. 1. This means, that NCOs, together with the attached output DAC, are limited by their realtime "computing" and conversion speed, resulting, for practical applications, in carrier synthesis of up to 500 MHz at signal-to-noise ratios (or spurious levels) of 42 dBc, or better for lower clock (i.e. carrier) frequencies. On the other hand, *frequency resolution* of a fraction of a Hertz is no exception.

Due to the NCO's digital nature, parameter setting is extremely fast; arbitrary frequency, phase (and sometimes also amplitude) changes can be completed within a few clock cycles, i.e. a microsecond or less. On the other hand, two or more NCOs can be synchronized for an indefinite length of time, even under frequency variation, and, if desired, at a fixed phase difference, if they are clocked by the same reference, and started by the same trigger. This is extremely useful for quadrature operation.

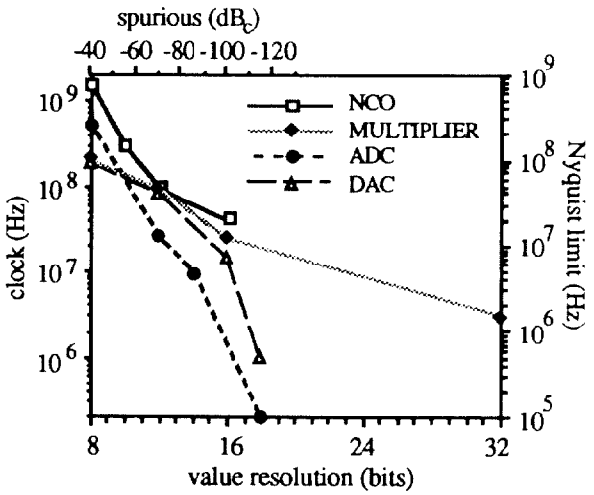

Fig. 1: Performance of present day digital rf VLSI circuits

Typical frequencies achieved with NCOs fall right into the regime of particle revolution frequencies (or their lower harmonics) in synchrotrons. Hybrid and up-conversion schemes with additional analog local oscillator frequency signals extend the range even more, or allow to further reduce

spurious content. NCO techniques are thus well suited for generating frequency signals in synchrotrons, including frequency generation for beam diagnostics. [2]

Aside from frequency generation, signal mixing is another main task in rf techniques. In the digital realm, it can be performed by multiplication. Real-time computation, however, requires a return-of-result time of some 10 to 50 nanoseconds, or less, i.e. a fraction of the rf carrier period. Although today's most advanced micro- or signal processors take now clock rates of 50 MHz, their performance-speed would fall short of this target by at least a factor of hundred. Instead, dedicated VLSI digital multipliers are used. Finally, for any sort of digital control, a measurement and conversion of the real-world rf signal by an ADC is needed. In short, a new brand of digital components with steadily increasing speed performance have evolved that are very well suited for *digital rf* (Fig. 1).

2. THE DIGITAL VECTOR CONTROLLER FOR COSY

Any rf controller for synchrotrons has to fulfill the two standard tasks of (a) a radio frequency signal generator, and (b) a PLL-type phase control to bring rf and beam-pulse phase in line.

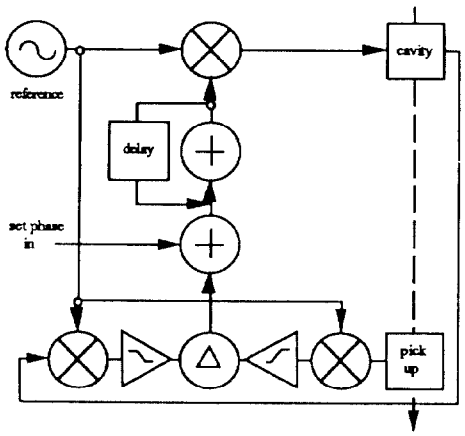

Fig. 2: Simplified control scheme

Table I: Rf parameter range and resolution

rf quantity	value range	value resolution		temporal resolution	
		stationary	transient	stationary	transient
frequency	0.3-1.6MHz	5Hz	50Hz	∞	10μs
amplitude	0-8kV	10V	10V	∞	10μs
phase	0-360°	0.5°	0.5°	∞	10μs

Fig. 2 shows the control scheme intended for COSY. It is greatly simplified, in that it suppresses the quadrature feature, described in Sect. 2.2 below. Characteristic target specifications for this rf control system are shown in Table I. Due to these requirements, the system was planned early on to be digitally controlled, incorporating one or another type of numeric oscillator. However, as a completely novel approach, the phase control part is also fully digital, implying control operations are *computed in real-time*. [3]

2.1. *frequency signal synthesis*

The synthesis system is specified so tightly, that in a first phase, COSY operation may rely on this synthesis part alone, without *any* feedback from either dipole fields ("B-train") or beam phase monitor (synchrotron loop), except a cavity-internal tuning control. The required time ramps of both magnetic fields and frequency signals will be computed for a desired particle momentum ramp, p(t). For simplicity, three types of time dependencies for p are "allowed": time constant bottom and top, a momentum in- or decrease linear in time, and transitions between these, quadratic in time. This applies both for the ramp-ups as for the ramp-downs, since COSY is also intended for storage and deceleration mode. All rf parameters are therefore constant for bottom and top, unless adiabatic trapping is used at bottom, where amplitude has to be slowly raised in time. Frequency only varies during the linear ramp, while all three parameters vary with time during the quadratic transitions. For the latter, only the product amplitude× sin(phase) enters. Even this being kept fixed, amplitude and phase still may vary separately only within limits not to exceed the momentum acceptance δ of the accelerator. However, any *one* temporal ramp of the three quantities (amplitude, phase, or acceptance) may be picked to uniquely determine the ramps of the other two. Schematic ramps are shown in Fig. 3, including a phase jump at the γ-transition.

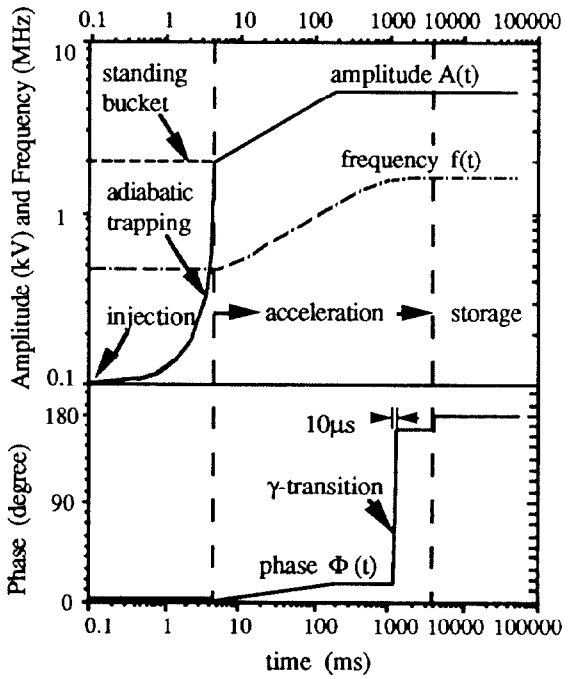

Fig. 3: Schematic depiction of rf parameter ramps

The synthesizer part, incorporating a UNIX-workstation controlled NCO in a VME environment, an output DAC, phase compensated analog filtering to eliminate the clock components from the signal, and line driving amplification with galvanic decoupling has been completed and used for first tests with the COSY acceleration station. The device was crucial for studying the station's transient behavior under rapid phase changes.[4]

At the core of the synthesizer, a 16-Bit NCO with frequency, phase and amplitude control is being used at a clock rate of 20 MHz. Digital-to-analog conversion is at 12 bit, 40 MHz clock rate, doubled by an interpolator for higher output fidelity, which takes some of the burden off of the output filter. A spurious content of better than -65dBc is achieved.

2.2. *synchrotron phase control upgrade*

For a phase control of the type shown in Fig. 2, a number of tasks is needed, e.g. frequency modulation and demodulation, phase discrimination, shifting and accumulation, as well as amplitude demodulation and digital filtering. Lacking sufficiently fast commercial signal processors, the control algorithm is built up in a hardware hybrid circuit, i.e. by single-task components. Nevertheless, the entire system is designed modular (by plug-in boards and on-board routing switches), that allow to reconfigure the algorithmic procedure to some extent. The over-all frame may be suitably chosen; we opted for a VME/VXI set-up. Mathematically, the algorithm must be integer binary for reasons of speed performance. It is made very efficient by invoking trigonometric calculus, involving sine and cosine, in lieu of phase values directly, which permits a full 2-π and 2-π periodic operation. This is in contrast to a standard PLL, whose range of phase control is commonly limited to less than π.

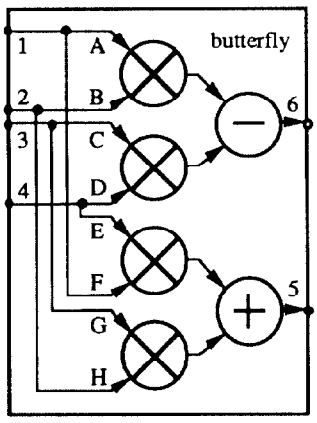

Fig. 4: Complex 16×16 bit multiplier used as "mixer"

Clock rates may be constant, as in the basic approach of Sect. 2.1. However, as an important feature, the algorithm can be made to be independent of frequency by clocking the entire circuitry with a rate *proportional to the carrier frequency to be synthesized*: an exact 16-times oversampling ensures constantly 16 sampling points in every rf period, irrespective of frequency. Actually, the clock delivers both 16 and 32 pulses per rf period. The latter is used for final interpolation before outputting the results via the DAC. The clock itself is based on NCO technology, while, in the final control configuration, the "reference" oscillator of Fig. 2 will be a simple look-up table for sixteen 16-bit words.

The backbone of the control circuit is a complex multiplier, 25-MSPS 16×16-bit, that can return a 32-bit value within two clock cycles (Fig. 4). This multiplier is used similarly to a mixer in analog circuitry, and performs all major tasks in the algorithm, except digital filtering and amplitude demodulation.

For the extreme speed requirements in rf applications, digital filtering methods must be restricted to utmost simplicity. We employ delay-line/pipeline (running average) filters with a length of several 1000 words each (for constant clocking) or of 16 words (for frequency-proportional clocking). In the latter case, any harmonic content may be eliminated *within one carrier period*, a feature inconceivable for analog technology.

Finally, amplitude demodulation for integer binary (i.e. fixed-point two's complement) arithmetic poses a challenge. Again, to achieve unsurpassed speed, no averaging over many periods is used. Instead, two alternatives are implemented. [3,5] (a) By use of two commercial VLSI polar/cartesian coordinate transformers back-to-back, the elimination of amplitude variations, necessary for phase discrimination, can be achieved in about 50 clock cycles, i.e. in about 3 rf periods. An even faster hybrid-circuit method uses extensively trigonometric identities and look-up tables, a manipulation taking less than one rf period.

3. CONCLUSIONS

Development and implementation of a fully digital rf frequency synthesis and phase control system is well under way, for use on the cooler synchrotron COSY. With it, a highly precise rf signal generation and control is available, with some features that are not possible with conventional techniques. The system can be configured flexibly, and should be suitable for other accelerator applications as well. A higher frequency version, generating carriers to about 10 or 15 MHz, should be conceivable with presently available commercial integrated circuit components.

4. REFERENCES

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