Lithography Production Techniques for Next Generations of Microelectronics

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Abstract

Advanced laboratory results indicate that the CMOS technology which is presently the mainstream technology for highly integrated silicon devices can be extended to effective channel lengths, even below 100 nm. At the end of this decade, the quarter Gigabit memory device with smallest design rules of a quarter micron will be in industrial mass production, and industrial prototypes of circuits of 0.15 µm will be available. Main technological problems on the way to achieving these goals will be the pattern generation, consisting of lithography and etching techniques, the control of extremely shallow doping profiles, the quality of surface conditions and layer interfaces, multilayer metallization schemes and a cost optimized flexible and stable production technique. Concerning the lithography process, in the nineties there will be a competition among very advanced optical lithography, X-ray lithography using synchrotron radiation and particle projection using either electrons or ions. The competition of different methods assures that at least one method will be available in time which fulfills the requirements for industrial mass production.

Forecasts of the future development of highly integrated silicon circuits are focussed on the so-called dynamic random access memory (DRAM), which are the devices with the highest complexity and integration density. They represent the forefront of technology development and show the smallest problems related to design rules and down scaling. Logic devices and microprocessors are also growing in complexity and integration level, but in the past they were at least one generation behind the DRAM development. It is imaginable that these development trends can be changed in future. It is possible that circuits for fast parallel computing of complex signals like pattern recognition etc., following the neural network scheme will need the highest integration levels. However, at the moment DRAMs are representing the forefront of technology development. Figure 1 shows the history of increasing complexity and simultaneously of decreasing smallest geometries on one chip. The line in Figure 1 (according to G. Declerck, IMEC) represented by squares indicates the

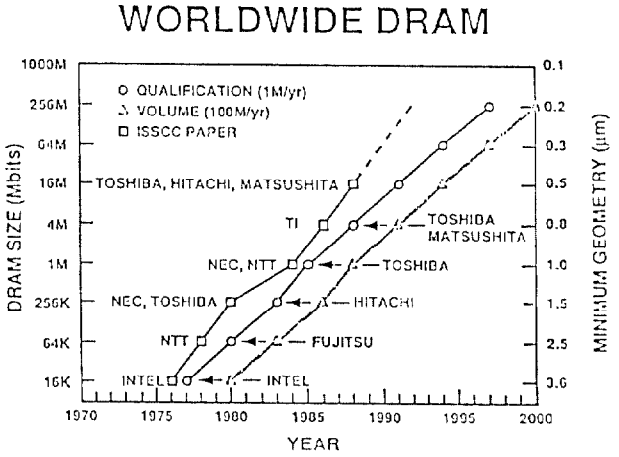

Figure 1.

first announcement of the new device generation by demonstrating laboratory results on the most famous circuit conference in the USA called ISSCC. The circuits published at this conference demonstrate only the feasibility, which does not necessarily mean that the entire circuit is fully operational. The line represented by circles indicates that the 4 Mbit DRAM generation, for example, needed two years to emerge from the laboratory into the pilot production scale. Some further years are necessary - in the case of the 4 Mbit DRAM it took 3 years - to learn how to commercially fabricate large quantities, e.g. more than 1 million pieces per year. The aim is to run as fast as possible through the so-called learning curve because only a few companies which are first in this process will earn money. The time needed to come from the first laboratory example to mass production will even grow in future. This demonstrates the risk which is linked to memory production.

Following the extrapolation of Figure 1 to the year 2000, we will have the 256 Mbit DRAM in mass production, the 1 Gbit DRAM in the pilot phase and first demonstration circuits of at least 4 Gbit. Therefore, the most advanced technology which is available in production in the year 2000 can be characterized by the following parameters:

- minimum geometries: 0.2 microns
- gate insulator thickness: 7 nm
- masking levels: > 20
- junction depth: < 0.1 microns
- number of interconnection levels: 4 or even more
- chip size wafer diameter: 200 mm

The basic and longterm research goals in the field of silicon devices will go in two directions:

1. Further increase of integration density: Laboratory results worldwide indicate that CMOS technology which is and will be the mainstream technology path for highly integrated circuits, can be extended even below 0.1 micron effective general lengths. Devices down to 50 nm and source/drain voltages of 1 V at room temperature are demonstrated. If it is possible to control surface effects on silicon it seems to be possible to use this extreme design rules range for industrial applications. Below 50 nm, so-called quantum devices will become interesting; it is imaginable that silicon can play an important role even in this domain. The conclusion is that the development of the so-called "nanolithography" in the range between 100 and 10 nm should be started early due to the fact that a lithography method needs at least 10 years from basic research to first industrial applications. Competing methods for this pattern range are the extension of X-ray lithography, e-beam and ion beam methods.

2. Multifunctional silicon systems or microsystem technology: The other direction of development with rapidly growing importance is aiming at technologies to integrate entire complex systems. That means, silicon will be the integration basis of "classical" microelectronics of other functions, like sensors and actuators, by combining silicon with other materials monolithically.

The above-mentioned goals in silicon technology can only be achieved by a fundamental further development of all process steps for circuit production. Three categories of problems have to be distinguished:

1. Process steps with a more or less evolutionary development: The presently used technical and physical principles for these process steps will remain unchanged; however, efforts have to be undertaken in the direction of higher sophistication, i.e. with respect to better process performance, higher parameter stability, transfer to larger wafer diameters etc. Examples in this field are ion implantation, some CVD and sputter processes, thermal oxidation etc.

2. Process steps where a revolutionary change by new processes are necessary: The most important examples are lithography, etching, metallization, respectively, interconnections, ultra clean processing and packaging. Especially the pattern generation consisting of lithography and etching is an important bottleneck for future device fabrication, especially in respect to clean room conditions.

3. The central problem for the future which determines how fast semiconductor technologies can be developed and what companies can participate in this severe international competition is the cost reduction of production lines. For example, a production capability of 5000 wafers per week cost in the year 1980 about 100 million DM, increased to approximately 500 million DM by the end of the eighties and will exceed 1 billion DM in the near future. In order to slow down this development, new process and factory concepts are required urgently. The development of stable defect insensitive processes with large process latitude, local clean rooms, increased yield by better factory concepts, in situ on-line computer control and so on, measures to reduce factory costs. Another goal is to increase the flexibility of process lines in order to be able to produce a larger product mix in one fabrication line.

Lithography has the strongest influence on production costs of integrated circuits. The reasons are that lithography is the most expensive single process step, the number of mask levels for an advanced circuit has grown to 20, lithography has the highest clean room requirements, especially in respect to optical lithography, and the strongest influence on circuit yield. Therefore, the selection of a special lithography process for a new semiconductor generation will not be done by comparing the patterning results, like resolution, resist performance, wafer throughput etc. The dominating decision criteria for each new device generation are: Which lithography method provides the lowest costs per chip and is available at a relatively early and small time window on a fully operational basis? That means, this process has to provide an uptime in production of 100%, not considered the regular maintenance sequences.

For the smallest pattern geometries which will be needed by the end of this decade, there are two competing lithography methods: advanced optical lithography and X-ray lithography. The basic scheme of the most advanced optical lithography system, the so-called deep UV excimer wafer stepper is shown in Figure 2; the exposure arrangement of X-ray lithography using parallel synchrotron radiation in the wavelength range between 0.2 and 2 nm can be seen in Figure 3.

The technical parameters of the different development stages of optical lithography related to the DRAM generations are listed in Figure 4. Four Mbit and 16 Mbit DRAM are produced by using the so-called i-line of the mercury spectrum with a wavelength of 365 nm. Here, high numeri-

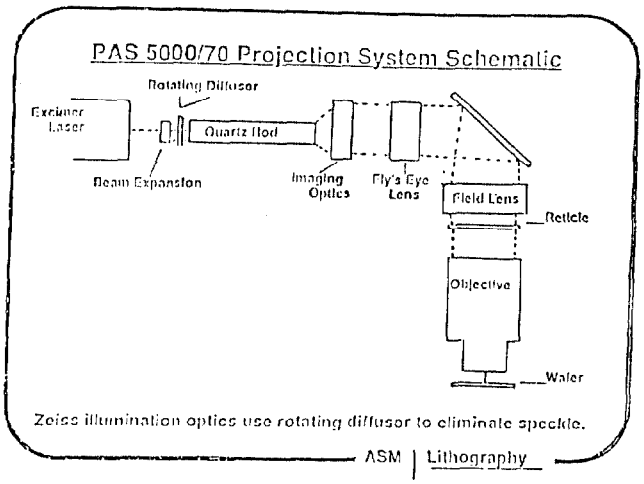

Figure 2.

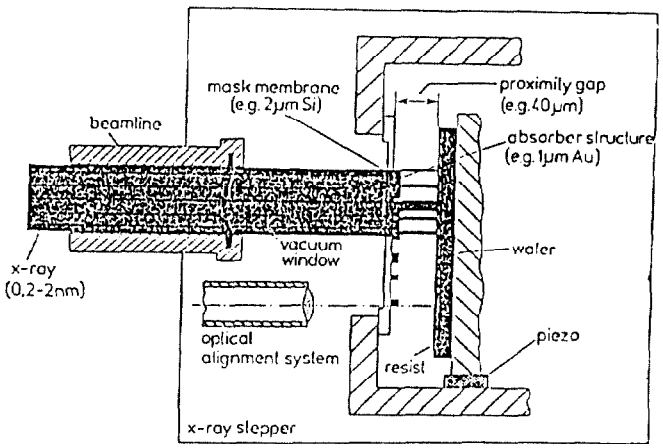

Figure 3.

Future Direction for Optical Lithography

Device Generation	256 k	1M	4M	16M	64M	256M
Minimum Geometry [µm]	2	1.3	0.7	0.5	0.35	0.25
Wafer Size	5"	6"	6"	8"	8"	12"
Lithography	10x g-line (436 nm)	5x g-line (436 nm)	5x i-line (365 nm)	5x i-line (365 nm)	5x DUV (oder i-line + phase-sh.) (248 nm)	?
NA	0.35	0.45 - 0.54	0.48	0.48 - 0.55	≥ 0.55	
DOF [µm]	2.0	1.5	...	1.6 -1.2	< 1.0	
Image field ø [mm]	20	20	25	30	30	
Lens material	quartz glass polychromatic	quartz glass polychromatic	quartz glass polychromatic	quartz glass polychromatic	quartz achromatic	
Lens diameter [mm]	200	200	200	300	300	
Lens Length [mm]	600	600	600	800 - 1000	800 - 1000	

Figure 4.

cal apertures of about 0.5 can be achieved by using polychromatic quartz glass optics. In the deep UV range, e.g., provided by excimer lasers with a wavelength of 248 nm, very complicated and sophisticated achromatic quartz lense systems are needed. Another problem related to deep UV lithography is the relatively poor uptime of excimer lasers and the very small depth of focus < 1 micron. The pattern resolution is improving linearily by increasing the numerical aperture, but simultaneously the depth of focus is decreased quadratically by this parameter. Therefore, people are trying to keep the i-line stepper for producing the 64 DRAM with design rules of 0.35 microns. A solution can be to use the so-called phase shifting mask concept which is illustrated in Figure 5. On the left handside, the conventional exposure scheme with the light wave fronts on mask and wafer are shown. This leads to a poor contrast ratio of the light intensity on top of the resist coated wafer, which is a decisive parameter for the resolution of two lines in the resist. This contrast ratio can be improved by using a π-phase shifter on every second line. It is very

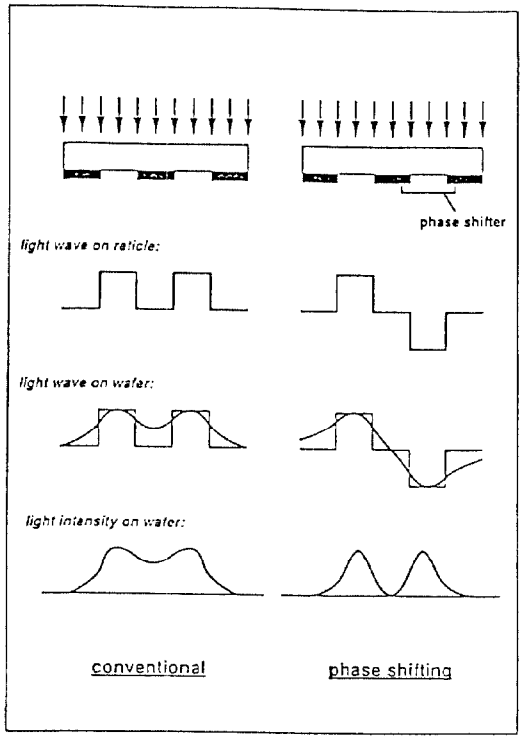

Figure 5.

clear that the resulting mask contrast can be improved significantly without changing any parameter of the exposure arrangement. The quantified improvement calculated by the optical process simulation tool "solid" which was developed at the IMT Berlin is shown in Figure 6, indicating that at a critical dimension, e.g. of 0.25 microns, the improvement of the contrast ratio of about 20%, which can never be used in reasonable applications, will be improved up to excellent 80%. A similar consideration can be made in respect to the depth of focus (illustrated in Figure 7). For example, looking at a contrast ratio of 80%, the depth of focus can be improved from ±0.5 microns up to ±0.9 microns, which would be very important for real applications. However, the fabrication of phase shifting masks is not very simple; problems are the significantly increased writing time, the defect and fault detection and the fact that the mask layout is becoming dependent on the special pattern geometry in the neighbourhood. This means that the design rules cannot be chosen aggressively, the filling degree of the chip area is decreased in critical fields and CAD and mask layouts are becoming dependent to technology.

X-ray lithography using synchrotron radiation has no problems with pattern resolution and depth of focus, which can be seen clearly in Figure 8: On top of a complicated wafer topography without any planarization (optical lithography cannot be applied without a complete planarization), patterns down to 0.2 microns are generated. The control problem of X-ray lithography is a necessity to fabricate the X-ray masks in 1x-scale because in this wavelength range no powerful optical tools like objective lenses are available. Here lies a huge advantage of optical lithography because presently this method can apply a reduction scale in projection of a factor of 5. This advantage will probably become obsolete in future as the chip area is growing very fast. It is not possible to increase the size of lenses with a full compensation of lense defects dramatically. Therefore, the reduction scale of optical lithography will decrease toward 1. If this will be the case, the last advantage compared to X-ray lithography will be lost. In the case of 1x mask fabrication all mask distortions and deviations caused by the mask writing process are fully

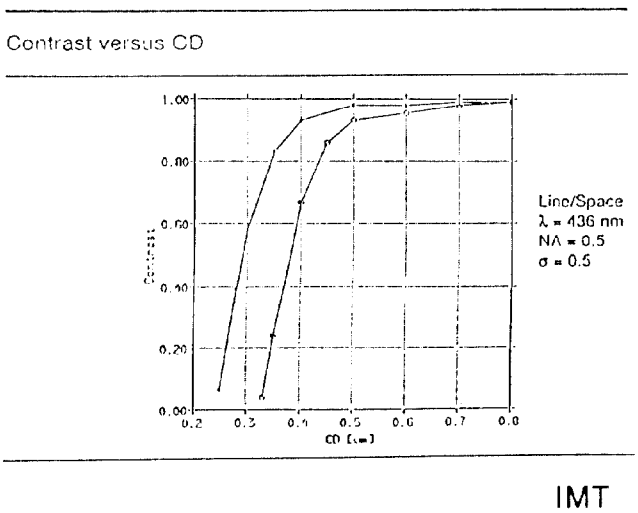

Figure 6.

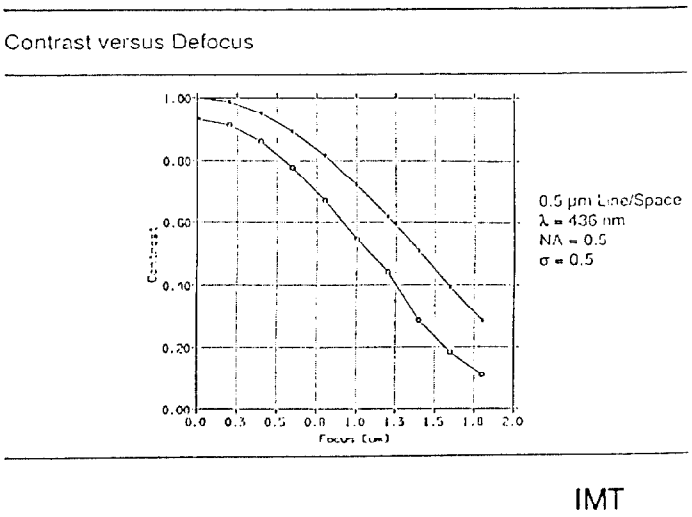

Figure 7.

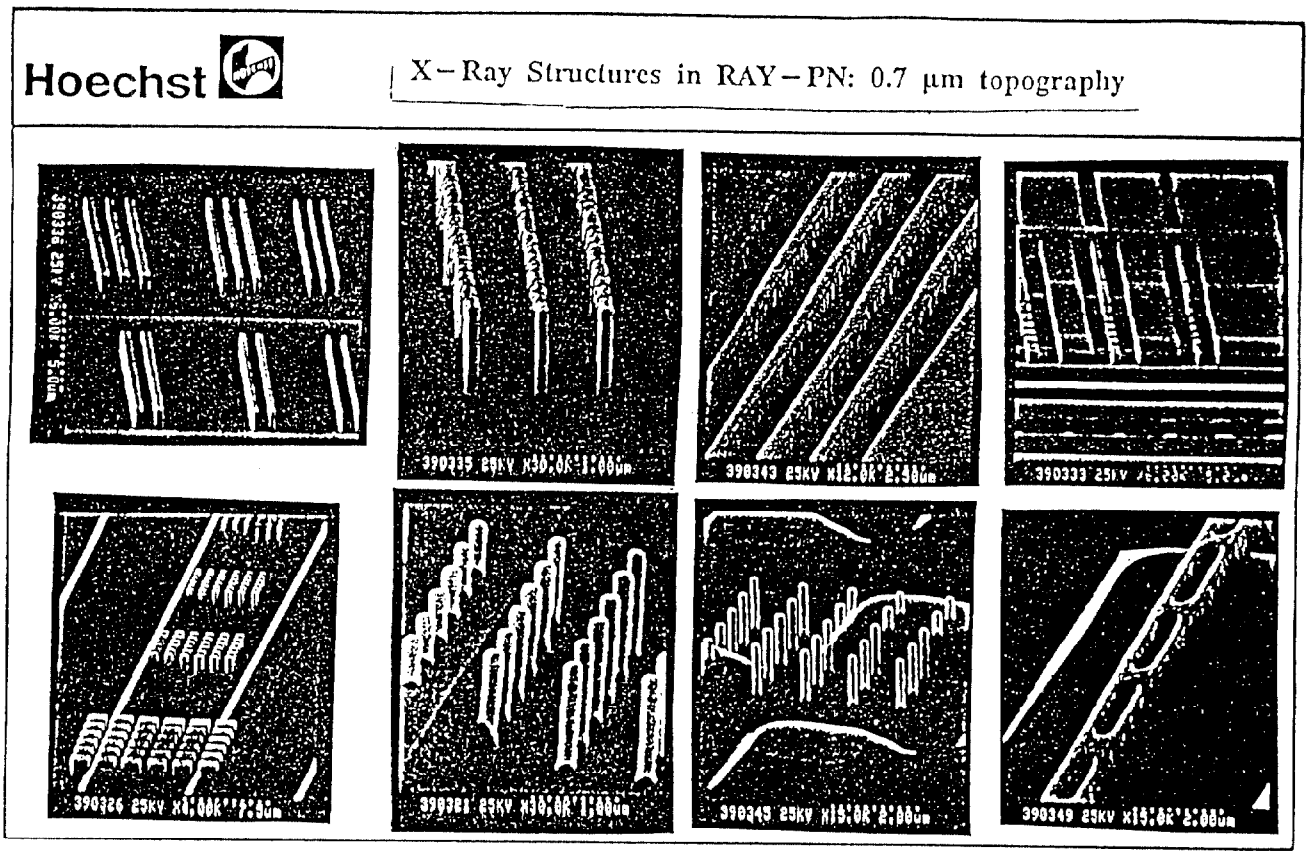

Figure 8.

exposed onto the wafer, i.e. X-ray lithography has problems with the overlay accuracy of different masking levels. Most people agree that the problems related to the 1x-scale, X-ray mask technology can be solved in respect to the 64 Mbit DRAM generation; however, the real question is what lithography method provides the lower production costs and higher yield in respect to the entire process. This question will be answered presently in pilot lines like the ASTC/ALF of IBM in East Fishkill.

In conclusion, the following forecasts can be made from the author's view:

- The 64 Mbit DRAM will be produced optically, however, using i-line steppers in combination with phase shifting masks. The reason for this statement is that optical lithography is an established technology in production and if it is possible to stay with i-line steppers, production tools are already available. In respect to the excimer deep UV lithography, X-ray lithography seems to be already in a more mature stage of development.
- The question of the best method for the 256 Mbit DRAM is completely open, but the better process performance, higher process latitude and circuit yield may turn the scale towards X-ray lithography.
- For the 0.2 micron range ("nanolithography"), a similar strong competition of different techniques can be expected. The most promising candidates for this are X-ray lithography, advanced e-beam writing, e.g. using character projection, and demagnifying ion or electron projection. But in all these fields huge efforts in research and development have to be carried out.