

## THE CONTROLS ARCHITECTURE AND EQUIPMENT ACCESS OF LEP

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*An overview of the LEP controls architecture and a description of the communication and equipment networks are given. The distributed architecture makes use of 57 process computers and 40 consoles located in the LEP underground and surface buildings. The control of all LEP equipment is achieved by 8 and 16 bit microprocessor assemblies driven by real-time kernels and languages. The paper presents in some detail the control of the large variety of LEP equipment including industrial turn-key systems. Particular emphasis will be made to the equipment controls protocol.*

### INTRODUCTION

The CERN Large Electron Positron (LEP) collider ring and the Super Proton Synchrotron (SPS) accelerator use the same protocol for communication over the Equipment Network.

Communication with equipment is performed via the MIL-1553-B bus from Bus Controllers in the VME Process Control Assemblies (PCA). All information is transmitted over the 1553 Bus and the VME Bus using datagrams and various services have been implemented on top of this basic communication mechanism.

Programs in the PCA and in Equipment can send and receive Command/Response (C/R) messages, using a Name Server to provide physical addressing. Equipment can broadcast on their local bus, perform programmable broadcasts globally, send Alarms and request the running of a program in the PCA. In addition an unstructured transparent mode of communication allows industrial equipment to communicate with each other without modification to their software.

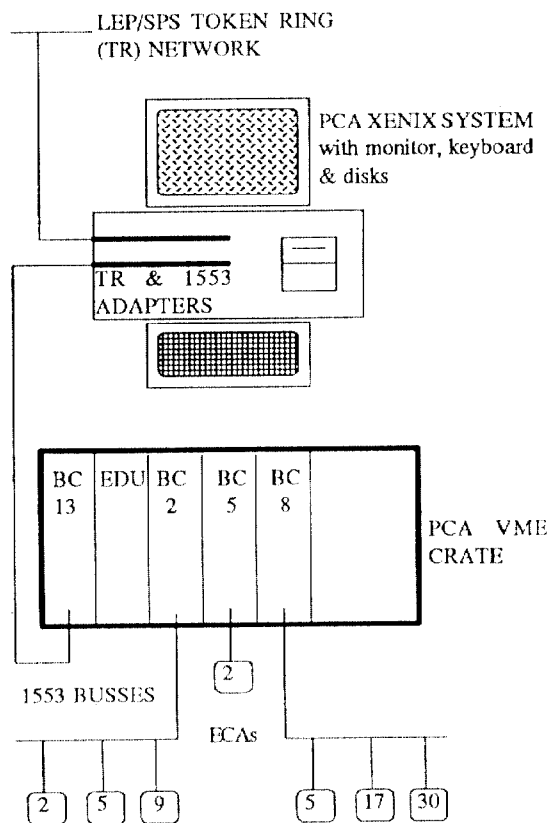
The overall goals have been to keep the software required in the equipment to a minimum (<10k bytes) as many are 8 bit systems, to provide reasonable speeds for large data transfers (10-20k bytes/second) and fast response times (up to 250 local broadcasts per second).

The Equipment Network of the LEP and SPS Accelerators is used to control a very large amount of equipment in the LEP and SPS tunnels and service buildings. Access to the Equipment Network from the main LEP and SPS control room is via the Token-Ring Network [1]. In addition an accelerator synchronization network permits real-time equipment triggering for control and data acquisition.

The basic aim of the communication package for the LEP and SPS has been to have a uniform application software interface that is small and fast, despite the differences in system hardware and software between various implementations.

Communication with the LEP and SPS Equipment Control Assemblies (ECAs) is from a Process Control Assembly (PCA). The MIL-1553-B bus is used as the communication medium. There may be up to 9 bus controllers (BCs) in a PCA and each Bus Controller may be connected to up to 30 Equipment Control Assemblies

### PCA HARDWARE OVERVIEW



Operational systems for LEP consist of IBM/PC compatibles running the SCO XENIX 386 operating system. They are connected to the consoles in the main control room via the LEP/SPS token ring network. The equipment connection is via a 1553 adapter in the PC Xenix system to a 1553 Bus Controller in the PCA VME crate. The equipment is connected to other 1553 Bus Controllers in this PCA VME crate. The Equipment Directory Unit (EDU) in the PCA VME crate performs a Name Server function, looking up the physical address of a piece of equipment from the name used by application software running in the PC Xenix system.

Development systems for LEP applications often use a serial link between the PC XENIX system and the PCA VME crate instead of a 1553 link.

In the SPS, older systems consist of a NorskData NORD 100 minicomputer connected via a special NORD 100 - VME interface card to a PCA VME chassis as described above.

Some recent SPS system are based on a PC Xenix system with a PC1553 adapter card running the BC and EDU software so that there

is no need for the PCA VME crate. Therefore these BCEDU system can only be connected directly to 30 ECAs.

### ECA HARDWARE OVERVIEW

Equipment Control Assemblies of many types are supported. The Remote Terminal Interface (RTI) cards to connect an ECA to the 1553 bus are available for various busses.

- 1) G64 bus RTI cards for Zilog Z80, Motorola 6809, 68000 and 68010 based Microprocessor systems.
- 2) VME bus RTI cards for 68000/68010/68020 systems.
- 3) MICENE bus RTI cards for Texas 99000 systems.
- 4) IBM PC bus 1553 adapter card incorporating a 68010 processor and implementing both Bus Controller and Remote Terminal Interface protocols. It is this card that is used in the PC Xenix systems

### PCA SOFTWARE OVERVIEW

LEPPC Xenix system are connected to the Token Ring network via TCP/IP protocols. Application programs to access the token ring network use Remote Procedure Calls (RPCs), automatically produced with the Network Compiler (nc), in such a way that C programs can perform network accesses transparently. Equipment access from the PCAs is performed principally via the EQUIP and NAMES procedures supplied in the C Equip Library.

Programs to access the token ring and equipment networks may also be written in NODAL. NODAL is similar to BASIC in that it is interactive but it incorporates many extra features to allow multi-tasking and program execution on remote computers via a network.

The NORD 100s in the SPS environment access the TITN network used in the SPS and ECAs only from NODAL.

There is a gateway between the LEP/SPS token ring network and the old TITN SPS network so that LEP/SPS consoles can access equipment connected to the SPS NORD 100s.

### ECA SOFTWARE OVERVIEW

Various software interfaces between Equipment Control Assemblies and the Equipment Network have been developed by the LEP/SPS controls group.

- 1) A simple 'polling' interface for Motorola 6809 microprocessor systems using the G64 bus. This interface is written in the language PASCAL. These systems often run the FLEX operating systems and the interface is compatible with FLEX although they may also be used standalone without an operating system.
- 2) A PASCAL interrupt driven interface for standalone G64 6809 systems or G64 6809 systems running the FLEX operating system.
- 3) A PASCAL multi-tasking interface using the AMX real-time executive for standalone G64 6809 systems or G64 6809 systems running the FLEX operating system.
- 4) A multi-tasking interface written in Modula-2 for 68000 and 68010 systems. This can be used from Modula-2, PASCAL and C.
- 5) A multi-tasking interface written in C for OS9 68000/68010/68020 systems. This is implemented as an OS9 device driver.

In addition LEP and SPS Equipment designers have written interfaces for:

- 1) Zilog Z80 systems running CP/M using the G64 bus. The interface is written in Turbo PASCAL.
- 2) NODAL running in Texas 99000 systems using the MICENE bus. The interface itself is written in assembly language.

### COMMUNICATION IN THE EQUIPMENT NETWORK

Communication in the equipment network is performed by the transmission of packets (i.e. datagrams). Packets have the same format on the 1553 Bus and the VME bus. Each packet has a 16 byte packet header followed by up to 240 bytes of data, giving a maximum packet size of 256 bytes. The header consists of:

```

BYTECOUNT (2 bytes)
VERSION (1 byte)
(spare) (1 byte)
SOURCE ADDRESS (2 bytes)
DESTINATION ADDRESS (2 bytes)
PACKET TYPE (1 byte)
SEQUENCE (1 byte)
SOURCE TRANSPORT (2 bytes)
DESTINATION TRANSPORT (2 bytes)
SESSION ERROR (1 byte)
(spare) (1 byte)

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The BYTECOUNT gives the total packet length in bytes including the header.

The VERSION is used to check if the sender and receiver of a packet are running the same version of the communication software and allows extra features to be added in later versions while maintaining compatibility with older versions.

The DESTINATION ADDRESS is used for routing a packet to its destination and the SOURCE ADDRESS allows the receiving system to reply to the sender by simply swapping the source and destination addresses. The high byte of an address specifies the VME module number of a processor in the Process Control Assembly. Generally VME module numbers are between 1 and 31. The low byte specifies the sub address with respect to the VME module. Equipment Control Assemblies connected via a 1553 RTI card have addresses between 1 and 31 while by convention 255 is used to address the VME module itself. In this way every element of a Process Control Assembly and every ECA can be uniquely addressed.

The PACKET TYPE is used to differentiate the various services provided. The most important packet types are:

OpenEquip	- Asks EDU for ECA address (C/R)
ReturnOpen	- EDU returns address of ECA with this
WriteData	- Data for C/R service
CloseEquip	- Informs EDU that C/R finished
OpenTransparent	- Asks EDU for ECA address (Transparent)
TransparentData	- Data for Transparent Service
CloseTransparent	- Informs EDU that Transparent finished
Alarm	- for sending alarms
BroadcastData	- Data for Broadcast Service
Multicast	- Request a multicast service
MulticastData	- Data for Multicast Service
ServiceRequest	- Service Request
ModuleInfo	- At startup gives server addresses
RTInfo	- At startup gives ECA addresses
Bounce	- Low level test packet
Error	- Returned to sender of failed packet

### PACKET TRANSMISSION OVER THE 1553 BUS

The 1553 Bus is a 2 wire serial multidrop [4]. The data bits are encoded in Manchester II biphase code. For distances up to 400 metres it can run at 1 Megabit per second, whereas for distances up to 2 km it can be run at 125 kilobits per second. With the aid of repeaters even distances of 30 km have been covered for the LEP and SPS.

A Bus Controller manages all communication on the bus and up to 30 remote terminal interfaces may be connected. Normally there is one RTI card in each Equipment Control Assembly. Only the Bus Controller can start a data transfer.

#### Basic 1553 Data Transfers

When writing data to an RTI the Bus Controller sends a 1553 command word followed by up to 32 16 bit words of parity checked data. The 1553 command contains an RTI address, word count, direction indicator (read or write) and a 5 bit field to indicate where the data should go in the RTI memory. Only the addressed RTI receives the 1553 command word and data. The RTI hardware checks that the 1553 command word is legal, that the correct number of words were received and that there were no parity errors. In addition the hardware checks that the bits of each word were correctly Manchester II coded. The hardware puts the data in the correct RTI memory locations and returns a 1553 status word to the Bus Controller indicating the success of the transfer.

To read data from an RTI the Bus Controller sends a 1553 command word specifying the number of words, that it is a read and the memory area to read. The RTI hardware checks the command and sends the data followed by the 1553 status word. The Bus Controller hardware checks the parity and Manchester II coding of the data it receives.

#### 1553 Buffers

The RTI cards used in the LEP/SPS control system have additional hardware to the basic minimum required to implement the 1553 bus protocol. There are two 256 byte or larger First In First Out Buffers and a Control Status Register (CSR). One buffer is used as a packet receive buffer and the other as packet transmit buffer. The RTI Control Status Register can be written and read both by the Bus Controller and the ECA processor. The bits in the CSR allow the BC and ECA to:

- 1) Indicate receive buffer full/empty
- 2) Indicate transmit buffer full/empty
- 3) Reset transmit/receive buffer pointers
- 4) Interrupt the ECA processor
- 5) Modify and monitor the state of the RTI card

To send a packet to the ECA the Bus Controller checks that the receive buffer is empty, clears the receive buffer pointer, transfers the data in up to 4 32 word transfers, i.e. up to 256 bytes, sets the receive buffer full bit and the ECA processor interrupt bit. The ECA gets the interrupt, sees the receive buffer is full and reads the data from the receive FIFO.

For a Bus Controller to receive packets from the ECAs it must continually poll all the ECAs on the 1553 bus, checking if any have the transmit buffer full bit set. This task occupies almost 100%

of the Bus Controllers processing time. Normally the Bus Controller will only poll the ECAs it knows are connected but periodically it will check all the possible ECA addresses (1 to 30). If a new ECA is found then it will be added to the list of ECAs to be polled frequently. The Bus Controller sends an alarm to the Alarm server if an ECA is disconnected or reconnected. In addition various other states are monitored.

All packets from an ECA pass by the Bus Controller, even if their destination is another ECA on the same 1553 bus.

#### 1553 Diagnostics

Each Bus Controller keeps statistics for the number of packet transfers and errors that occur. In addition a Bus Controller can give a hardware reset to the RTI card and processor of any ECA which is setup for this facility, without any dependence on the state of the ECA software. This is invaluable when the ECA is in an inaccessible tunnel or 30 kms away.

### PERFORMANCE

The time for a command/response transaction to send one real from a NODAL application program running on a PCA Xenix system to a G64 6809 ECA is 60ms. 10 kilobytes of data can be sent at 20 kilobytes per second.

A 10 kilobyte command/response transaction from one G64 6809 ECA to another similar ECA on the same 1553 bus is performed at 24 kilobytes per second. A G64 6809 ECA can broadcast 1 byte of data to all the other ECAs on its 1553 bus 250 times per second.

The interface library for a G64 6809 ECA providing the command/response, transparent, alarm and broadcast services is smaller than 10 kilobytes. This is important in a 6809 system because they can only address 64 kilobytes of memory.

### CONCLUSION

The equipment network of the LEP/SPS control system provides a variety of services enabling many types of Equipment Control Assemblies to be accessed from application programs. Application programs may run in different environments but they all have the same software interface towards the equipment network allowing portability between current and future configurations of the LEP/SPS control system. The speed of the equipment network, despite the long distances and number of Equipment Control Assemblies involved should ensure that bottlenecks do not occur. The interface software is relatively compact so that small, inexpensive microprocessor systems can be interfaced.

### REFERENCES

- [1] R. Rausch. Real Time Control Networks for the LEP and SPS Accelerators "Europhysics Conference on Control Systems for Experimental Physics" - Villars-sur-Ollon, Switzerland, 28 September 1987.
- [2] THE LEP/SPS ACCESS TO EQUIPMENT MANUAL, The LEP/SPS Controls Group, SPS/ACC/Note 85-23, LEP Controls Note No. 54 rev., CERN.
- [3] A Proposed Standard for Binary Floating-Point Arithmetic, Draft 8.0 of IEEE Task P754, 1981, IEEE.
- [4] BUS MULTIPPOINTS MIL-1553B POUR LE CONTROLE DES EQUIPMENTS LEP ET SPS MANUEL DE L'UTILISATEUR, D. Francart, R. Rausch, J.M. Sainson et R. Wilhelm, SPS/ACC/Note/85-26, LEP Controls Note No.56, CERN.