MEASUREMENTS ON AN A/D INTERFACE USED IN THE POWER SUPPLY CONTROL SYSTEM OF THE MAIN DIPOLES OF CNAO

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Abstract

CNAO, the Italian Centre of Oncological Hadrontherapy located in Pavia, is in its final step of construction and is about to be fully operative. It is based on a synchrotron that can accelerate protons up to 250 MeV and carbon ions up to 400 MeV/u for the treatment of patients. In this paper we describe an A/D interface, used in the power supply control system of the synchrotron main dipoles, called B-Train. The field is measured in a dedicated dipole connected in series with the sixteen ones of the synchrotron and is then fed back to the power supply. The field is obtained integrating and digitizing the voltage induced on a pickup coil inserted in the gap of the seventeenth dipole. The A/D interface under study is based on a 64-channel current to frequency converter ASIC, in CMOS 0.35 μm technology, followed by a counter and uses a recycling integrator technique. The digital signal obtained is then used to generate a feedback signal for control system of the dipoles power supply. We present the electronic structure, the lab measurements and the behaviour for various setups of the A/D interface described.

INTRODUCTION

CNAO is an advanced research and hospital centre which is under construction in Pavia and is expected to be fully operative within 2009. The main goal of this project is to introduce hadrontherapy in Italy to treat patients affected by cancer. The hadrontherapy [1] involves the use of hadron beams instead of X rays (used in the most common radiotherapy techniques) in order to ionize DNA molecules and kill the diseased cells. The Hadron beam's energy release curve through the matter is affected by Bragg peak phenomenon resulting in a concentration of ionizing power in a volume of the order of $1mm^3$, allowing to damage diseased cells while preserving the healthy cells which are near the treatment area.

ACCELERATOR LAYOUT

The CNAO accelerator is designed to employ proton beams up to 250 MeV and carbon ion beams up to 400 MeV/u [1]. Protons or carbon ions are collected from the sources, accelerated up to 7 MeV/u and injected into a circular synchrotron of about 25 m of diameter. They are collimated and accelerated and then directed to the extraction lines. Four independent extraction lines lead to three different treatment rooms, which allow to parallelize treatments. The typical magnetic cycle designed for the synchrotron is reported in Fig. 1. It lasts about 2 second, which is the duration of a single treatment cycle.

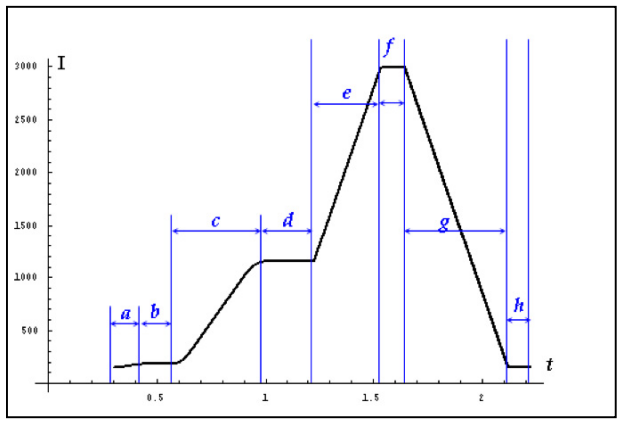

Figure 1: CNAO synchrotron magnetic cycle.

The first plateau (*b*) represents the injection phase, the following ramp (*c*) is used during the acceleration phase and the second plateau (*d*) is the beam extraction phase.

The following phases are needed to cycle the magnets for the next treatment cycle.

THE B-TRAIN SYSTEM

The 16 dipoles of the CNAO synchrotron are connected in series to a single power supply. Measurements of the magnetic field vs. magnet current characteristic showed, for the typical magnetic cycle, that the field lags the current by few ‰ with a characteristic time of the order of several hundred msec, impacting the treatment efficiency.

For this reason a dedicated system, similar to the field control system of PS at CERN and nicknamed B-train [2], has been developed to control the dipole power supply using a magnetic field reference signal instead of the usual current signal.

The B-train system provides a real time accurate measurement of the magnetic field in the synchrotron dipole magnets (Tab.1), which is used to generate a feedback signal for the power supply.

Table 1: Dipole Specifications

Parameter	Value
Maximum magnetic field	1.6 T
Maximum Dipole Current	3000 A
Magnetic Length	1677.2 mm
Slew Rate	3 T/s

It is used also to control the frequency of the accelerating cavity of the synchrotron, although, in this

paper, we mainly focus on the bending magnets application.

The CNAO B-train system [3] block diagram is shown in Fig. 2. A digital measurement of the magnetic field is obtained by integrating and digitizing the voltage induced on the pickup coil inserted in the gap of a spare 17th dipole, connected in series with the synchrotron dipoles.

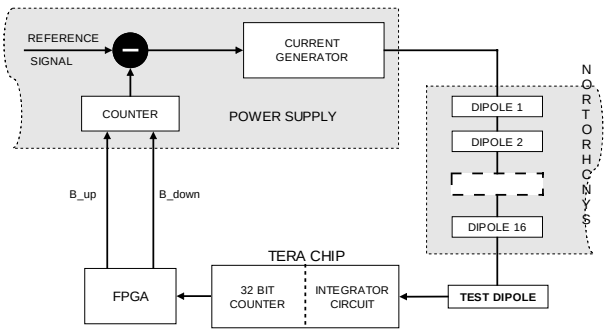

Figure 2: B-train block diagram.

The control system is driven by an FPGA which generates the control signals for the power supply and manages the digital magnetic fields readings, provided by an A/D interface. The digitized readings are translated by the FPGA into two digital single bit signals, *B_up* and *B_down*, which correspond respectively to an increment and decrement of the magnetic field of a given step. This information is then used by the power supply to manage the output current.

Since the magnetic field readings obtained through the pickup coil are differential measurements, the B-Train system is equipped with a nuclear magnetic resonance (NMR) probe, which is used to obtain the absolute value of the magnetic field at the beginning of every magnetic cycle and in the plateau (*f*) of Fig. 1, in order to calibrate the system.

To fulfil the role of the A/D interface discussed above, an ASIC chip in CMOS 0.35μm technology has been selected. The chip, called TERA, has been designed by INFN-Torino [4].

It is currently used for another application inside the beam diagnostics system of the CNAO project. Basically it is a 64-channel current to frequency converter followed by a 32 bit counter.

Each channel is independent and uses a charge balancing technique in order to nullify any deadtime during his working state. As can be seen from the diagram in Fig. 3, the input current which flows through an external impedance is integrated by a capacity C_{int} in parallel with an Operational Tranconductance Amplifier.

Two comparators with fixed thresholds are then used to drive a pulse generator which is connected to the output counter. The pulse generator drives also the charge balancing circuit: for every pulse generated, this circuit subtracts a fixed amount of charge from C_{int}, avoiding overloads and restoring the charge balance.

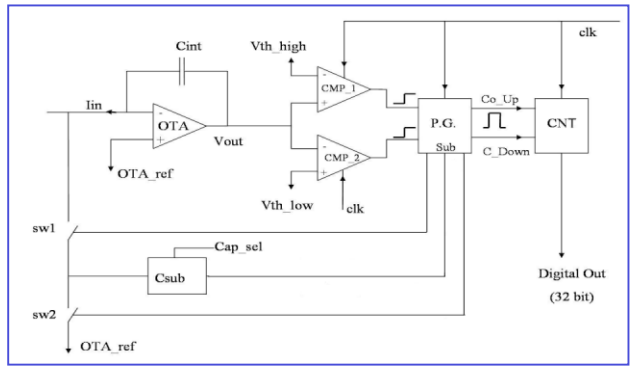

Figure 3: TERA chip block diagram.

The input-output relation is given by:

$$f = \frac{I_{in}}{Q_c} \qquad (1)$$

where f is the numbers of counts per second of the output counter, I_{in} is the input current and Q_c is the charge subtracted every cycle from C_{int}, via the balancing circuit.

The latter, which represents the quantization step, can be selected between 50 fC and 350 fC, with 50 fC steps.

MEASUREMENTS

The pickup coil used for magnetic readings provides a voltage output given by:

$$V(t) = -\frac{dB(t)}{dt} \cdot N \cdot S \qquad (2)$$

where NS=1.6 m^2, so that the maximum voltage for the given magnet slew rate is ~|4.8| Volt.

Bench measurements have been performed to evaluate the compatibility of the chip TERA with B-Train requirements reported in Tab. 2.

Table 2: B-train requirements

Parameter	Value
B-field measurements resolution	0.1 G
A/D conversion frequency	300 ks/s
Minimum System Bandwidth	10 kHz

The experimental setup is reported in Fig. 4: an FPGA module installed in a PXI system with an embedded controller is connected to the TERA chip via an optoisolator interface, in order to guarantee the electric isolation of the chip.

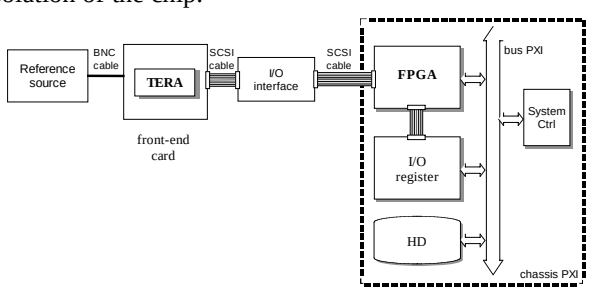

Figure 4: Measurement setup.

The FPGA receives output data from the chip via a 16 bit dedicated line and send them to an I/O interface (NI6534) for data storage and analysis. The entire measurement system has been controlled with dedicated LabView routines. The output of the pickup coil has been simulated with a HP3245A reference source connected to the input of the chip via an input resistance R_{in}.

The choice of a proper experimental setup involves considerations about:

- maximum input current
- resolution of the A/D conversion
- resistance of the pickup coil
- system bandwidth

These points put limits on the choice of R_{in} and Q_c.

The maximum input current can be derived from equation (1) and is of the order of few μA, considering that the maximum counter frequency is 20 MHz, which yields to R_{in} in the order of few megaohm.

An input resistance of order of magnitudes larger than the pickup coil resistence (r=1.6KΩ) also helps to minimize the effects due to thermal variation in the coil and if needed can be easily kept at a constant temperature.

Quantization error in the analog to digital conversion can be estimated by integrating eq. (2), which leads to:

$$\pm \Delta B = \mp \frac{R_{in}}{N \cdot S} \cdot Q_c$$

The B-Train system is aimed at realizing a closed loop controller for the dipoles power supply. An evaluation of errors due to the finite bandwidth of the controller device has been estimated, assuming a single pole low pass transfer function for the TERA chip. It led to an accettable minimum bandwidth of 10 KHz to reproduce the typical ramp current with an error smaller than 5ppm.

System bandwidth measurements for different input resistances ranging from 100 kΩ to 80 MΩ are reported in Fig. 5. As a result, values of R_{in}=10 MΩ and a Q_c=200 fC have been selected as compatible with requirements. This leads to a value of 0.0125G for a single output count.

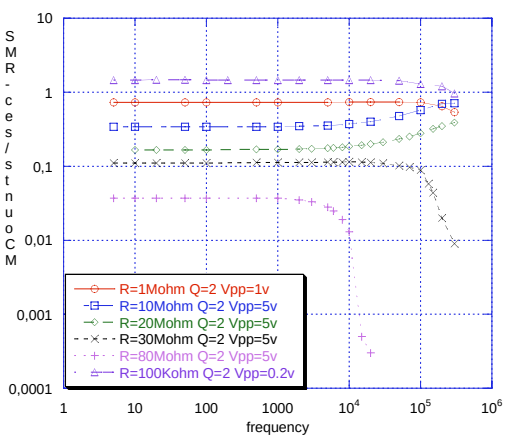

Figure 5: Bandwidth measurements.

Measurements on I/O dynamics show that the chip has a linear behavior over four decades,, working from few hundreds pA to few μA inputs. The maximum limit is due to the chip maximum frequency (f_{max}=20MHz), while the minimum is related to the noise, as it will discussed below. Measurements show differences between positive and negative current dynamics. Using our setup, the rate of counts for negative inputs are roughly 6% less than for positive inputs. This can be due to different behaviors in the charge subtraction circuit for positive and negative currents, but can be calibrated and corrected by software.

In Fig. 6 is reported the noise power spectrum obtained for a small input current. The 1/f trend given by *flicker noise* is dominant up to ~0.1Hz while white noise is dominant at higher frequencies. On top there are some noise peaks, which appear at frequencies in a binary sequence. Such signature can be due to a cross-talk between the digital output of the chip counter and the analog integrating front-end. It may compromise the conversion precision for our application, bringing it to a relative magnitude value of roughly 10^{-4}.

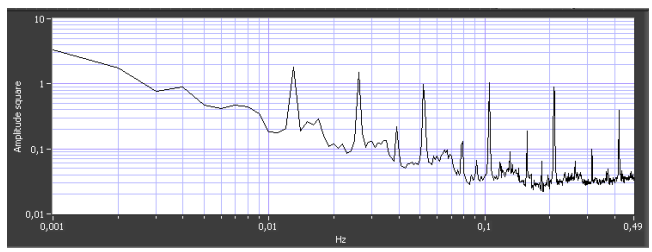

Figure 6: Noise power spectral density.

CONCLUSION

The chip TERA should be implemented in the B-Train system for integration and digital conversion of the voltage signal provided by a pickup coil inserted in one of the CNAO synchrotron dipoles. It has been characterized and tested with various setups to compare its performance with system requirements. While the frequency response and the A/D conversion frequency are adequate, its conversion resolution is up to two order of magnitude higher then the acceptable value.

This is due to cross-talk noise in the chip between the analog and digital sections.

A new TERA version is currently under test to verify its compatibility with the B-Train requirements also with respect to the cross-talk noise. With the new version of the chip, it is possible to read the single incremental counts and accumulate them at the FPGA level, bypassing the digital counter, to avoid the cross-talk noise.

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