# DIGITAL LOW LEVEL RF

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*Abstract*

The demand on high stability and precision on the RF voltage for modern accelerators, as well as better diagnostics, maintenance and flexibility is driving the community to develop Digital Low Level RF systems (DLLRF) for both linear accelerators and synchrotrons. The state of the art in digital technologies applied to DLLRF systems is reviewed; different designs developed or in development at various laboratories are surveyed.

## INTRODUCTION

Low Level Radio Frequency (LLRF) improves accelerator performance by stabilising RF voltages and the beam via feedback loops and feedforward (with/without beam in the loop). Demands on RF accuracy, stability and reproducibility make LLRF an essential ingredient of accelerator design; coupled to digital and telecommunication technology progress over the last 10 years, they are the reason for recent Digital LLRF (DLLRF) developments. The success of the ICFA LLRF05 workshop [1] and recent reviews on DLLRF aspects [2,3,4], confirm the great interest for DLLRF. In this paper, DLLRF systems are defined as those with important LLRF features achieved digitally, even if there are other analogue parts.

### *From Analogue to Digital*

First use of microcontrollers for LLRF in accelerators go back to the late '70s [5,6] and was limited to pre-calculating control values. An example was the frequency program to control a Voltage Controlled Oscillator (VCO) in circular machines [5] from the measured magnetic field. The first mixed analogue-digital systems for circular machines date to the '80s [7,8], when VCOs were replaced by high accuracy and stability Numerically Controlled Oscillators, often structured in master/slave schemes. Digital filters were also introduced in feedback loops [9]. Further steps included implementing controllers in Digital Signal Processors (DSPs) and programmable logic devices [10,11]. Analogue LLRF systems are still used in new accelerators [12,13].

### *DLLRF Advantages and Consequences*

DLLRF has many advantages over analogue LLRF. Naturally flexible and reconfigurable solely via software, it permits the upgrade to new requirements and operating modes [14]. Remotely controllable, DLLRF supports multi-user operation better than analogue LLRF, as more parameters can be changed on a per-user basis. Another plus is reproducibility and absence of drifts. DLLRF allows using built-in diagnostics, essential for system optimisation, troubleshooting, low down-time and operations close to the machine performance limits [15]. DLLRF can handle special situations, e.g. cavity quench detection/recovery [16]. Cavity vector sum calibration, sophisticated algorithms and modern control methods are easier to implement than in analogue LLRF.

Drawbacks over analogue LLRF include a longer group delay, which might limit control performances; technology improvements are reducing this drawback. Analogue LLRF is often less sensitive to radiation effects.

DLLRF changed the LLRF expert professional figure: analogue expertise is complemented by high-speed digital design and DSP/FPGA software skills. DLLRF-to-infrastructure responsibility separation is becoming blurred: for instance, timing decoding may occur on the DLLRF side [17,18]. The software effort is also relevant.

## STATE-OF-THE-ART: SYSTEM DESIGN

I review here the latest trends and typical choices for DLLRF systems and their enabling technologies. Technical choices depend on performance requirements, accelerator type and on factors such as local expertise, control infrastructure and time/resource constraints.

### *Custom Vs. COTS Modules*

An important choice is whether to build custom modules or buy Commercial-of-The-Shelf (COTS) modules for the LLRF-specific part. Currently most DLLRF systems include RF-custom modules.

COTS boards allow easier project planning. COTS systems are used in the J-PARC linac [19] and RHIC [20]. In the latter, custom boards will replace COTS ones [18].

Custom boards can target the needs of most accelerators on a given site by a common modular architecture and tailored software, which reduce maintenance efforts. In addition, maintaining the in-house knowledge usually pays off, for example in coping with material obsolescence. The downside is a possibly steep learning curve and the designer's need to be ready to tackle unexpected snags. Evaluation boards are useful for rapid system prototyping [21]. The custom design burden may be eased by inter-lab collaborations, e.g. SNS. Industry/DLLRF interaction is less developed than for diagnostics or orbit feedback. BNL [18] and CERN's PS Complex [17] are developing custom solutions to be applied to different accelerators. LHC will have a custom DLLRF with over 300 custom cards of 23 types [22].

### *System Architecture*

DLLRF control architecture often depends on the existing laboratory infrastructure and is not freely chosen. From a software viewpoint, there are two approaches to the Controls Standard Model [23]: 1) mapping single process variables to the higher level or 2) grouping them in devices. The first approach is used in EPICS (Experimental Physics & Industrial Control System); the second is used for instance in CERN's controls

infrastructure [24]. From a hardware viewpoint, there are two approaches: the novel Network-Attached Device (NAD) [25] and the traditional one using crates as platforms. NADs are connected directly to the network; the SNS linac interim system is a DLLRF NAD [26]. The traditional approach relies on front ends made of crates and front-end computers running real-time kernels. Figure 1 shows CERN's controls infrastructure: a 3-tier distributed model provides clear separation of Graphical User Interface (GUI) from server and device tiers.

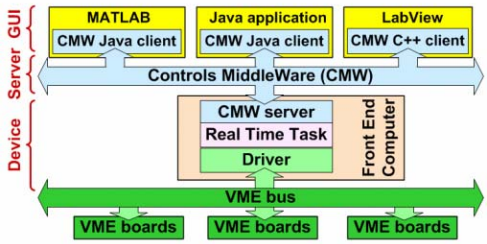


Figure 1: CERN's controls infrastructure.

For hardware platforms, PCI joins established LLRF multidrop parallel bus standards (VME, VXI) [19]. Gigabit serial busses (e.g. ATCA [27]) are new options.

## *Use of DSPs and FPGAs*

DSPs and FPGAs perform fast signal processing [28]; FGPAs are also used for general logic and interfacing.

Most DSPs are ADI- or TI-families, floating-point products, as the high dynamic range benefits win over cost considerations. DSPs provide sequential and parallel processing, owing to powerful architectures, e.g. Single Input Multiple Data (SIMD). DSP code is typically interrupt-driven and does not include a Real Time Operating System (RTOS), as RTOS features (e.g. multi-threading) do not compensate processing and resource overheads. High-level language DSP programming is coupled to assembly coding for processing optimisation or to access otherwise unavailable hardware features. Network licences for development tools are not available for all DSPs and single licenses are mostly used.

FPGAs belong usually to Xilinx or Altera families and provide massive parallel processing. Recent high-processing level families include an embedded processor as hard (e.g. PowerPC 405 on Xilinx Virtex) or soft core (Altera NIOS). Floating point is still rarely used as its performance is slow. FPGA are programmed by different languages and methods: text, proprietary, VHDL/Verilog, higher level (ex: VisualElite [29]). FPGA development tools are available mostly through network licences.

Figure 2 shows the layout of a typical DLLRF board including DSP and FPGA. A system may be composed of several similar boards; daughtercards (dashed boxes), are used with the aim of starting from building blocks and of customising the system with appropriate FPGA/DSP coding [14]. In linacs sometimes only FPGAs are used owing to the low latency required by cavity servoing [30-32]; in circular machines DSPs are usually included, for easier implementation of complex algorithms and control-intensive programs [10,17,33,34].

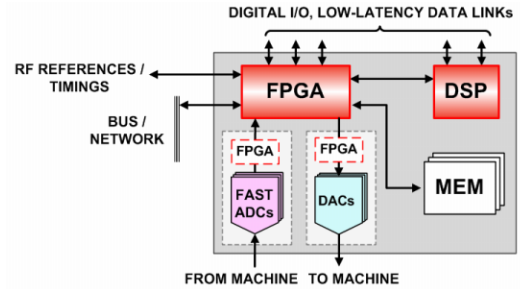


Figure 2: General DLLRF board with DSP and FPGA.

Several buses and ADCs/DACs may be connected to the same FPGA, thanks to the high number of I/O pins in powerful FPGAs (1170 in Altera Stratix II). ADCs/DACs may be hosted on daughtercards where additional FPGAs perform data processing and reduction. The memory type is Static RAM (SRAM) and Dynamic RAM (DRAM); SRAM have larger width and easier interfacing, while DRAM have bigger depth in smaller die size but present more complex interfacing. The main board FPGA interfaces with DSP, memory, external bus/network and daughtercards and interfaces them all together, handling coherent data set presentation (e.g. I/Q). A synchronous design should be used, by dividing the FPGA into separate clock regions and re-synchronising as data cross clock boundaries. Remote DSP/FPGA configuration and programming should be made available. System shrinkage on moving to digital increased the functionality available on one board and the number of connections needed. Low-latency point-to-point data links are used for system interconnects; serial links with clock-data recovery help reduce the number of traces (compared to parallel links) and eliminate clock-to-data skew. Differential-transmission standards are used (e.g. RapidIO and Infiniband). FPGA protocols include Aurora (Xilinx) and SerialLite (Altera). Optical links are extensively used. Tagged clocks, i.e. including width-modulated pulses, are used for synchronous system setup and data acquisition [17]. DSPs provide parallel and serial links that can be routed/multiplexed via FPGAs.

## *Digital I and Q Detection*

RF signals are usually acquired and processed in rectangular coordinates, I and Q. I/Q detection, processing and control are particularly suited to digital systems [3,35]. I discuss two digital I/Q detection schemes: I/Q sampling and Digital Down Conversion (DDC). Figure 3 shows I/Q sampling basics. The RF signal is sampled after a down-conversion step, which may be removed for a fast ADC; in this case, the scheme is called direct I/Q sampling. The ADC is clocked at a frequency of $4 \cdot f_{IF}$ (the Intermediate Frequency) and (I,Q) data can be retrieved from sampled data by a simple demultiplexer and sign reversal scheme. Owing to the short latency, this scheme is used in cavity field detection for linear accelerators [31]; several input signals can also be multiplexed into the same ADC with corresponding loss in bandwidth resolution and latency [36]. Digital I/Q detection suffers from fast ADCs differential non-

linearity; increasing the number of samples per synchronous period may improve the resolution [37].

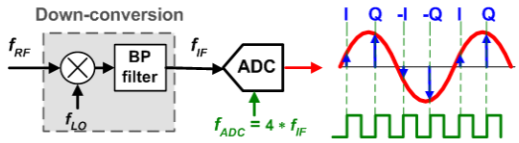


Figure 3: I/Q sampling.

For low RF frequencies ($f_{RF} < 1/3\ f_{ADC}$), the RF signals can be digitized directly and I/Q detection is most conveniently achieved by FPGA-implemented DDCs [28] with digital mixers, frequency agile quadrature NCOs and digital decimating low-pass filters. This improves the S/N ratio and provides data reduction. COTS telecom DDCs are used in diagnostics but not in feedback applications, owing to their long group delay; their strong out-of-band attenuation is not of use in feedback systems.

Finally, from a signal processing viewpoint I/Q sampling is a special DDC case, where the ease of implementation balances the lack of flexibility.

## STATE-OF-THE-ART: ALGORITHMS

I mostly describe known algorithms, now applicable, thanks to digital technology progress, in real-time control and feedback tasks. Algorithms are often optimised and simulated via high-level tools (e.g. Matlab) [15,32,38].

### *Efficient Algorithm Implementation*

Algorithms optimisation (speed, resolution, resources), depends on numerical format (fixed/floating point) and processing structure (serial/parallel). I outline biquads and trigonometric functions, greatly used in DLLRF.

Second-order blocks (biquads), made of two poles and two zeros, implement second-order Infinite Impulse Response (IIR) filters and Proportional-Integral-Derivative (PID) controllers. Biquads are used as building blocks for more complex filters, resulting in lower sensitivity to quantisation noise in fixed-point implementations. Biquads can be expressed in different ways: the Direct Form I is preferred for fixed-point DSP implementations and the Direct Form II is usually chosen for FPGAs and floating-point DSP processors. IP cores, FPGA compilers and library functions are also available.

Trigonometric functions are processing-intensive operations, used in feedback and DDC tasks, in particular in high phase resolution cases. In FPGA, trigonometric functions are achieved via the Coordinate Rotation Digital Computer (CORDIC) algorithm [39]; in floating point DSPs, a good balance between high resolution and execution speed is reached by polynomial interpolation and hardware-specific DSP features (e.g. SIMD).

### *Cascaded Integrator Comb (CIC) Filter*

The CIC or Hogenauer filter [40] is a multirate interpolating or decimating low-pass filter made of cascaded integrator and comb stages. CIC filters are fully determined by three parameters: $N$ = number of cascaded integrator and comb stages; $R$ = decimation or interpolation ratio; $M$ = number of delays in the comb stages. Figure 4 shows the decimating CIC filter structure: integrator and comb stages operate at the sampling rate $f_s$ and at the reduced sampling rate $f_s/R$, respectively.

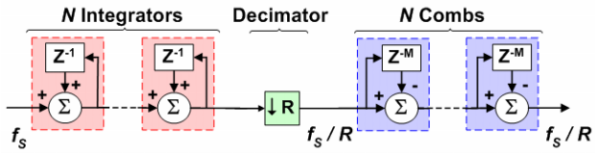


Figure 4: Decimating CIC filter structure.

The decimating CIC filter frequency response corresponds to that of $N$ cascaded $MxR$ sliding average filters; it has high passband droop, low stopband attenuation and notches located at multiples of $f_s/M$. In applications not requiring a low group delay the passband droop and low stopband attenuation are improved by an additional filter after the CIC filter. FPGA use of CIC filters is attractive because a) fewer resources are used than with IIR and Finite Impulse Response (FIR) filters and b) of the direct relationship between desired filter characteristics and accumulators width. CIC filters are preferred over FIR filters for DDC I/Q detection with feedback loops, owing to their shorter group delay which allows better loop stability margins. The group delay is shortened by filtering the signal only where necessary, as notches are located at multiples of the revolution frequency $f_{REV}$. In synchrotrons with large frequency swings, $f_s$ varies and is chosen as an integer $f_{REV}$ multiple [18]. In the J-PARC Rapid Cycling Synchrotron (RCS) $f_s$ must be constant and CIC filters with smoothing varying coefficients are used [41].

### *Modern Control*

Modern control consists mostly of time-domain techniques to handle complex Multi-Input-Multi-Output (MIMO), non-linear and time-variant systems. State-variable methods [42] allow design of feedback controllers from information on the plant internal states. This method was used for BNL's initial design of the AGS and RHIC loops [43]. Adaptive techniques implemented by the crate controller are used for Adaptive FeedForward (AFF) systems. Examples are the TTF [44] and SNS linacs [45] AFF systems. The latter counteracts cavity beam loading: next-pulse RF control is based on FIR-filtered previous-cycle errors. Figure 5 shows the SNS AFF effect on the cavity amplitude and phase.

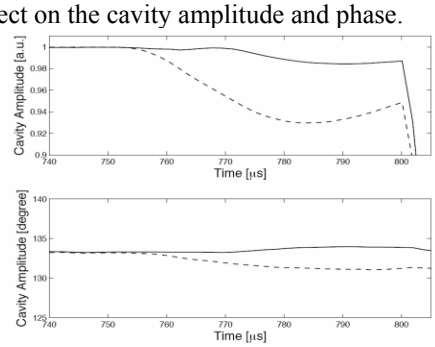


Figure 5: SNS DTL4 cavity amplitude/phase under beam loading with (solid line) and without (dashed) AFF [45].

## OVERVIEW OF DIFFERENT DESIGNS

LLRF requirements and DLLRF systems are reviewed, sorted according to RF needs, with selected examples.

### *Cyclotrons, Synchrotrons and Hadron Colliders*

Isochronous cyclotrons need cavity voltage amplitude/phase control to counteract beam loading. Most synchrotrons include beam phase, radial and synchronisation loops; cavity amplitude, phase and tuning loops may be digitally implemented. In high-intensity synchrotrons the LLRF must also counter beam loading. RF feedback loops, reducing the apparent coupling impedance of the RF fundamental mode, are often analogue owing to the short latency required; digital systems in parallel with them include feedforward, fast feedback and one-turn delay comb filter feedback (e.g. CERN's SPS, PS, LHC). Hadron colliders may include a synchronization loop to phase-lock two circulating beams.

In the TRIUMF cyclotron [46], DSPs achieve an amplitude/phase PID controller.

CERN LEIR [17] and Fermilab's Main Ring [10] are examples of DLLRF–equipped synchrotrons. CERN LEIR DLLRF includes extensive diagnostics, is based on DSP-carrier boards, daughtercards and FPGA-implemented I/Q detection and control. A tagged clock achieves system-wide synchronisation and deals with large $f_{REV}$ swings. Fermilab's Main Ring DLLRF is based on VXI crates and SHARC DSPs. Fermilab's Main Injector and Recycler have digital, FPGA-implemented transverse and longitudinal bunch-by-bunch dampers [47]. SNS [48] is a DLLRF-equipped storage ring, implementing a digital cavity controller through EPICS by VME modules and SHARC DSPs hosted on COTS PCM daughtercards. I/Q loops and PI regulators control individually the amplitude and phase of the four SNS ring cavities. Beam current feedforward compensation and dynamic tuning are implemented. J-PARC RCS and Main Ring (MR) synchrotron [49] will accelerate an ultra-high intensity proton beam; their FPGA-based DLLRF is equipped with multi-harmonic RF generation for acceleration and bunch shaping, phase, radial and cavity amplitude control loops. A multi-harmonic feedforward scheme will compensate heavy beam loading on their broadband cavities.

The three hadron colliders planned or under operation are CERN's LHC [22], BNL's RHIC [20] and Fermilab's Tevatron [10]. LHC DLLRF main functions are cavity tuning/power control, beam control, RF synchronization and longitudinal damping. Custom hardware modules are implemented with a VME form factor and include Xilinx FPGAs and TigerSHARC DSPs. Digital I/Q demodulators, feedforward and feedback methods are used; eight cavities per ring are individually controlled by a klystron and a cavity controller module. RHIC DLLRF is based on COTS VME boards. Phase/radial loops are designed with state-variable formalism. Tevatron DLLRF is based on VXI bus and SHARC DSPs. Phase, radial position and collision point are feedforward-calculated.

### *Linacs, FEL and Linear Colliders*

Linacs include cavity voltage amplitude, phase and tuning loops. Superconducting linacs require fast loops fighting cavity detuning due to Lorentz force and microphonics, achieved by feedback/feedforward methods. Linacs can be Continuous Wave (CW) or pulsed; both are sensitive to microphonics and pulsed machines are sensitive also to Lorentz force.

SNS [30], VUV-FEL [38], J-PARC [19] and the future PEFP proton linac [50] are pulsed linacs equipped with DLLRF. The SNS linac is a 60 Hz repetition rate machine with a Generator-Driven Resonator (GDR) scheme. Its DLLRF, developed as collaboration between ORNL, LBNL and LANL, uses EPICS and controls both superconducting and normal conducting cavities. An FPGA-implemented PI controller performs the cavity field fast feedback control, while adaptive feedforward takes care of transient beam loading [45]. J-PARC linac DLLRF is based on COTS cPCI modules including DSPs, FPGA and a Programmable Logic Controller (PLC) as the main system controller. DSPs control the cavity tuning via the PLC, while the daughtercard-hosted FPGAs implement a PI controller for fast feedback. VUV-FEL's powerful DLLRF is based on GDR, cavity vector-sum control and VME boards that host DSPs/FPGAs and are connected to ADCs/DACs via Gigabit links; feedback and feedforward methods are used. The CERN Linac3 energy ramping cavity is controlled by a VME-sized, FPGA-implemented PI controller [32]. PEFP proton linac will be equipped with a FPGA/DSP-based DLLRF implementing cavity field fast feedback control under EPICS.

CEBAF [32], Cornell's Energy Recovery Linac (CERL) [51] and ISAC II [52] are DLLRF-equipped CW linacs. CEBAF has single-cavity control and digital GDR with PI controller in a FPGA. VXI bus-based, it includes daughtercards carrying ADCs/DACs. CERL is to operate cavities at extremely high loaded $Q$ ($Q_L$ = several $10^7$), the resulting small cavity bandwidth making the RF field very sensitive to tuning perturbations. Its initial DLLRF, based on modules designed for Cornell's Electron Storage Ring (CESR), was successfully tested at JLAB FEL. ISAC II uses a self excited loop, with a hybrid analogue/digital LLRF and a DSP-based controller.

The SLAC Linear Collider, not operating anymore, was the first linear collider and a pioneer in modern control applied to fast digital feedbacks [53], which were cascaded via adaptive methods to avoid over-corrections. Proposals for future linear colliders include the International Linear Collider (ILC) and the Compact Linear Collider (CLIC). ILC DLLRF is already being proposed. CLIC LLRF will need very good driving field stability, especially concerning the phase. Fast DLLRF and feedforward techniques will be used.

### *Light Sources and Lepton Colliders*

Synchrotron light sources and lepton colliders usually need no beam phase and radial loops. Cavity tuning, amplitude and phase loops are present. Direct analogue

RF loops often counteract beam loading in parallel with digital feedbacks. Light sources and lepton colliders suffer from multi-bunch instabilities, longitudinal and transversal, generated by stored bunches interacting with cavities or electron/ion clouds. These instabilities increase beam emittance, can cause beam losses and may be cured by mostly-digital bunch-by-bunch feedback.

ALBA [35] and SOLEIL [54] light sources are considering DLLRF usage. ELETTRA and SLS use digital transverse/longitudinal multi-bunch feedback [34].

Lepton colliders are CESR [33], DAFNE [55], HERA, PEP-II [56] and KEKB. CESR was supplied in 2004 with a custom digital RF field control system based on Virtex II FPGAs and SHARC DSPs. This stabilises the vector sum of superconducting, heavily beam-loaded cavities by fast feedback/feedforward control. DAFNE is a small-sized collider with digital transverse and longitudinal bunch-by-bunch feedback. HERA LLRF, mostly analogue, includes digital parts in the frequency control, synchronisation and narrow-band proton feedback. PEP-II LLRF, mostly digital, is based on custom VXI boards, EPICS and baseband I/Q processing. Loops include an analogue klystron direct RF feedback, digital comb filters and an adaptive digital gap feedback to prevent klystron saturation. Digital longitudinal and transversal feedbacks are also implemented [11,21]. KEKB runs on a mostly analogue LLRF and digital bunch-by-bunch feedback [57]; the future SuperKEKB will include a new DLLRF.

## SUMMARY

This survey shows many DLLRF appealing factors, difficult to achieve with analogue solutions, e.g. remote control, full multi-user support, built-in diagnostics, sophisticated algorithms and easy customisation. This implies useful transportability of algorithms between machines. For these reasons, DLLRF is used in most existing accelerators and is the choice for complex new developments. Analogue LLRF is still used in very fast loops but the latency advantage over DLLRF will soon be reduced by technology progress. Custom units are mostly used and each laboratory often develops its own version; hence possibilities for inter-laboratory collaboration exist, particularly for new complex projects being proposed.

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