THE TIMING SYSTEM FOR DIAMOND LIGHT SOURCE

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Abstract

The Diamond timing system is the latest generation development of the design, principles and technologies currently implemented in the Advanced Photon Source and Swiss Light Source timing systems. It provides the ability to generate reference events, distribute them over a fibre-optic network, and decode and process them at the equipment to be controlled. The timing system is closely integrated within the Diamond distributed control system, which is based on EPICS. The Diamond timing system functionality and performance, and first operational experiences in using the timing system during the commissioning of the accelerators, are presented in this paper.

INTRODUCTION

Diamond is a new 3rd generation synchrotron light source currently being commissioned in the UK. The timing system provides the hardware trigger to operate the three accelerators. The Diamond timing system is a development of the design, principles and technologies currently implemented in the Advanced Photon Source [1] and Swiss Light Source [2] timing systems, but introduces additional features including programmable pulse delay and width on all outputs, multiplexed front panel outputs, RF clock recovery on the event receiver, extended time stamping support and larger event sequence RAMs, together with improved stability and resolution.

DIAMOND TIMING SYSTEM STRUCTURE

The Diamond timing system is based on an event generator (EVG) which generates events from an internal sequencer and external signals. The events are distributed over fibre optic links to multiple event receivers (EVRs). The EVRs, which are located in the control system interface layer, decode the events as hardware triggers, software interrupts or EPICS software events. Hardware triggers are connected directly to the equipment using copper or fibre optic connections, or through a four channel timer when greater timing resolution is required. For the linac the decoded events are further encoded by a gun driver set and sent over a fibre link to the gun high voltage platform where they are decoded. This structure is shown in Fig 1.

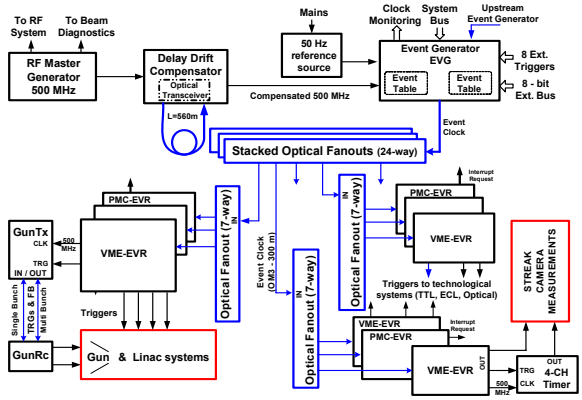

Figure 1. Structure of the DLS Timing system

HARDWARE DESCRIPTION

The core components of the timing system, the EVG, the EVR, the linac gun driver, and the four channel timer were designed by Micro Research Finland to meet a performance specification by Diamond Light Source.

Event Generator

The EVG issues event frames, each consisting of an 8-bit event code and an 8-bit distributed data bus, at a rate of 125 MEvent/sec. The event clock is derived from the 500 MHz RF signal. There are several sources from which events are generated: eight external trigger events, a sequence RAM, software events and events received from an upstream event generator. Events from different sources have different priorities which are resolved in a priority encoder. The sequence RAMs provide a method of transmitting or playing back sequences of events stored in random access memory. The sequence RAM clock is produced by dividing down the event clock. The 8-bit distributed data bus signals are sampled simultaneously at the event clock rate and distributed to the event receivers.

Event Receiver

The EVR recovers the 500 MHz clock from the event stream and demultiplexes the event stream to the 8-bit distributed bus and the 8-bit event code. The decoded events are mapped through RAMs on to one of the following: four delayed pulse outputs, with programmable width and delay (16-bit pre-scaler from an event clock, 32-bit delay and a 32-bit width register), 14 pulse outputs with programmable delay and width (32-bit delay and 16-bit width) or seven set/reset flip-flops. The processed events can produce hardware outputs, software interrupts

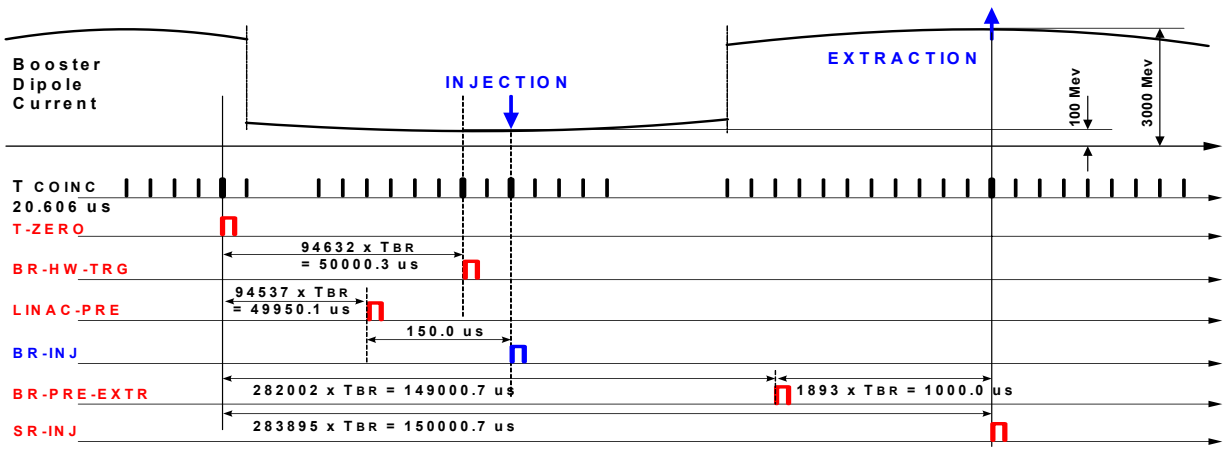

Figure 2. Timing sequence for accelerating electrons through the Linac and Booster

or EPICS software events. The hardware outputs are routed either to the front panel connectors as TTL or PECL signals, or to rear transition boards giving conditioning to TTL and optical outputs. Three event codes and one bit of the distributed bus are reserved for transmitting timestamping data. Two of these event codes are used for sequentially shifting UNIX time into all EVRs, whilst the third code latches the new value into the seconds register and resets the fractional time register. The fractional time register is constantly incremented by the 1 MHz reference clock provided via the distributed bus. Logic inside the EVG and EVRs ensures the correct operation of timestamping distributions and avoids time discontinuities. The EVR is realised as both VME and PMC modules. The latter costs less but provides fewer front panel outputs, no RF clock recovery and reduced stability of outputs.

Linac Gun Driver

The linac gun driver is realised as two modules, a gun transmitter, and a gun receiver which is placed on the gun HV platform. The gun transmitter accepts two trigger signals from an EVR system, delays them with a resolution of 2 ns and range up to 8.5 sec, and generates modulated optical signals which are sent to the gun receiver. A fine programmable delay is also available which allows adjustment of the triggering position to a resolution of approximately 10 ps over a range exceeding 2 ns.

Four Channel Timer

The four channel timer [3] provides four independent timer channels with programmable delay and pulse width. The timer channels may be triggered by PECL signals from the front panel or through a rear transition board by TTL levels. Multiple timer channels may be triggered from a common input. The delay and pulse width for each channel may be adjusted from 0 to 8.5 sec with resolution of 2 ns (one RF clock cycle). In addition, each channel may be further delayed for a period up to 10 ns defined to 10 ps resolution.

Timing System Optical Network

The timing distribution network delivers event messages to a maximum of 250 EVRs using OM3 multimode fibre as the transmission medium. The network is structured as a two level multi-star topology using 24- and 7-way fanout modules. Simultaneous delivery of event messages to multiple EVRs is arranged by using fibres of equal lengths, about 320m, cut with a precision of +/-0.5 metre.

Given the expected range of temperature deviation in the Diamond building, there could be induced delay drifts in the timing system network on the level of more than 100 ps. A scheme to compensate for this has been developed using a delay compensation loop [4].

OPERATIONAL ASPECTS

The Diamond SR has 936 buckets and a revolution frequency of 533.8 kHz, and the Booster 264 buckets and a revolution frequency of 1892.6 kHz. The coincidence of the SR and Booster revolution determines a frequency for the coincidence clock of 48.529 kHz, based on the common factors of the two frequencies. The Booster clock is used to increment the EVG sequence RAM, and the coincidence clock is used to reset the sequence, thereby locking all cycles to both accelerators. Event entries are placed in the sequence RAM to generate the necessary sequence of triggers to accelerate the electrons through the linac and booster and into the SR.

Timing System Events

The timing sequence for accelerating electrons through the linac and booster into the SR is shown in Fig 2. The events to achieve this are listed in Table 1. They provide the key fiducials to realise the timing sequence.

Table 1. Timing system events used for Diamond

Event Reference	Time (us)	Description
T-ZERO	0	Booster cycle trigger
LINAC-PRE	49950.1	Linac gun pre-trigger
LINAC-HBT	49950.6	Linac systems trigger
BR-HW-TRG	50000.3	Booster magnets
BR-INJ	50100.1	Booster injection
BR-PRE-EXTR	149000.7	Booster pre-extraction
SR-INJ	150000.7	SR injection

Storage Ring Fill Pattern Control

The above sequence is sufficient to move a single bunch of electrons to same bucket in the SR for each cycle. The operation of modern light sources requires that a variety of fill patterns are realised in the SR. It is possible to place arbitrarily a single bunch or bunch train anywhere in the SR by delaying the extraction from the Booster. However, this delay would become unacceptably long.

An improved scheme is to consider that the SR orbit is divided into 8 segments of 120 buckets and every fourth Booster turn is phase-locked with its SR segment. Hence, it is possible to place a single bunch or start of bunch train by varying the linac gun trigger (in range of 120 RF clock periods) and booster extraction event with multiples of four booster orbit clocks. So to target SR bucket number 340 the booster extract delay will be 8 periods of booster orbit clocks and a linac delay of 100 RF clocks. This sequence of modifying the linac trigger times and booster extraction on a cycle-by-cycle basis is controlled through an EPICS application. Control system inputs to this application determine the fill patter for the SR. Currently supported patterns are single bunch repeat, bunch train repeat, single bunch one shot, bunch train one shot, SR 2/3 fill and SR fill of all buckets.

CONTROL SYSTEM INTEGRATION

The timing system integrates into the EPICS control system through a number of EPICS records. The EG record is used to configure and modify the options of a specific EVG module. Options include choice of the EVG operating mode, selection of internally generated clock rates, optional transmission of software-invoked events and enablement or otherwise of event trigger inputs. The EGEVENT record is used to specify a single event to be placed into the sequence RAM. The time displacement from the start of the sequence and event code are assigned by the record.

The ER record configures the options for the EVR, such as pulse delay, width and polarity, front panel output assignments and distributed bus enable. The EREVENT record specifies the desired actions to be performed upon receipt of a specific event code.

Event system events are decoded into EPICS events using the EPICS EVENT record which can subsequently trigger the execution of other EPICS records.

The time stamping support provides distributed common time to all systems. The extended time stamping registers on the event receivers hold the UNIX time in seconds as well as a fractional seconds count with a 1uSec resolution.

Applications to control the timing system are built with the usual EPICS tools for databases and EDM for display panels. These applications provide control for the EVG and for each of the decoded triggers.

CONCLUSION

The overall timing system has provided the required functionality to operate the linac, booster and storage ring during the commissioning phases. However the timing system is not complete, with additional hardware for thermal induced delay compensation yet to be installed, EVRs yet to be installed for some technical systems, and additional events yet to be created including those for post mortem and synchronous control of insertion devices with beamline components. The components installed to date have worked reliably and have achieved the required level of functionality and stability. Overall performance of the system is still to be determined but looks promising.

REFERENCES

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