# HIGH DYNAMIC RANGE SPECTRAL ANALYSIS IN THE kHz BAND

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#### Abstract

Many beam instrumentation signals of large circular accelerators are in the kHz range and can thus be digitised with powerful high resolution ADCs. A particularly large dynamic range can be achieved if the signals are analysed in the frequency domain. This report presents a system employing audio ADCs and FPGA-based spectral analysis, initially developed for tune measurement applications. Technical choices allowing frequency domain dynamic ranges beyond 140 dB are summarised.

## **INTRODUCTION**

The large market for PC sound cards and audio processing devices has resulted in the availability of excellent and inexpensive audio ADCs. Often they have two channels and are accompanied by two (or more) DACs in a single chip, commonly referred to as "codec". Good audio ADCs have 24-bit resolution with excellent linearity given by the  $\Sigma/\Delta$  architecture and datasheet signal-to-noise ratios (SNRs) in the order of 100-120 dB, corresponding to some 16-20 effective number of bits. The remaining bits normally contain noise, but as this is to a large extent white noise, it can be lowered by spectral analysis or time domain filtering, resulting in an increased dynamic range. Since the frequency domain SNR improves as  $\sqrt{N/2}$  for an *N*-point FFT, for 4K-point FFT one gains some 33 dB and for 64K-point FFT the gain is about 45 dB, giving potential SNRs above 160 dB.

As illustrated in Fig. 1, the presented spectral analysis system is based on an audio codec, connected to a digital acquisition board (DAB) through an LVDS link. The DAB, hosting a large FPGA and memory, is a standard CERN acquisition/processing VME board used for most of the LHC beam instrumentation systems. In the discussed system the DAB stores the acquired data and performs FFT calculation, prior to transmitting raw data and calculated spectra to a VME front-end computer (FEC). The FEC, connected to the control infrastructure by a fast Ethernet link, makes the data available for end applications [1].

As the DAB-based real-time FFT analysis providing 180 dB dynamic range is described in [2], this paper

focuses on the remaining crucial aspects of the system, making it a powerful, inexpensive high dynamic range acquisition and spectral analysis system.

#### 24-BIT ADC/DAC MODULE

The system described in this paper was built primarily for the LHC tune and chromaticity measurement systems [1], which process two beam signals and provide two excitation signals that are band-limited to half the revolution frequency ( $f_r \approx 11.2$  kHz for the LHC). An audio stereo codec with two ADCs and two DACs was the natural choice for the core of the system. Since system prototypes were studied at the CERN SPS ( $f_r \approx 43$  kHz) and BNL RHIC ( $f_r \approx 78$  kHz), the design is compatible with all these machines.

The 24-bit ADC/DAC circuit was built not as a VME module, but in a NIM format, at the expense of having an additional crate in the system. This solution offered more room to accommodate input and output insulation transformers, which have substantial dimensions as they carry low frequency signals of relatively large amplitudes. Furthermore, NIM chassis typically offer lower levels of electromagnetic interference, since they usually contain analogue electronics in shielded modules, and as they provide power supplies of good quality that are less subject to perturbations from complex digital modules rare in NIM chassis.

From the many audio codecs available in the market Cirrus Logic CS4272 was selected, a 28-pin chip containing two 24-bit ADCs and two 24-bit DACs with differential inputs and outputs. The choice was a compromise between the chip performance and complexity, mainly of the configuration protocol. Its datasheet SNR is 111 dB and the maximal sampling frequency ( $f_s$ ) 200 kHz, however, its best SNR was found to be for  $f_s$  below 50 kHz.

The codec inputs and outputs allow differential architecture for the input amplifiers and low pass filters (LPFs) as well as for differential output interpolation LPFs. This increases the immunity to interference and the dynamic range.

Despite the fact that the 24-bit ADC/DAC module

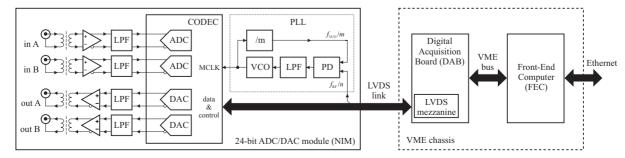


Figure 1: Block diagram of the kHz range spectral analysis system.

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circuits work at low frequencies, in order to maximise the dynamic range, its four-layer PCB was designed according to high frequency design rules, such as using only small surface mount components, low inductance power supply decoupling, solid ground planes and no thermal reliefs on the component layers.

The inputs and outputs of the NIM module have insulation transformers. The purpose of the input transformers is to prevent ground loop currents that may arise if the module and the source of the analysed signal (typically an analogue front-end) are distant from each other and if their local grounds are not exactly on the same potential. This is especially common in the vicinity of large power systems. In case the signal cable connecting the module and the source is grounded on both ends, any ground potential difference will drive a current through the cable ground conductor. This current creates in turn a voltage on the cable resistance and the voltage appears on the input of the ADC. Introducing insulation transformers between the two ground domains reduces the ground currents to the one flowing through the interwinding capacitance of the transformer. While in the kHz range this current can be kept small, insulation transformers significantly reduce ground loop interference for low frequencies.

The purpose of the output insulation transformers is to prevent ground loops for the input of the remote system connected to the DACs (e.g. high power transverse damper amplifiers).

Unfortunately, the insulation transformers for the kHz range have to be of substantial size and wound on a high permeability core with many windings. To minimise their size and number of turns, the NIM module has 50  $\Omega$  input and output impedance, contrary to typical audio systems. Low input/output impedance also helps to achieve good transformer insulation.

The drawback of using insulation transformers is measurable signal distortion that depends on signal amplitude and frequency. This was one of the reasons to limit the full scale (FS) amplitude to 2.8 Vpp for the inputs and to 2.5 Vpp for the outputs.

It was observed that the insulation transformers captured some stray magnetic fields (e.g. of the NIM power supply transformer, however below the -100 dBFS level), thus they are useful only if the ground loop interference dominates, which is usually the case in large accelerator installations.

For tune measurement applications it is necessary that the ADC sampling is synchronised to the machine revolution frequency  $f_r$ . The ADC sampling clock is thus derived from the machine RF system. In addition, typically for the  $\Sigma/\Delta$  architecture, the master clock (MCLK) frequency supplied to the codec is a multiple of  $f_s$ . To fulfil these requirements the codec MCLK was produced by a PLL synchronised to the RF frequency ( $f_{\rm RF}$ ), as shown on the system block diagram in Fig. 1.

To minimise MCLK jitter, the voltage controlled oscillator (VCO) was built as an LC generator tuned with a varicap diode. Since  $f_r$  variations for all considered

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machines are small (e.g. maximal relative change of LHC  $f_r$  is some 25 ppm), the VCO tuning range was limited to some  $\pm 1$  %, determined by potential drifts of resonator components. The phase detector (PD) is a part of an integrated PLL circuit, followed by a passive low-pass filter. The MCLK jitter was measured to be about 5 ps<sub>rms</sub>.

Since the system is supposed to work for three machines, the required clocking flexibility was achieved by programming the  $f_{RF}$  divider in the FPGA and the VCO frequency divider in the NIM module, as shown in Table 1, listing also other parameters of the clocking scheme. With such a scheme, it was possible to maintain a similar VCO frequency for all machines, and only the simple LPF of the PD is machine specific, in order to achieve an optimal PLL dynamic for different loop gains.

For the LHC system  $f_s$  is a fourth multiple of  $f_r$  and samples are filtered and decimated to  $f_r$ , in order to improve the system SNR by 6 dB.

Tune measurement of smaller CERN accelerators required extending the system bandwidth to a few MHz and this was achieved by replacing the 24-bit ADC/DAC module with two DAB mezzanines, one accommodating two 16-bit, 40 MHz ADCs and the second with two 12-bit, 40 MHz DACs. The FPGA signal processing required only a few minor changes. The achieved ADC SNR, largely sufficient for the small accelerators, is lower by some 30 dB with respect to the system based on the audio codec.

Table 1: Codec Clocking Parameters

	<i>f<sub>r</sub></i> [kHz]	$\frac{f_s}{f_r}$	$\frac{f_{\rm MCLK}}{f_s}$	$\frac{f_{\rm RF}}{f_r}$	<i>f</i> <sub>RF</sub> [MHz]	n	m	f <sub>мсlк</sub> [MHz]
LHC	11.25	4	384	3564	40.08	297	128	17.27
SPS	43.4	1	384	924	40.08	77	32	16.66
RHIC	78.0	1	192	360	28.08	60	32	14.98

#### **RESULTS**

Beam measurements obtained with the described system are presented in [1, 2] and this report focuses on lab measurement results shown in Fig. 2, documenting an ultimate SNR performance of the system in the LHC version.

In typical applications of the system the DAC signal quality is much less important than the performance of the ADCs. However, for the presented measurements the DAC signals were put on the ADC inputs, as the DAC signal quality surpasses all typical lab sine wave sources.

Figure 2a shows a 4K-point FFT magnitude spectrum for a measurement done with the DAC signals (in blue), alongside with a measurement with no ADC input signal, averaged 100 times (in red). As the DAC signal amplitude was close to the FS, many harmonics of the fundamental tone are present. They are related to nonlinearities of the two insulation transformers and the rest of the chain, in particular the DAC output amplifier driving low impedance load. The noise floor for the measurement without signal is about -152 dBFS, clearly seen due to the averaging. It rises ( $\approx 2$  dB) for low frequencies, because of

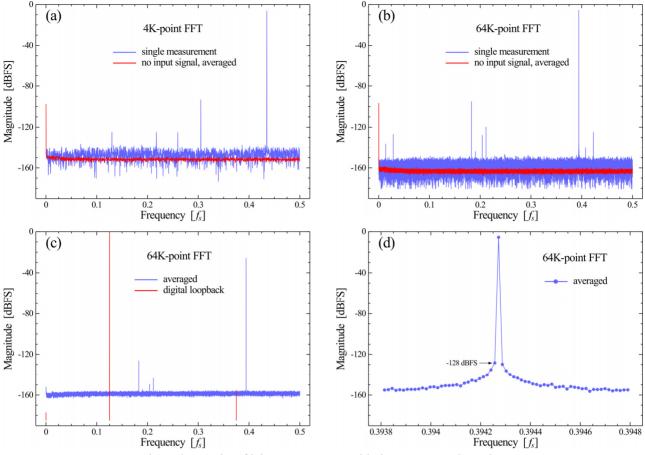


Figure 2: Results of lab measurements with the system LHC version.

low-pass filtered noise from an ADC input bias resistors. If from the -152 dBFS noise floor are subtracted SNR improvements due to the FFT (33 dB) and the time domain averaging by four (6 dB), one gets the time domain noise floor of -113 dBFS, which is compatible with the datasheet typical SNR of 111 dB.

Corresponding measurements for a 64K-point FFT magnitude spectrum are shown in Fig. 2b. The noise floor, having similar low frequency slope, reduces to about -163 dBFS, i.e. by 11 dB, which is close to the theoretical 12 dB related to the FFT length increase by factor 16.

Figure 2c shows an average of 100 spectra with a lower DAC output (in blue) and a spectrum obtained with the digital signal processing in the loopback mode (in red). In this mode calculated DAC samples directly undergo processing normally performed on the ADC data. It can be seen that smaller DAC amplitude decreases the harmonic level. The noise floor, now being the superposition of the ADC and DAC noise performance, is higher by  $\approx 4$  dB than the one with no input signal shown in Fig. 2b. The loopback spectrum contains only three non-zero bins: the fundamental tone, the third harmonic and the DC component, both accommodating all the quantisation noise related to digital sine generation and truncations in signal processing. The achieved spurious component level is a measure of quality of the sine generation and the remaining bins containing zeros

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(which have been omitted on the logarithmic scale plot) show the dynamic range of the FFT calculation [2].

Figure 2d shows the fundamental tone averaged 100 times and zoomed within  $0.001 \cdot f_s$  (65 bins).

#### CONCLUSIONS

The described high dynamic range frequency analysis system was built primarily for the LHC tune and chromaticity measurement applications. At the expense of designing algorithms and code for the FPGA of the DAB and building the NIM 24-bit ADC/DAC module, the CERN Beam Instrumentation Group gained a powerful and inexpensive system, which is used also for the LHC 4.7 GHz Schottky monitor [3] and special RF system diagnostics based on wall current monitor signals [4].

### REFERENCES

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