AN FPGA BASED DATA ACQUISITION SYSTEM FOR A FAST ORBIT FEEDBACK AT DELTA

G. Schuenemann, P. Hartmann, D. Schirmer, P. Towalski, T. Weis, K. Wille,
DELTA, Technical University of Dortmund, Germany
P. Marwedel, Technical University of Dortmund, Germany

Abstract

The demand for beam orbit stability for frequencies up to 1kHz resulted in the need for a fast orbit position data acquisition system at DELTA. The measurement frequency was decided to be 10kHz which results in a good margin for 1kHz corrections. It is based on a Xilinx University Program Virtex-II Pro Development System in conjunction with an inhouse developed Analog-Digital Converter board, featuring two Analog Devices AD974 chips. An inhouse developed software written in VHDL manages measurement and data pre-processing. A communication controller has been adopted from the Diamond Light Source [1] and is used as communication instance. The communication controller is versatile in its application. The data distribution between two or more of the developed measuring systems is possible. This includes data distribution with other systems utilizing the communication controller, e.g. the Libera beam diagnostic system[1].

To enhance its measuring capabilities one of the two onboard PowerPC cores is running a Linux kernel. A kernel module, capable of receiving the measurement data from the Field Programmable Gateway Array (FPGA) measurement core, was implemented [2], allowing for advanced data processing and distribution options. The paper presents the design of the system, the used methods and successful results of the first beam measurements.

INRODUCTION

Since DELTA faces the demand for improved beam orbit stability for supplying a higher brilliance synchrotron radiation, a suitable data acquisition system for fast orbit feedback had to be found. Measurements regarding the electron beam disturbances have shown a variety of sources [5]. Slow orbit shifts have been observed, caused by thermal drifts on a day to week scale. In addition ground motion and girder movement in the low frequency range of up to 10Hz (DELTA girder resonance) have also been observed. On the other hand much faster excitation is caused by the mains power frequency of 50Hz and its harmonics up to 300Hz. The existing analog position measurement system used for the slow orbit feedback at 0.1Hz may be operated at a maximum orbit position data rate of 10kHz. To exploit this capability a most versatile adoption to this data had to be found and a data acquisition system had to be designed and implemented without any interference with the existing global slow orbit feedback system, which is supplied with orbit data from the same orbit calculating devices. This approach includes cost effectiveness (by using existing orbit electronics) as well as modularity (modular system) and versatility (broad range of communication options).

GENERAL LAYOUT

DELTAs orbit feedback is a classic control loop. The data is acquired, corrections are calculated and applied to the beam by means of magnetic fields. Modern fast orbit feedback systems [1, 3] are based on turn-by-turn (TBT) beam position data reduced to kHz bandwidth. Only a minor number of Deltas BPMs are TBT measurement capable. Therefore the idea to use the existing analog Bergoz MX-BPMs in combination with TBT capable devices for a fast orbit data acquisition system came up. To achieve the systems desired versatility and modular design a decentralized solution was chosen. Initial design ideas were adopted from the concept of the Libera Electron fast orbit feedback at Diamond Light Source, England, including data interchange with any device running the underlying communication structure, the Diamond Communication Controller (DiamondCC) [1].

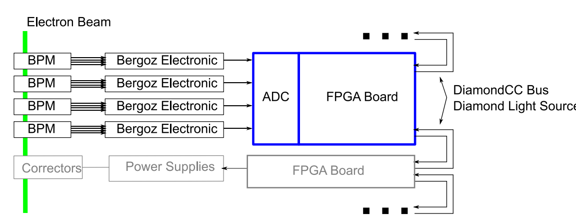

Figure 1: Data acquisition system (DAQ) layout. Additional bus participants can be connected if desired.

The system follows the idea of a classic control loop (see figure 1). The electron beam induces a voltage on the four beam pickup buttons. The position of the electron beam is calculated by the Bergoz MX-BPMs. The analog position value is then digitized by an ADC-board and transferred to the FPGA being part of the Xilinx University Program development board [6]. The FPGA takes over the task of pre-processing and then distributing the data amongst the feedback participants. These are typically either data pickup stations, correction calculation instances or data logging devices. The DiamondCC is the communication instance used for this data distribution. It features a synchronized, global position data exchange on a fast time basis, thereby avoiding the common bottleneck for orbit feedback applications. Adjustment to the possible maxi-

[1]Instrumentation Technologies d.o.o., Solkan, Slovenia

mum number of bus participants is accomplished through the number of communication interfaces. The necessary correction is then calculated by each corrector station and applied accordingly (see figure 1).

ORBIT POSITION GENERATION & DATA READOUT

The analog orbit position data at DELTA is generated by Bergoz MX-BPMs. These analog electronics use a multiplexer to sample each of the four orbit position pickup button signals to make use of a single amplifier stage and an additional sample/hold and position calculating circuit [4]. Due to the input multiplexing technique used, the maximum position data output rate is a quarter of the multiplexing frequency. Without a possible external clock this frequency is coasting with approximately 8kHz, resulting in a 2kHz position data rate. The maximum specified operation range however is a 40kHz multiplexer frequency creating a 10kHz position data rate. Measurements have shown that the MX-BPMs indeed are able to run at 40kHz, the only drawback being a fluctuation of the position signal at the start of the multiplexing cycle. Fortunately the start of this cycle is indicated by a trigger, thus making a workaround to this problem by clever timing possible (see figure 2).
These demands resulted in the development of the data readout board. The core component is the Digital Analog Converter, in our case the AD974 by Analog Devices was chosen, having a 16Bit, 200kHz data conversion rate in the required voltage range. Additionally it features four multiplexed inputs. It was decided to use one AD974 chip for the horizontal plane and one AD974 chip for the vertical plane. By using the multiplexing feature four Bergoz MX-BPMs can be read out with one ADC-Board. The data rate is split into a four times 50kHz signal rate, resulting in an five times oversampling of each Bergoz MX-BPM position signal. To enhance the signal quality and to filter higher frequency artefacts an optional 10kHz lowpass-filter for the input signal was integrated into the board. Apart from the data conversion part the ADC-board integrates the signal connectors for the additional control signals provided by the Bergoz MX-BPMs, e.g. the multiplexer sequence start signal (SYNC). Two additional triggers and two additional clock inputs are also installed for future use. As the communication of the FPGA-board requires special clocking, the quartz and suitable connectors are also installed on the printed circuit board.

ADC CONTROLLING & READOUT TIMING

The readout of the two ADCs is accomplished directly from the FPGA on the FPGA-board. The AD974 features different readout modes, set by configuration signals. In our case the fastest possible mode has been chosen. Due to internal design this is also the mode ensuring highest conversion precision [7]. The conversion is initiated by the FPGA. The conversion result, the digitized analog value, is then transferred from the ADC to the FPGA during the next conversion cycle. Special care has been taken on the FPGA side to synchronize the two AD974 chips and to detect possible errors. Two ensure a high quality readout signal a special, additional timing block was created on the FPGA.
The reason for this is the structure of the Bergoz MX-BPMs. Since four MX-BPMs are usually connected to one ADC-board, each multiplexer runs at a random clock around 8kHz. As soon as the external 40kHz clock is applied, the multiplexers start to run synchronized, except for the cycle of each individual multiplexer (from button one to button four), which is again random and indicated by the SYNC signal (see figure 2). This SYNC signal spoils the position readout. The workaround found is the application of the following procedure: Enabling of the external clock, checking whether the sequence of SYNC signals is suitable and re-applying the clock if necessary, hoping for a drift during the non-clocking period.

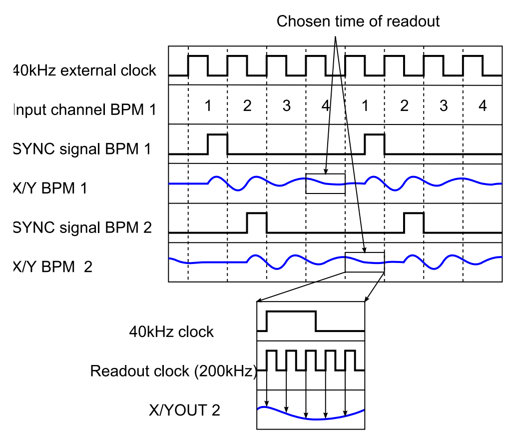

Figure 2: Signal sequence of two BPMs. The SYNC signal, always at position 1 of the Bergoz MX-BPMs multiplexer distorts the output signal. The time of readout has been adopted to the least distorted region of the signal.

Once a suitable sequence is found, the readout sequence is adjusted accordingly. The system is designed fault tolerant, thereby the number of Bergoz MX-BPMs is completely variable from one to four including hot-plugging.

DATA PRE-PROCESSING

In the ideal case one complete readout sequence takes $100\mu s$, resulting in four (one from each MX-BPM) times five (readouts of one position) by two (horizontal and vertical plane) datasets. At present only a very limited pre-processing of this data is undertaken. The last of each of the five position values is discarded and the other four are averaged for higher precision. These four by two datasets are then passed on to the communication instance.

DIAMOND COMMUNICATION CONTROLLER

Developed for the fast orbit feedback system at the Diamond Light Source, the DiamondCC has been designed for fast global data exchange. The communication is based on point to point two way connections, eliminating data collision problems. It is synchronized, clocked and deterministic. A trigger network connects all communication participants for synchronization. Once synchronized, the communication is split into 10kHz frames, each frame is completed when all position data is globally exchanged. It is a distributed communication protocol without a central server. The communication structure can be user-specified. Specific demands like fault-tolerance, lower delay or a varying number of communication participants can easily be implemented [1].
The DiamondCC was integrated onto the FPGA after adoption to the specific needs of this application. The DiamondCC was designed for I-Tech Libera Electron [8], therefore its data retrieval is adjusted to the Libera data chain. This data chain has been adopted to our ADC-Board. The most prominent alteration is the existence of four position values instead of one.

EXTERNAL CONNECTION

Instead of using the slow and the fast orbit data acquisition in parallel, a single fast data source with a reduced data rate to run a slow orbit feedback reduces the amount of complexity. The present control system has no DiamondCC interface, hence the PowerPC cores available on the FPGA fabric are utilized for this purpose. The averaged data is transferred from the pure FPGA side to one of the PowerPC cores running Linux. This enables a data exchange with an easily accessible system [2].

SOFTWARE DESIGN

The software has been designed and implemented in VHDL. The ADC-Board is controlled by the Bergoz Control unit, taking care of clocking, SYNC signal processing and readout timing. A second entity, the ADC Control Module, is solemnly for the control of the AD974 chips and reception of the digitized data. The data is passed on to the data processing unit and then on to the DiamondCC. The DiamondCC is controlled from the control module containing all global configuration informations and settings.

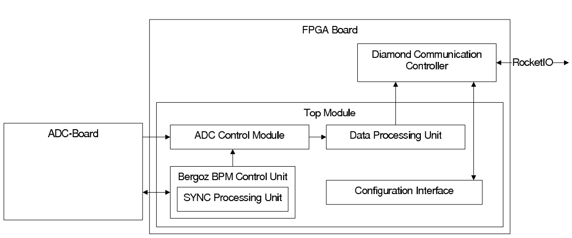

Figure 3: DAQ software layout.

CONCLUSION

The data acquisition system has proven its functionality in test measurements with beam (see figure 4) showing its broad capabilities as DAQ for a global fast orbit feedback. In a first step a local fast orbit feedback, using this fast communication structure, has been implemented successfully by P. Towalski [5]. In addition calculations have shown a precision increase in the order of one magnitude concerning the slow orbit feedback position data.

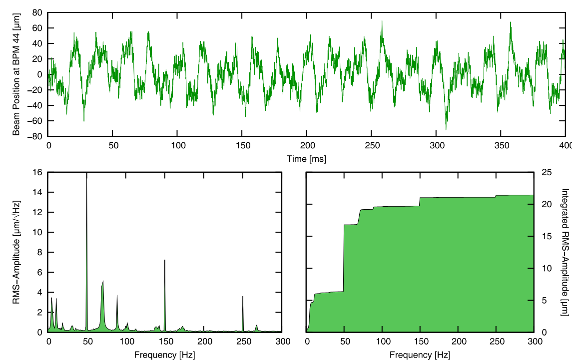

Figure 4: Horizontal beam position versus time (top), spectral rms orbit deviation versus frequency (bottom left) and integrated power density spectrum (bottom right).

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