MEASUREMENT OF ELECTRON BEAM CHARGE IN THE ESRF ACCELERATOR COMPLEX FOR ABSOLUTE AND INJECTION EFFICENCY MEASUREMENTS USING AN FPGA BASED DIGITAL BPM ELECTRONICS

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Abstract

A Beam Position Monitor (BPM) using Virtex II pro FPGAs ('Libera Electron' from Instrumentation Technologies) has been programmed with an alternative firmware in order to determine the charge by measuring integrated RF amplitude, over an adjusteable time window, of signals from 4 striplines. These striplines are located on the transfer line from the linac to the booster, on the booster ring, on the transfer line from the booster to the storage ring and on the storage ring. By calibrating the RF loss in all the cables, knowing the geometry of the striplines and using the crossbar switching before the 4 RF ADCs of the Libera, the charge/current can be compared in order to determine the efficiency of transfer at various locations during injection. Since the current in the storage ring is known to a high accuracy using a parametric current transformer (from Bergoz Instrumentation), the absolute charge can be determined at all locations.

INTRODUCTION

The transfer efficiency of beam between the various parts of the ESRF accelerator system is currently determined using electronics to integrate the signal from a current transformer in the transfer lines and parametric current transformers to mesure the quasi constant current in the booster and storage rings. The different temporal response of these different systems makes accurate comparative measurements difficult with the variety of time structured modes used at the ESRF. A new method is proposed [1] to measure the beam charge by integration of a beam signal from a stripline taken in a narrow band at the acceleration radio frequency (352.2MHz). Measurements are reported here of such a system using a Libera 'electron' to acquire and filter the signals. The technique also allows the relative RF phase of the beams in the booster and storage rings.

HARDWARE DESIGN

Striplines are located on:

i) The transfer line from the linac to the booster.
ii) The booster
iii) The transfer line from the booster to the storage ring
iv) The storage ring

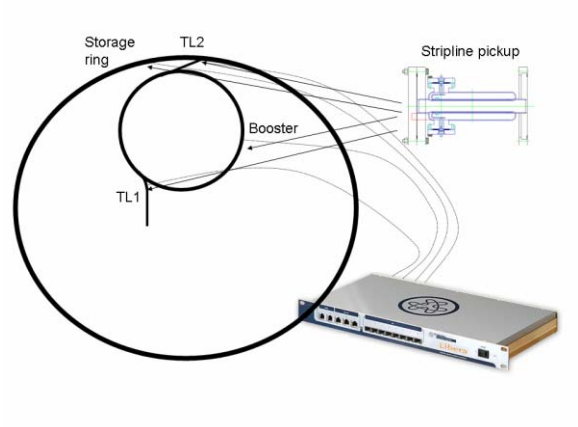

Figure 1: Location of pickups.

The signals from the 4 striplines are connected to the 4 inputs of the libera electron via 1% bandwidth RF filters (centred at 352.2MHz the acceleration frequency). The filter allows 'smearing' of the RF signal over time so as to correctly determine the amplitude with undersampling at 108MHz when in 16 bunch mode where single electron bunches are seperated by 177ns. The smearing of the signal reduces problems due to aliasing. Figure 2 below shows the single bunch currents from the Linac and then in the booster (lower trace), after a 10MHz filter (middle trace) and after a 3.5MHz filter (upper trace).

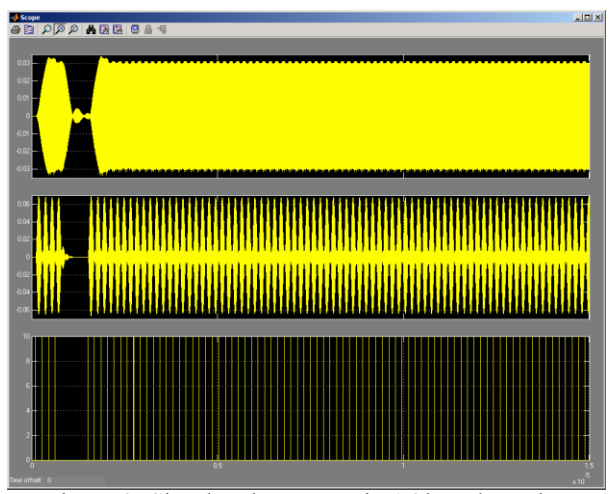

Figure 2: Simulated response in 16 bunch mode.

Libera Electron

The libera electron is a device produced by instrumentation technologies [2]. While its intended purpose is as a BPM electronics, the low noise narrow

band RF front-end with adjusteable gain and 12 bit ADCs make it ideal for the application described here. The ADCs are read using a Virtex II pro FPGA from Xilinx, which is at ease doing the digital signal processing necessary to perform accurate integrated amplitude and phase measurements. It is also designed to be directly connected to an ethernet network allowing a simplified connection to the control system. The alternative FPGA firmware design was prepared using System Generator – a tool provided by Xilinx to integrate DSP functions into their FPGAs within a *Simulink (Matlab)* environment.

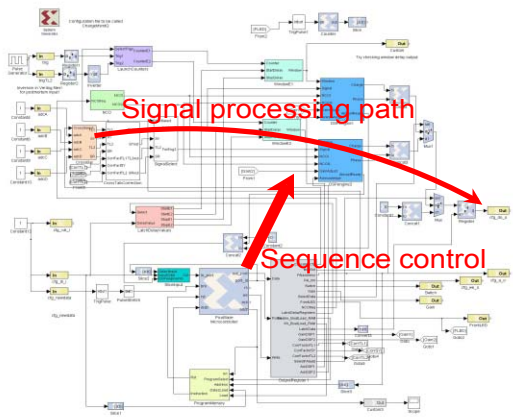

Figure 3: Firmware design in Simulink.

Firmware Design

The input signal is downconverted from the 352.2MHz frequency to an IF of 27MHz due to the undersampling of the input ADC. The image frequencies that would overlap at this frequency due to the undersampling are removed by the SAW RF filters in the front-end of the libera. The IF is mixed with a numerically controlled local oscillator, which is set to within a few kHz of the input signal (ie not locked). The demodulated signal is integrated over a time window of adjusteable delay and duration compared to either a linac trigger pulse or the booster extraction pulse. The sequencing of the integration measurements is controlled by a small 'soft' processor programmed onto the FPGA called a picoblaze. This processor is programmed in assembler and allows the scheduling of many measurements during the injection cycle. Its role is to set up each measurement, choosing a trigger source, timing delays, gain settings, signal source, crossbar setting, RF attenuators etc. The processor is not in the signal processing path, which is performed purely in the logic of the FPGA by two block called DSPeng1 and DSPeng2. The use of 2 'DSPeng' blocks allows 2 measurements to be performed simultaneously, for example to compare the relative phase of the beam in the booster and storage rings. The details of the required measurements are taken from a block RAM on the FPGA which is written to from the control system server.

OPERATION

Control Application

The libera is configured via registers in a shared memory, which is also used to export the results in a buffer. For the purpose of development a graphical application was prepared using *Matlab's* '*Guide*' utility, which allows configuration data to be enterred and details of all the required measurements (eg Transfer line, start and stop delays for integration, trigger pulse to use, numerical gain setting)

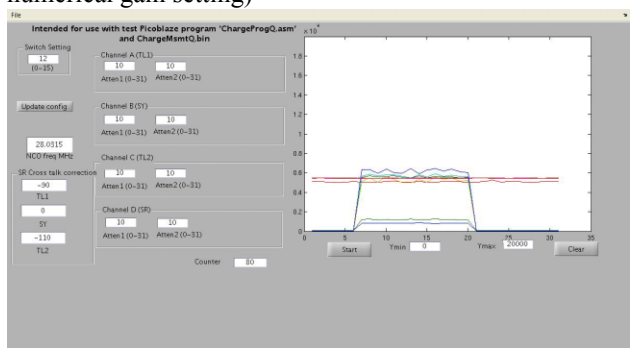

Figure 4: Graphical test application.

Table 1

Trig	Sig	Gain	DSP#	Start/us	Stop/us
0	0	1	0	0,19	2,18
0	1	1	1	2,96	6,94
0	3	2	0	2,96	8,59
0	1	1	1	21,48	25,46
0	3	2	0	21,48	27,11
0	1	1	1	40,00	43,98
0	3	2	0	40,00	45,63
0	1	1	1	9299	9303
0	3	2	0	9299	9304
0	1	1	1	18558	18562
0	3	2	0	18558	18564
0	1	1	1	38836	38840
1	2	1	0	0,19	2,18
1	3	2	1	4,17	9,80
1	3	2	0	18522	18528
1	3	2	1	37041	37046

RESULTS

The measured beam charge at the different stripline locations is shown in figures 5-8 during injections in 16 bunch mode (16 bunches equally seperated in the storage ring turn of 2.8μs).

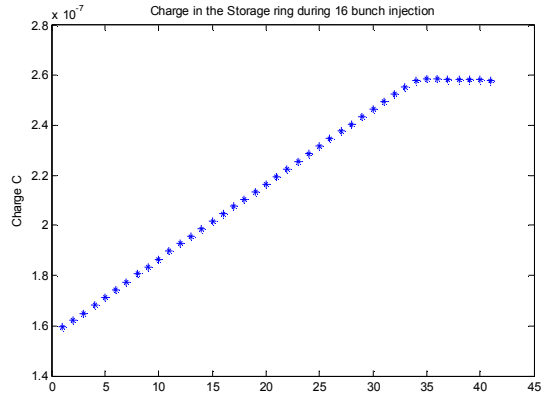

Figure 5: Charge measured in the storage ring (SR).

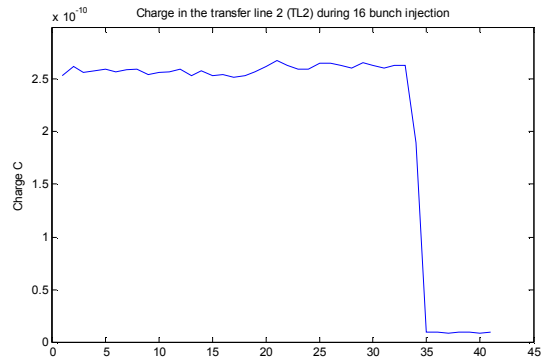

Figure 6: Charge measured in transfer line 2 (TL2).

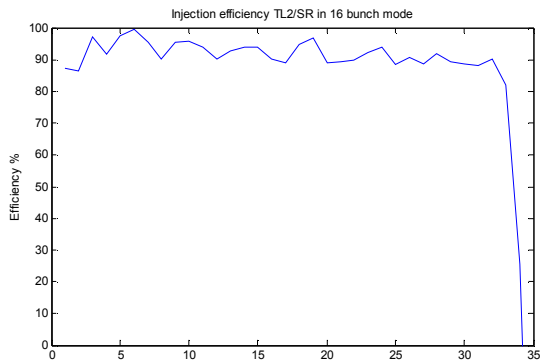

Figure 7: Injection efficiency TL2-SR.

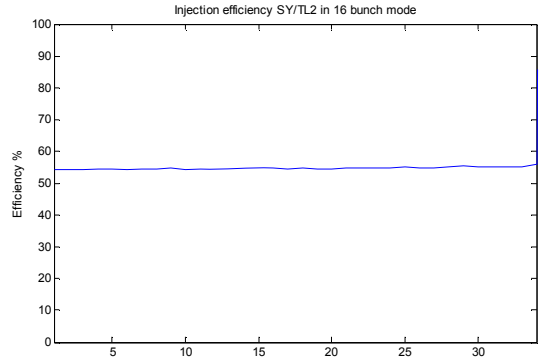

Figure 8: Injection efficiency SY-TL2.

Relative beam phase can also be measured between the booster and storage rings (see figure 9) at different times during the acceleration phase.

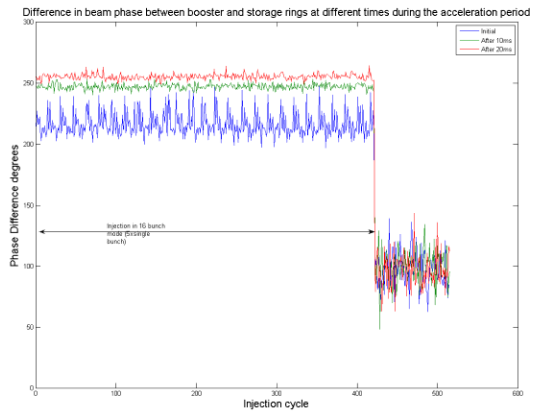

Figure 9: Beam phase difference between booster and storage ring.

CONCLUSION

A system using stripline pickups and a narrow band detection system with signal processing in an FPGA is shown to be an efficient method of measuring beam charge and relative phase. These measurements are of use for optimisation of the injection process.

REFERENCES

[1] G.A. Naylor, B. Joly "Determination of Beam Charge Using Stripline Signals at the RF Frequency by Fast Signal Processing in a FPGA". proceedings DIPAC 2005, Lyon p153

[2] A. Kosicek, "Libera Electron Beam Position Processor", Proceedings of the Particle Accelerator Conference, 2005. Page(s): 4284 - 4286