ANALOG FRONT-END ELECTRONICS IN BEAM INSTRUMENTATION

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Abstract

The work gives an overview of present and near future technological opportunities for the analog first conditioning and subsequent processing of sensor signal. The interactions between beam sensor capability, their signals characteristics and the system requirements are analyzed from different approaches as: full analog continuous, sampled time discrete, full digital time and amplitude discrete. Special attention will be given to the impact of measurement methods and new devices in circuits and instrumentation architecture design, especially from the metrological point of view

BASIC INSTRUMENTATION STRUCTURE

In order to reach the paper aim it is better to start little bit away, taking in consideration the basic structure of generic monitoring or control system, figure 1. We can identify several sub systems, characterized by specific functionalities, and devoted to collect some aspects of a physical event, modify them in order to allow the comparison with a reference and codify them in order to make easier any reasoning on it. The first reasoning results can be reprocessed with different strategies in order to reach a specific goal, decoded in physical attribute and actuated on the physic domain.

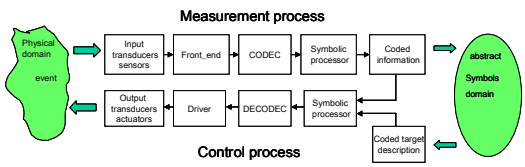

Figure 1. Structure of basic monitoring or control system

From the abstract point of view, in the main loop flow the same information but carried by different physical supports and code figure 2.

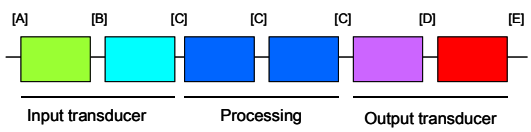

Figure 2. The same information is carried by different physical supports and code.

That is the physical world act as an information source, some of these are captured by a measurement process and converted in to symbols by a coding process, then some actions on the physical world can be performed by reasoning on the coded information and on the activity aim. With this approach we can define a criteria able to identify the transition from the transduction and the processing. We can consider transduction processes where the information carrier change block to block and processing where the physical carrier is stable. Taking in consideration how the information processing can be performed we can identify two different approaches: first based on a physical platform able to modify the carrier by different and controlled phenomena in order to approximate a required model, the analog solution, and the second based on coding processes and symbols manipulations driven by a defined paradigm, the symbolic or numeric solution. Which is the best? It is not easy to answer this question because the best performances or better the suitable performances depend on a large number of aspects as the system aim, the technology state of art, the number of systems required, the available technologies, the time to market, the available design tools, the cost performance ratio, the compliance with specific regulations, without to neglect the designer know-how and habits, his creativity, and his risk propensity etc. and in the end from the functional and technical specifications as accuracy, resolution bandwidth etc..

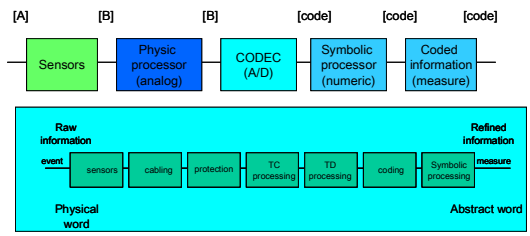

Figure 3. Model of information capture process

The information capture process can be modelled as shown in figure 3 where the coding process can be taken as the border from the physical processing, the analog space, and the symbolic or numeric processing, the digital space, moving this border, basically the A/D converter which perform the measurement process, we can modify dramatically architecture, performance, time delay, cost, knowledge engaged in the design etc. The works aim is to give an overview of some of these aspects and in special manner those related with the analog front end.

SILICON STATE OF ART

The silicon based integrated circuit (IC) industry has followed a strategy of shrinking device geometries for more than 30 years. With the assumption that the basic MOS transistor will remain the dominant switching device and the silicon will remain the dominant substrate material, it is widely believed that this process will continue for at least another ten years. However, there is great uncertainty about the ability to continue scaling metal–oxide–semiconductor field-effect transistor structures due to the considerable increasingly difficult materials and technology problems to be solved. The strategy of constantly shrinking device geometries and

increasing the number of devices per chip produces new technology generations, with deep performance and functionality improvements, every two to three years. This trend is commonly referred to as "Moore's Law". Each new generation has approximately doubled logic circuit density and increased performance by about 40% while quadrupling memory capacity. The increase in components per chip comes from three key factors first identified by Gordon Moore 40 years ago. The factor of two in component density comes from a shrink in each lithography dimension. An additional factor of two comes together from an increase in chip area and from device and circuit cleverness, providing the overall quadrupling in chip capacity. The apparent ease with which all this has happened has led to an expectation that faster and more powerful chips will continue to be introduced on the same schedule for the foreseeable future. In fact, the semiconductor industry itself has developed a "roadmap" based on this idea. The National and the International Technology Roadmap for Semiconductors (NTRS ITRS) now extend this device scaling and increased functionality scenario to the year 2014, at which point minimum feature sizes are projected to be 35 nm and chips with components are expected to be available. The requirements of a very thin thickness oxide is the main troubles source. The practical MOSFET structures generally require the gate dielectric thickness to be a few percent of the channel length. Silicon oxides thinner than about 1.0–1.5 nm, few atomic layers, conduct direct-tunnelling currents at the supply voltages below 1 volt and require a standby power too large for most IC applications. A new higher dielectric constant material system will have to be employed starting with the 100 nm generation. This kind of materials will allow a physically thicker dielectric layer to have a very thin equivalent SiO_2 thickness. Higher, up to 30, dielectric constant materials are also needed for dynamic random access memory (DRAM) storage capacitors. However, the requirements are quite different in this application because only a charge storage function is required. In a logic device because of the difference in permittivity between the silicon channel and the gate insulator, make the dielectric requirements very different and a good solution now does not exist. The gate electrode itself also presents some significant challenges. Polysilicon has been used for more than 25 years as the gate electrode material. However, decreasing its resistivity implies increasing the doping levels in the polysilicon. But this approach is limited by dopant solubility limits and by dopant out diffusion from the poly through the thin gate dielectric and into the silicon. This problem is particularly acute with P gates because boron diffuses rapidly through SiO_2. The likely solution is again new materials metal gate electrodes. But today is not available an optimum material. Ideally, the intrinsic channel resistance limits the current drive in a MOSFET. In practice, all the other parasitic resistances play a significant role and degrade the intrinsic device capability. Normal design procedures require these other resistances to total less than 10% of the channel resistance. Today there are no manufacturable means to reduce the contact resistance. Contacts are almost always made with either TiSi or CoSi contacting heavily doped silicon. The junction depths must keep on to decreasing to minimize short channel effects. Thus, doping levels in these regions must increase in order to keep resistances low. But doping concentrations are limited by dopant solubility and, hence, there are lower bounds on achievable sheet resistances. Today the integrated circuit industry gives some solution for the previous problems such as: Copper as connecting material supported by a low dielectric constant materials in order to reduce the interconnections time constant. This solution reduced the power requirement of 30% and the propagation time of 60% from 25 to 10 pS. SOI Silicon On Insulator, with the same design, speed up the device up to 20 %. Strained silicon. This material is obtained by growing, on a silicon bulk, about 2 μm of silicon-germanium alloy with a graded germanium concentration starting from the top with 20 % of Germanium. Over the silicon-germanium layer is deposited a 20 nm thin layer of pure silicon. The larger silicon germanium lattice strains the last silicon layer, because of the natural tendency for atoms inside compounds to align with one another. This effect gives an improvement of mobility, which can lead to chips up to 35 percent faster without having to shrink the size of transistors. High dielectric constant materials are normally used in memory devices, but are under development for logic application. This approach can delay or reduce in the near future the real problem connected with thinner gate isolator. The great driving force for the huge investments required in the actual technological effort is related to very large scale products as embedded applications in: automotive, medical, personal communication, home automation, and consumer which need, from one side, new high speed low power processors and, from the other side, high speed serial bus (10Gb/s) as the IEEE 802.11, and the IEEE 1394 in order to reduce the chips connections and to improve the system connectivity. Nevertheless 65nm technology is on the market, THz transition frequency transistors are available and 10÷15 GHz bandwidth 40÷80 GSample/s oscilloscopes are presented or announced

SAMPLING STATE OF ART

The high sampling rate is achieved by using the time-interleaved architecture. Here the signal is captured by a parallel array of slow digitizer that is sequentially clocked at a sub-Nyquist rate. The Nyquist criterion is satisfied when the signal is reconstructed in the digital domain. It is well known that the mismatches between digitizers in the array limit the dynamic range, so measured by the ENOB (equivalent number of bit). The process of ADC can be partitioned into two stages: (i) sampling, and (ii) quantization. Given the lack of an efficient digital optical switch, it has been prudently assumed by researchers that quantization is best done in electronic domain, and optics

should be considered as a mean to perform ultra fast sampling. Time-to-wavelength mapping, inherent in chirped optical signals, offers a natural mechanism for sampling a wideband RF signal and to demultiplex the samples into a parallel array of digitizers. In the discrete-time implementation of this approach the spectrum of pulses from an actively mode locked laser are broadened via a nonlinear pulse compression stage (super continuum generation) and sliced to attain discrete wavelength-to-time mapping. The multi-wavelength pulse stream samples the analog signal in an electrooptic modulator. A passive wavelength demultiplexer is then used to perform serial to parallel conversion. An array of slow (20 GSample/s) electronic digitizers quantize each channel. For an N channel system, the aggregate sampling rate would be Nfs, where fs is the sampling rate of individual electronic digitizers. This approach uses photonics for sampling and serial-to-parallel conversion; otherwise, the ADC architecture is identical to that of time-interleaved system. It offers an ultra-high sampling rate, with a resolution (ENOB), which will fundamentally be limited by the mismatch between different channels. A new A/D architecture is the so-called time-stretch ADC, shown in figure 4.

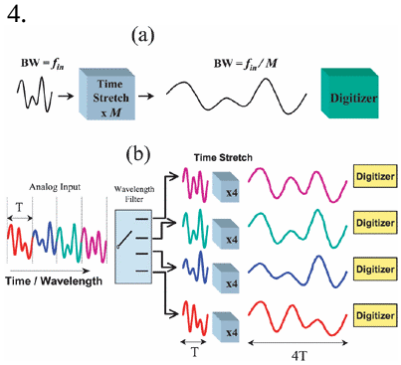

Figure 4. Time-stretch A/D architecture

Here the analog signal is slowed down prior to sampling and digitization by an electronic digitizer. Figure 4a, shown a time-limited input, single channel time-stretch ADC. A continuous-time input could be captured with a multi-channel system shown in figure 4b, where the partitioning of the continuous signal into parallel segments can be performed in the wavelength domain through time-to-wavelength mapping. Slowing down the signal prior to digitization has several advantages: for a stretch factor of M, the effective sampling rate is increased to Mfs. The input bandwidth of the electronic digitizer is also increased by M; the error associated with the jitter in the sampling clock of the digitizer is reduced due to a reduction in the signal slew rate. For a time-limited input, only a single digitizer is needed hence eliminating the inter-channel mismatch problem. For the continuous-time system it has recently been shown that mismatch errors can be corrected using the information available in the signal. This is an important advantage of the time-stretch ADC over the time-interleaved ADC. It exploits a fundamental difference between the two systems: in the former, the signal at each channel is sampled at or above the Nyquist rate, whereas in the latter it is sampled at a fraction of the Nyquist ra

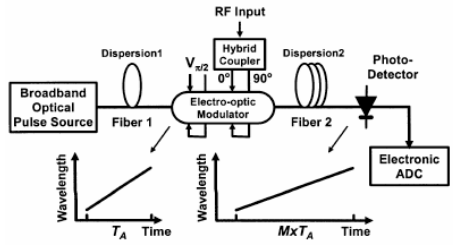

Figure 5. The time-stretch ADC physical implementation

Figure 5 shows the physical implementation for a single channel time-stretch ADC. The input electrical signal is modulated onto a chirped optical carrier. This is followed by dispersion, leading to temporal stretching of the modulation envelope. A single sideband modulation format eliminates the dispersion penalty that would otherwise place a limit on the electrical bandwidth. While the phase distortion remains, the effect is static and can be filtered in the digital domain. The differential scheme, using dual-output Mach-Zehnder modulator, is used to remove temporal distortions caused by the non-uniform power spectral density of the supercontinuum source and noise. A 120 GSample/s real-time digitization of a 20 GHz signal can be achieved by cascading a 6x photonic time-stretch preprocessor with the 20 GSample/s digitizer which has typically a 4 GHz bandwidth. The time-stretch increases the bandwidth to 24 GHz making it possible to capture a 20 GHz signal with the 4 GHz digitizer. The general approach for analog-to-digital conversion is to increase the performance of an electronic digitizer by optical signal pre-processing. Presently, the time-stretch technique appears to be the most promising in enabling ultra wideband analog-to-digital conversion with moderate resolutions 480GSample/s, 96GHz, bandwidth and 5 ENOB has been demonstrated.

INSTRUMENTATION TRENDS

The technological improvements can be seen from the instrumentation designers point of view as the availability of new class of components able to manage high-speed low-level signal in easy and cheaper manner. The availability of good analog switches and the large number of components engaged in the modern integrated circuits allow the implementation of very complex procedure derived from different methods and techniques. They are devoted to maintain the performance of physical processor, as the analog one, typically needed in the first interface with the physical domain for instance in the common mode rejection and low level amplifying with the explicit goal of realizing the whole system in one chip figure 6. The more suitable devices today are:

- Low level differential high-speed ADC
- SSP sensor signal processor
- FPAA field programmable analog array
- PSoC programmable systems-on-chip

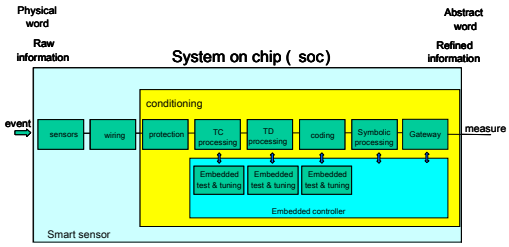

Figure 6. Instrumentation trends is one chip system

Low-level differential high-speed ADC the architecture of this device is more or less always the same: a controlled differential amplifier followed by a track-hold device and a flash analog to digital converter. The innovation is located in a dedicated embedded controller devoted to maintain the overall device performances by a continuous monitoring and adjusting of that. The today performances available on the market are 2.2 GSamle/s and 10 bit resolution. The SSP is a device family able to interface directly the low-level sensors signal today in the medium frequency range but, in the near future, also in the high frequency range. The family main characteristic is the customer availability of a general-purpose programmable microcontroller and/or a digital signal processor. A second important aspect is associated to the capability of those devices to stimulate the sensor and to interface many high-level communication networks. With this devices class is really possible to make one-chip instrumentation. FPAA field programmable analog array and design software introduce two new capabilities to the analog world. The first is the ability to translate complex analog circuits to a simple set of low-level functions, and thus to give designers the analog equivalent of an FPGA. The second is the ability to place analog functions under real-time software control within the system. By providing the analog equivalent of logic gates, FPAAs give designers the ability to describe analog functions such as gain stages and filters without reference to the underlying function. Lifted to this higher level of abstraction, the design process becomes so simple that non-specialists can create sophisticated circuits that would require weeks or months of design work with ASICs or discretes. Dynamic configurability adds to these capabilities by allowing analog functions to be updated in real time using automatically generated C-code. With analog functions under the control of the system processor, new device configurations can be loaded on the fly, allowing the device's operation to be "time-sliced," or to manipulate the tuning or the construction of any part of the circuit without interrupting operation of the FPAA, thus maintaining system integrity. As the physical platform, FPAA architecture is built on the natural precision, generic form, and switching fabric of a CMOS-based switched-capacitor (SC) network. The addition of a programming layer allows designers to implement an extremely wide variety of signal processing functions using digital configuration data. The core of the device is an array of identical Configurable Analog Blocks (CABs). The CABs are enriched with analog-to-digital converters, addressable memory, programmable comparators, references, and dedicated signal interfacing functions. PSoC programmable systems-on-chip developed by Cypress, PSoC mixed-signal arrays are programmable systems-on-chips (SOCs) that integrate a microcontroller and the analog and digital components that typically surround it in an embedded system. Dedicated development tools enable designers to select the precise peripheral functionality they desire, including analog functions such as amplifiers, ADCs, DACs, filters, comparators and digital functions such as timers, counters, PWMs, SPI and UARTs. The PSoC family's analog features are based both on time continuous structure and switched capacitor time discrete architecture and include rail-to-rail inputs, programmable gain amplifiers, low noise, low input leakage and low voltage offset up to 14-bit ADCs. The device digital side typically include flash memory, SRAM, multiplier, long accumulator, power and sleep monitoring circuits, and hardware I2C communications. Very recently has been announced a new component the PROC (programmable receiver on chip) able to support a Direct Sequence Spread Spectrum (DSSS) 2.4 GHz radio system mainly devoted to wireless USB technology.

BEAM POSITION MONITOR (BPM)

The Beam Position Sensor gives four voltage signals proportional to the beam horizontal and vertical positions. The beam position is determined from the ratio between the difference and the sum of two voltages induced in horizontal and vertical electrodes. The information processing can be performed in frequency domain by phase normalization and in time domain by time normalization. Both solutions need high-speed electronics and special care if high resolution is required. This kind of behaviour is quite common in sensor and instrumentation field. A typical example is the linear variable displacement transducers LVDT basically a differential transformer with variable magnetic coupling driven by the position of a moveable iron slug. For this reason a lot of conditioning architectures has been developed in order to improve the performance and the resolution. Some of these can be revised in order to verify if better features can be implemented to BPM. The state of art in BPM is well known and involving DSP, DRX, and FPGA. The four BPS voltage signals are down converted and coded in digital form, and then translated to base-band in the DRX. The DRX bandwidth is user selectable; this allows several measurements modes such as multi bunch, turn-by-turn, closed orbit and tune modes. When set to low bandwidth (typically 10 kHz) it allows following slow aspects of the beam evolution with a resolution of about 1 μm. When the bandwidth is wider (≥ 1MHz) it is possible to look at fast aspects of the beam position with a resolution lower than 20 μm in turn-by-turn mode. If the signal of BPS are combined by a hybrid device and sampled at 500MHz and then processed by multi DSP architecture with suitable firmware it is

possible to perform also bunch-to-bunch measurement. From the metrological point of view it is possible to observe that is quite difficult to obtain good resolution with single end architecture because the common mode weight and amplifier gain mismatching must be always lower than differential one. This condition is quite hard to maintain in the complex field especially if the amplifier gain is variable. The best choice in this situation is to perform an intrinsic difference of signal by a real differential amplifier with high common mode rejection or by a well-matched passive hybrid followed by a variable gain amplifier realized by means of a passive attenuator and a fixed gain amplifier. Today very interesting new devices are available on the market.

FUTURE BEAM POSITION INSTRUMENTATION

A forecast for near future beam position instrumentation goes in direction of wireless autonomous one chip system. A first step can engage a hybrid or a new generation differential amplifier followed by DRX or directly a differential DRX, a PSOC in order to perform the required data processing and continuous performance adjustment based on dedicated procedure and support the external connectivity figure 7a. The second step can be closer to single chip system by exploiting a SSP sensors signal processor where is possible to implement all the procedure needed to perform a good measurement also from the metrological point of view figure 7b.

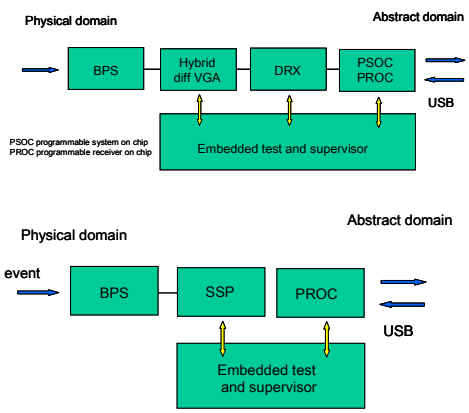

Figure 7. The future of BMP instrumentation

CONCLUSION

At the end of this overview the following statements are widely believable: also the instrumentation is going from module to chip. The new mixed signal array with on chip controller allows a more easy analog hardware practice. A high configurability is achievable by real time programmable physical connectivity. For some aspects more knowledge is required because the result is architecture dependent but good simulators and development tools are available for this purpose. The goal of low development time, low hardware platform dependence, and a suitable cost performance ratio become really more easily achievable.

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