AN IMPROVED PLL FOR TUNE MEASUREMENTS

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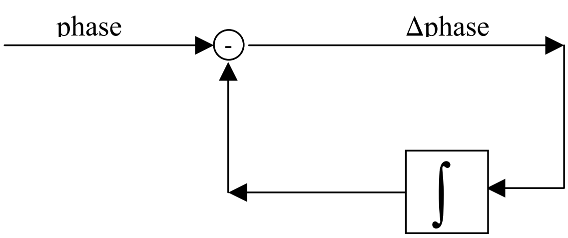
Abstract

Phase locked loop (PLL) systems are being used on several machines for continuous tune measurements. All these implementations are based on a continuous sinusoidal beam excitation and a monitoring of the resulting beam oscillation.
The key element determining the dynamic performance of such a PLL is the phase detector between the beam oscillation and the internal oscillation. Most circuits use a quadrature phase detector, for which the high frequency carrier at twice the excitation frequency is attenuated by a low-pass circuit. The remaining ripple of this component contributes to the bandwidth/noise performance of the PLL.

In this paper we propose an alternative solution for the filter, notably an adaptive notch filter. We explain in detail design considerations and the resulting improvements in PLL bandwidth and/or noise figure.

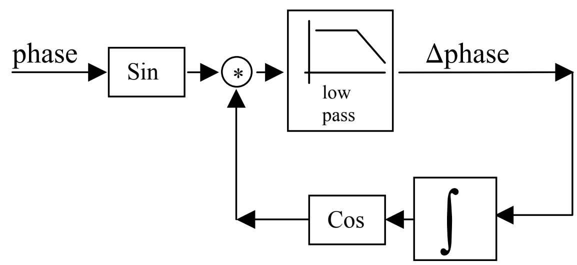
1 PLL BASICS

The following diagram shows the “raw” PLL:

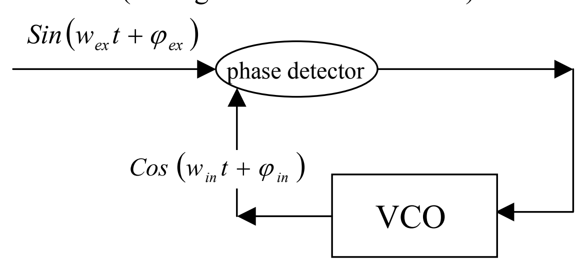


The definition of phase only has meaning when linked to a sine function. Since the sine function, which the PLL is locking on, is normally embedded within many other sine functions, only that phase should be extracted and the phases from the other sine function must be suppressed.

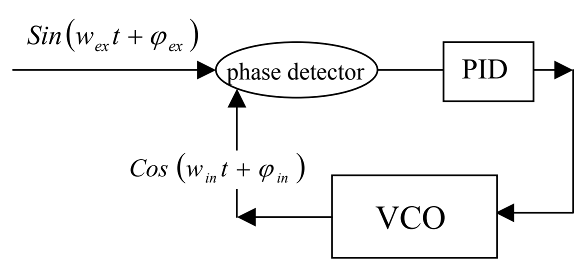
The phase difference could be extracted from the input sine function in a way similar to a Fourier integral, which is a very good filter. Assuming that the amplitude of the external sine has been normalized to 1 (e.g. by an amplitude regulation loop), the PLL becomes:



We can now introduce the concept of “phase detector” and VCO (Voltage controlled Oscillator):



Often a PID regulation is added (or in some cases, combined with the phase detector filter), which allows locking on widely varying input frequencies:



When the PLL is locked, the two inputs of the phase detector are 90 ° out of phase or “in quadrature”.

2 WHAT IS THE PROBLEM?

The output of a quadrature phase detector has a systematic noise, which limits the accuracy of the PLL. This error varies as $2\,w_{ex}\,t$, i.e. the double of the external frequency. The reason lies in the way the phase difference is calculated:

$$\Delta p = LowPass\left[2 \cdot \sin(wt + \varphi_{ex}) \cdot \cos(wt + \varphi_{in})\right]$$
$$\Delta p = LowPass\left[\sin(\varphi_{ex} - \varphi_{in}) + \sin(2wt + \varphi_{ex} + \varphi_{in})\right]$$

(*The above equations assume that the PLL is locked and therefore* $w \cong w_{ex} \cong w_{in}$)

The Low Pass filter is of course there to remove the term: $\sin(2wt + \varphi_{ex} + \varphi_{in})$ However, it is not perfect and a residue noise signal will be present at the output of the phase detector.

In order to enable the Low Pass filter to reject the *2wt* noise signal better, one could of course use a higher order filter or lower its cut-off frequency, but both of these methods could have a negative impact on the locking ability of the PLL. E.g. the lowering of the filter cut-off frequency would either lower the bandwidth or lower the damping of the PLL.

The Low Pass filter has several functions:

- It removes the *2w* noise term
- It removes the other frequency terms of the input signal (in fact it removes the products of these terms and the $\cos(wt + \varphi_{in})$ function
- Together with the PID regulator, it determines locking capability of the PLL

Therefore, a better way to remove the systematic *2w* frequency is to include a notch at *2w* in the Low Pass filter. Since only one frequency is removed, there will be no impact on the other qualities of the PLL.

3 A PROPOSED SOLUTION

A simple way to remove the *2w* noise is first to use a running average as a Low Pass filter. A running average has a frequency characteristic very similar to a first order filter with a cut-off frequency equal to:

$$w_{cut-off} = 2\pi / T$$

When using a running average as the Low Pass filter, the phase difference can then be recognized as a Fourier integral:

$$\Delta p = \frac{2}{T}\int_{t-T}^{t} Sin\left[w_{ex}t + \varphi_{ex}\right] * Cos\left[w_{in}t + \varphi_{in}\right]dt$$

This Fourier integral still has the *2w* noise. The origin of the noise is a mismatch between the integration time and the frequency. If $T = 2\pi / w$ there would be no noise!

The proposed solution is to subtract the term $\sin(w_{in}t + \varphi_{in})$ from the input signal, and the *2w* noise will be strongly rejected:

$$\Delta p = LP\left[2 \cdot \{\sin(wt + \varphi_{ex}) - \sin(wt - \varphi_{in})\} \cdot \cos(wt + \varphi_{in})\right]$$
$$\Delta p \approx \varphi_{ex} - \varphi_{in} \qquad \text{where } \varphi_{in} \cong \varphi_{ex} \wedge w_{in} \cong w_{ex}$$

The actual calculation is then:

$$\Delta p = \frac{2}{T}\int_{t-T}^{t} \left(V_{input} - Sin\left[w_{in}t + \varphi_{in}\right]\right) * Cos\left[w_{in}t + \varphi_{in}\right]dt$$

NB! *w_{in} is kept constant during the integration, which gives a better noise reduction because it excludes any noise from the regulation loop.*

The following example is a LEP type PLL, where a phase detector filter of the above type has been added. It is compared to the same PLL where the phase detector filter has been removed but instead a running average filter has been added to the output of the PLL. The two filters have the same integration time in order to have similar regulation characteristics:

PLL response to jump in frequency
Noise free input signal

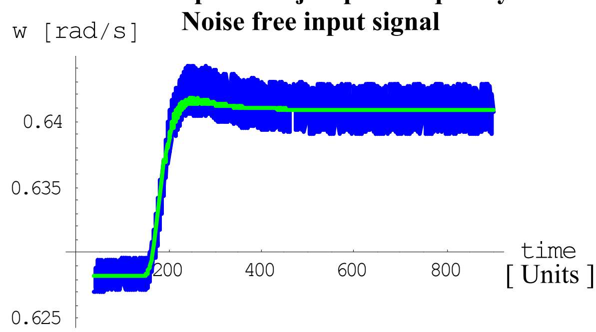


Fig 1. Blue curve: Filtered PLL output.
Green curve: Same PLL but with improved filter put onto the phase detector.

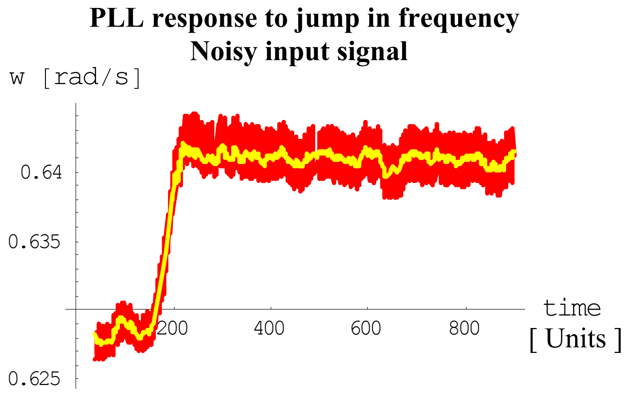


Fig 2. Red curve: Filtered PLL output.
Yellow curve: Same PLL but with improved filter put onto the phase detector.

In Fig.2 the ratio of the standard deviations for the red and yellow curves is ~ 5 i.e. in this example we get a factor 5 reduction in the noise. The less noise in the input signal, the more reduction we get in the *2w* noise signal.

In general one can say that a phase detector filter is better than a filter on the output of the PLL. The reason is that a phase detector filter removes the noise before it enters the regulation, so the noise does not stay in the loop but is removed at the entry.

In the following example, a neighboring frequency w_n with factor 5 higher amplitude and 0.1 Hz away from the locking frequency is introduced:

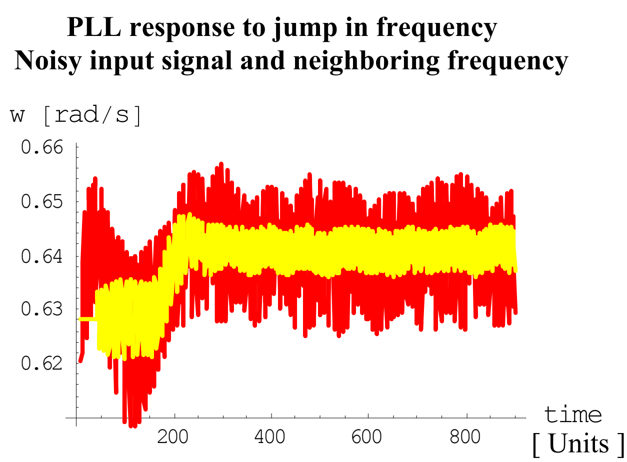


Fig 3. Red curve: Filtered PLL output.
Yellow curve: Same PLL but with improved filter put onto the phase detector.

Calculating the ratio of the standard deviations for the two curves, we get ~ 2.5 i.e. the PLL with the phase detector filter rejects the noise from the neighboring frequency 2.5 times better than the PLL with the filter on the output.

CONCLUSION

It is shown that a PLL with a quadrature phase detector is in the same family as a Fourier transformation.

The main point is to demonstrate that the *2w* noise that is inherent in quadrature phase detectors can be strongly rejected by an adaptive notch in the phase detector filter.

Further more it is shown that having the choice between a filter at the output of a PLL and a phase detector filter, it is better to use the phase detector filter because the noise of the input signal is then removed before it enters the regulation loop.

There is still scope for investigating the reduction of *2w* noise. How much can this noise be reduced as a function of the PLL regulation characteristics? And is it possible to integrate the phase detector filter with the PID regulation and still keep the notch filter?

ACKNOWLEDGEMENTS

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REFERENCES

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