Direct Sampling Digital Low-Level RF Control for CIAE BNCT Cyclotron

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ABSTRACT

Boron Neutron Capture Therapy（BNCT） can be delivered using a high current cyclotron, resulting more compact and environmentally friendly design, yet the difficulties remain in the cyclotron part, particularly in RF systems. The high beam loading challenges the stability of the amplifiers, as well as the control loops. Especially in our case, the wall loss of each cavity is more than the beam-loading power of the CIAE BNCT cyclotron. To address the heavy beam loading coefficient, a higher-performance ADRC control algorithm is evaluated, together with the regular PID control. In the meantime, a direct sampling/synthesizing digital low-level RF(LLRF) control hardware design is put forward to have more flexibility in control implementation. Since this new design adopts Xilinx SOC as the main controller, it is convenient to combine real-time control algorithm with high-level control through Advanced Extensible Interface. In this LLRF design, the amplitude and phase control using PID control is implemented in the PS end, and the tuning control is taking advantage of the ADRC algorithm in the PL end. Using a symmetrical design, together with the buncher control, in total, regulation of three loops are achieved using two control boards. The software/hardware design as well as the commission result will be reported in this paper.

Overview of BNCT LLRF system

The LLRF system of BNCT controls the amplitude, phase, cavity resonant frequency, and anomaly protection of the accelerating voltage in both cavities, as well as closed-loop control of amplitude and phase of the buncher.The diagram of BNCT LLRF system is show in Fig.1.

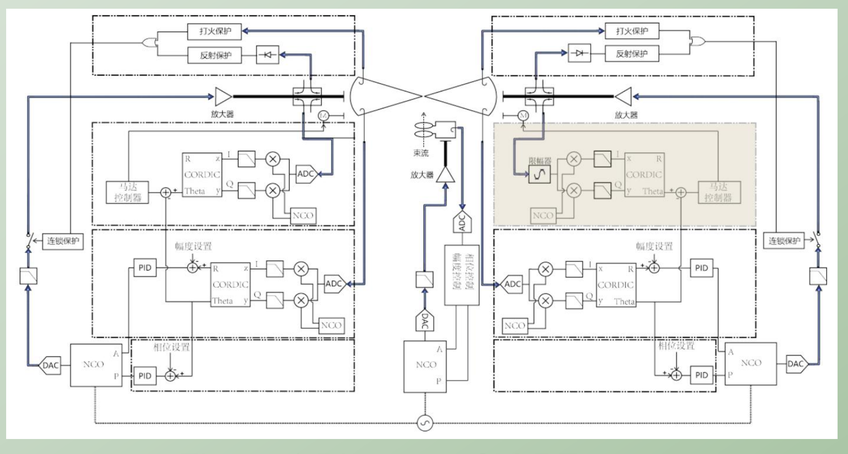
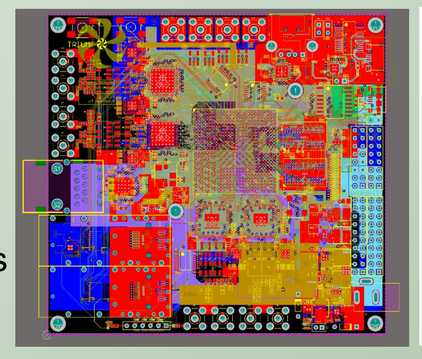
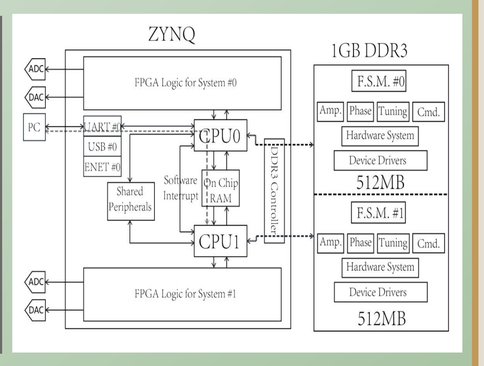


Figure 1.Diagram of LLRF system

Hardware and Firmware Design

The hardware architecture of the system uses ZYNQ series FPGA+ dual ARM architecture.In order to make full use of on-board resources and space，the hardware board of the LLRF system is a custom peripheral device, designed on a 14 - layer PCB of 11x11cm， as shown in Fig.2 a).The program of the system runs on a ZYNQ processor, where the FPGA is responsible for the digital PID and ADRC control of each control loop, and the ARM is responsible for the self-starting process of the RF system,the block of firmware as shown in Fig2. b) .



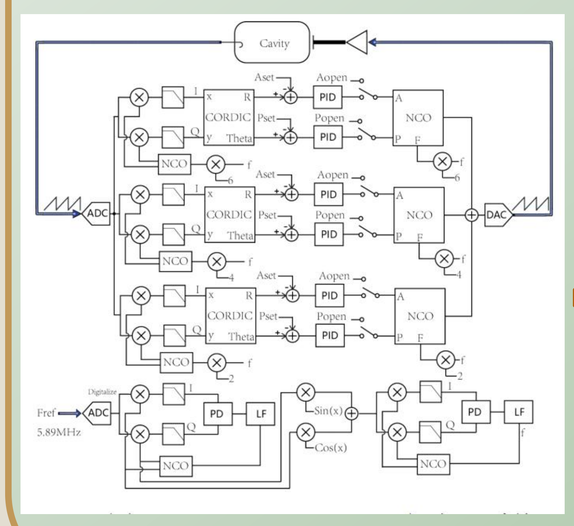


a) PCB Board layout b) Firmware design

Figure 2. System hardware and firmware design

Direct Sampling Method

In order to sample the RF signal with any clock, the LLRF system adopts direct digital sampling technology,as shown in Fig.3. One ADC channel is used to sample three sinusoidal signals at the same time, and the sampled signals are split into three channels inside the FPGA to process signals of corresponding frequencies respectively.



$$u_1(t) = A_0(t)\cos[\omega_0 t + \phi_0(t)] + A_1(t)\cos[\omega_1 t + \phi_1(t)] + A_2(t)\cos[\omega_2 t + \phi_2(t)]$$

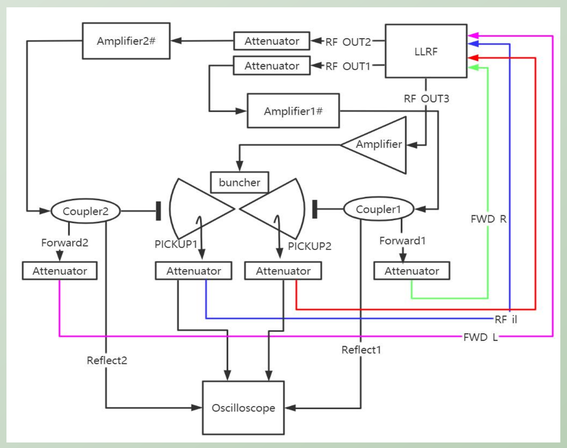
$$\begin{cases} I = \cos(\omega_0 t) \\ Q = \sin(\omega_0 t) \end{cases}$$

$$\begin{cases} I_o = A_0(t)/2\{\cos[(\omega_0+\omega_0)+\phi_0(t)]+\cos[(\omega_0-\omega_0)+\phi_0(t)]\} \\ +A_1(t)/2\{\cos[(\omega_1+\omega_0)+\phi_1(t)]+\cos[(\omega_1-\omega_0)+\phi_1(t)]\} \\ +A_2(t)/2\{\cos[(\omega_2+\omega_0)+\phi_2(t)]+\cos[(\omega_2-\omega_0)+\phi_2(t)]\} \\ Q_o = A_0(t)/2\{\sin[(\omega_0+\omega_0)+\phi_0(t)]+\sin[(\omega_0-\omega_0)+\phi_0(t)]\} \\ +A_1(t)/2\{\sin[(\omega_1+\omega_0)+\phi_1(t)]+\sin[(\omega_1-\omega_0)+\phi_1(t)]\} \\ +A_2(t)/2\{\sin[(\omega_2+\omega_0)+\phi_2(t)]+\sin[(\omega_2-\omega_0)+\phi_2(t)]\} \end{cases}$$

$$\begin{cases} I_o = A_0(t)/2\cos[\phi_0(t)] \\ Q_o = A_0(t)/2\sin[\phi_0(t)] \end{cases}$$

Test with cavity

Through previous low-power and high-power tests, the final beam loading debugging block diagram is shown in Fig.4 a).During the beam loading debugging, the output amplitude and phase of LLRF are adjusted to ensure the intensity of the beam and the coherence of the two cavities.The cavity pickup and reflection in the final continuous and stable operation are shown in Fig. 4 b).

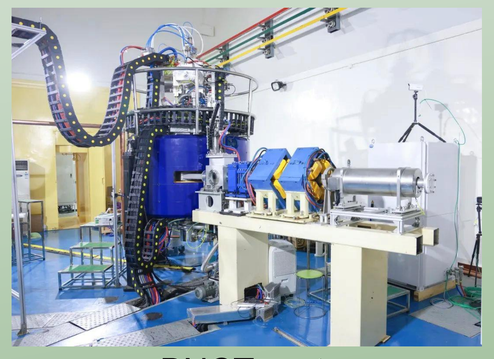


a) Test block diagram b) Test results

Figure 4. beam loadingest test

Conclusion

This set of digital LLRF system uses ZYNQ chip to make full use of on-chip resources, and completes the control function of LLRF system through a LLRF board card. During beam loading debugging, by increasing the LLRF system output, adjusting the output of the buncher and the phase difference between the two cavities, the problem that the beam intensity is not high enough under the condition of high beam loading is solved.



BNCT system