ISBN: 978-3-95450-212-7 ISSN: 2673-5482 doi:10.18429/JACoW-CYCLOTRONS2022-THP0007

DIRECT SAMPLING DIGITAL LOW-LEVEL RF CONTROL FOR CIAE BNCT CYCLOTRON

Xueer Mu, Zhiguo Yin, Junyi Wei, CIAE, Beijing, China
Xiaoliang Fu†, TRIUMF, Vancouver, Canada

Abstract

Boron neutron capture therapy (BNCT) can be delivered using a high current cyclotron, resulting more compact and environmentally friendly design, yet the difficulties remain in the cyclotron part, particularly in RF systems. The high beam loading challenges the stability of the amplifiers, as well as the control loops. Especially in our case, the wall loss of each cavity is more than the beam-loading power of the CIAE BNCT cyclotron. To address the heavy beam loading coefficient, a higher-performance ADRC control algorithm is evaluated, together with the regular PID control. In the meantime, a direct sampling/synthesizing digital low-level RF control hardware design is put forward to have more flexibility in control implementation. Since this new design adopts Xilinx SOC as the main controller, it is convenient to combine real-time control algorithm with high-level control through Advanced Extensible Interface. In this LLRF design, the amplitude and phase control using PID control is implemented in the PS end, and the tuning control is taking advantage of the ADRC algorithm in the PL end. Using a symmetrical design, together with the buncher control, in total, regulation of three loops are achieved using two control boards. The software/hardware design as well as the commission result will be reported in this paper.

INTRODUCTION

The boron neutron capture therapy (BNCT) method can protect normal cells as much as possible while killing cancer cells. BNCT technology based on high current proton accelerators is gaining increasing attention in various countries due to the adjustable energy of the neutron beam of the accelerator and the fact that the accelerator also has safety advantages that reactors do not possess [1, 2].

The CYCIAE-14B cyclotron [3] for BNCT developed by the CIAE provides a 14 MeV, 1 mA proton beam for the production of neutrons for BNCT. The CYCIAE-14B cyclotron uses two 20 kW transmitters to drive two independent cavities respectively, and a 300 W amplifier to drive the buncher to increase the beam intensity. The low-level RF (LLRF) system requires amplitude and phase control of the three signals and tuning control of the two cavities [4]. Based on the characteristics of CYCIAE-14B high-frequency system, this paper proposes a design method of direct sampling/synthesis all digital low level control system, and completes the debugging task of this digital low level control system in CYCIAE-14B.

† xfu@triumf.ca

DESIGN OF BNCT LLRF SYSTEM

The design requirement of the digital LLRF system designed by the CIAE is to realize a set of broadband RF system to control the amplitude and phase of three channels of signals and the tuning of two cavities. The digital LLRF system is universal and can be applied to the RF control system of cyclotron in the CIAE. This paper mainly introduces the application of this system in CYCIAE-14B LLRF system. The LLRF system block diagram of CYCIAE-14B cyclotron is shown in Fig. 1.

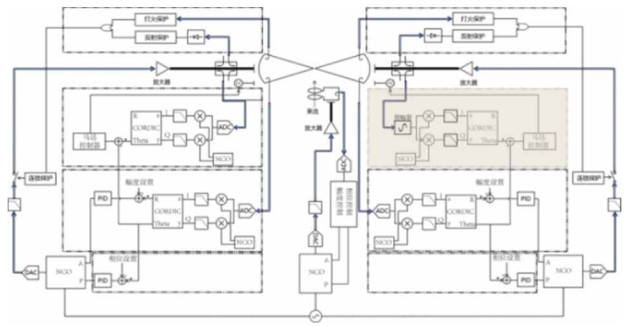

Figure 1: The LLRF system block diagram of CYCIAE-14B.

Hardware Design

The hardware architecture of the system is based on the ZYNQ series FPGA + dual ARM architecture. The FPGA is mainly used to modulate and demodulate the digital signal: After ADC sampling, the radio-frequency sampling signal and the sampling signal of the buncher form the IQ sequence. FPGA reads the IQ sequence, calculates the amplitude and phase information, and completes the demodulation operation. The function of the modulator is realized by DAC and NCO. The output amplitude of NCO is modulated by multiplying the output of NCO by hardware multiplier, and the modulation result is output by DAC to drive the amplifier. The dual ARM structure completes the control of the two RF auto-start processes [5], abnormal protection and online parameter modification, allowing the two RF systems to operate independently. The hardware system is designed with a 14-layer PCB and the physical diagram of the hardware system is shown in Fig. 2.

The LLRF system board will be installed in a LLRF chassis which will display the LLRF operation on the front panel. In order to visually display the running state of the LLRF system and provide driving for the stepping motor, a motherboard has been designed for the system and the core board can be plugged into the motherboard for use. A physical diagram of the motherboard is shown in Fig. 3. In the design of the motherboard, all input and output ports of

ISBN: 978-3-95450-212-7 ISSN: 2673-5482 doi:10.18429/JACoW-CYCLOTRONS2022-THP0007

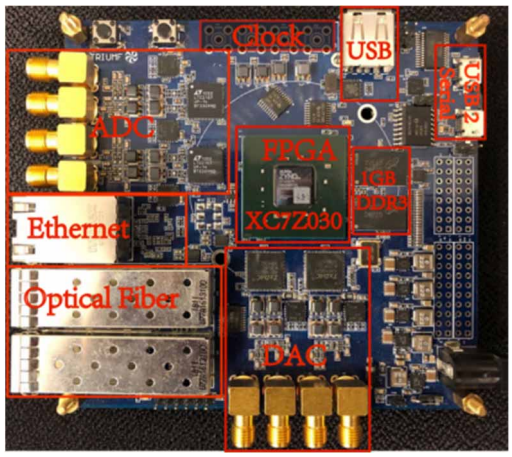

Figure 2: Digital LLRF platform for BNCT cyclotron.

Figure 3: Motherboard for LLRF system board.

the daughter board are isolated in order to achieve complete electrical isolation of the inputs and outputs, increase the anti-interference capability and make the system work stably.

Core Algorithm

The core control algorithm of FPGA is realized by digital PID controller, and the realization expression of digital PID controller is:

$$u(k) = K_p\left\{e(k) + \frac{T}{T_I}\sum_{k=0}^{n} e(k) + \frac{T_D}{T}[e(k) - e(k-1)]\right\} \quad (1)$$

The expression for an incremental PID controller can be obtained from the above equation as:

$$\begin{aligned}\Delta u(k) &= u(k) - u(k-1)\\ &= K_p[e(k) - e(k-1)] + K_I e(k)\\ &\quad + K_D[e(k) - 2e(k-1) + e(k-2)] \end{aligned} \quad (2)$$

This expression is the basis for PID control using FPGAs. In practice, amplitude PID controller requires special handling of integral saturation and increased output limits. Unlike amplitude PID controllers, phase PID controller doesn't need to consider the case of integral saturation and do not need to add output limits.

In practical tests, in order to address the heavy beam loading coefficient, a higher performance ADRC control algorithm is proposed, which retains the characteristics of "error control by error" of PID technology, but also addresses the shortcomings of PID by introducing a non-linear Tracking Differentiator (TD), an Extended State Observer (ESO) and a Nonlinear State Error Feedback Control Law (NLSEF).The ADRC control algorithm using TD and ESO to process the reference input and system output respectively, and selecting the appropriate non-linear combination of state errors to obtain the NLSEF of the system, so as to obtain the output of the controller.

TEST RESULTS

The debugging block diagram of LLRF system is shown in Fig. 4.The power of the LLRF system output is increased after passing through the amplifier, and after the directional coupler, the reflection of the coupler is directly connected to the oscilloscope, and the forward signal is connected to the LLRF system through the attenuator; the pickup from the cavity is passed through the attenuator and power divider respectively and is connected one way to the oscilloscope and the other way to the LLRF system. At the same time the LLRF system output RF_OUT3 is used as the input to the buncher. With the wiring connected, the control of the LLRF system is implemented using the upper computer program. The control of the LLRF system is realised by computer program, which is used to set the closed loop point of the Dee voltage after the closed loop has been achieved in both cavities.

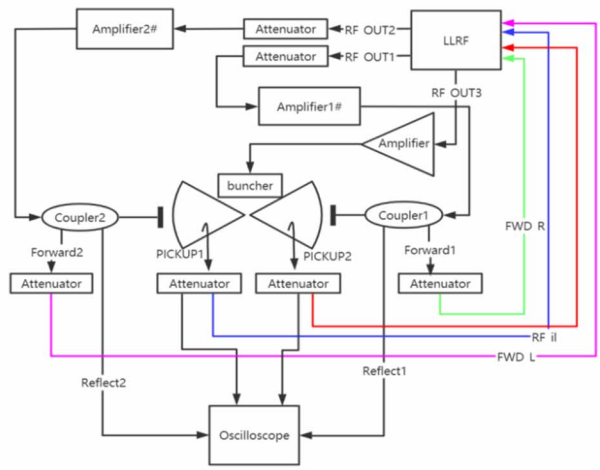

Figure 4: The debugging block diagram of LLRF system.

In the process of commissioning the accelerator with beam current, the resonant frequency of the RF cavity will shift due to beam loading [6] and heat loss causing the phase bias value calibrated when the beam was not added to be no longer accurate. Therefore, in the beam loading commissioning, the Dee voltage is set low, and after the system is closed loop, the phase set point is adjusted at a lower power level to minimise the reflected power, when the RF cavity is in resonance, the Dee voltage set point is then continuously increased to eventually achieve the power required for closed loop.

ISBN: 978-3-95450-212-7 ISSN: 2673-5482 doi:10.18429/JACoW-CYCLOTRONS2022-THP0007

CONCLUSION

This set of digital LLRF system uses ZYNQ chip to make full use of on-chip resources, and completes the control function of LLRF system through a LLRF board card. During beam loading debugging, by increasing the LLRF system output, adjusting the output of the buncher and the phase difference between the two cavities, the problem that the beam intensity is not high enough under the condition of high beam loading is solved.

REFERENCES

[1] M. A. Dymova, S. Y. Taskaev, V. A. Richter, and E. V. Kuligina, "Boron neutron capture therapy: current status and future perspectives", *Cancer Commun.*, vol. 40, pp. 406-421, 2020. doi:10.1002/cac2.12089

[2] A. J. Kreiner, J. Bergueiro, D. Cartelli, *et al.*, "Present status of accelerator-based BNCT", *Rep. Practical Oncol. Radiother.,* vol. 21, pp. 95-101, 2016. doi:10.1016/j.rpor.2014.11.004

[3] T. Zhang, B. Cui, Y. Lv, "BRIF: From the first proton beam to RIB production", *Nucl. Instrum. Methods*, vol. 463, pp. 123-127, 2020. doi:10.1016/j.nimb.2019.06.045

[4] X. Fu, Z. Yin, K. Fong, *et al.*, "LLRF controller for high current cyclotron-based BNCT system", *IEEE Trans. Nucl. Sci.*, vol. 68, pp. 2452-2458, 2021. doi:10.1109/TNS.2021.3097702

[5] Z. Yin, X. Fu, B. Ji, *et al.*, "Digital control in LLRF system for CYCIAE-100 cyclotron", *Nucl. Instrum. Methods*, vol. 819, pp. 33-36, May. 2016 doi:10.1016/j.nima.2016.02.100

[6] X. Chengye, W. Zhijun, G. Zheng, H. Guirong, H. Ran, and M. Jinying, "Simulation and evaluation of beam loading feedforward Compensation for CiADS Linac", *Nucl. Phys. Rev.*, vol. 37, pp. 848-853, 2020. doi:10.11804/NuclPhysRev.37.2020023